QP SEMICONDUCTOR

QPL4C381

January 25, 2012

QPL4C381 16-bit Cascadable Arithmetic/Logic Unit

General Description

The QPL4C381 is designed as a pin for pin replacement for the Logic Devices L4C381 device. The QPL4C381 is a high speed 16-bit ALU (Arithmetic/Logic Unit). It combines four (4) 381 4-bit ALUs, a lookahead carry generator and miscellaneous interface logic into a single 68 pin device. It supports high speed pipelined architectures and single 16-bit bus architectures. It retains full functional and performance compatibility with the Logic Devices L4C381 and even older 381 bipolar devices.

- Replacement for the Logic Devices L4C381.
- High-speed, 16-bit ALU
- Input and Output registers can be made transparent
- Cascadeable with or without carry lookahead
- Extension to the 54S381 instruction set
- Force A or B → 0 allows two's complement, PASSA, PASSB instructions
- Internal feedback path for accumulation
- Low-power, high speed CMOS Technology
- All status and carry outputs available.

Architecture

The QPL4C381 operates on the 16-bit operands "A" and "B", and produces a single 16-bit result "F". Three select lines control the ALU and provide 3 arithmetic, 3 logical and 2 initialization functions. Full ALU status is provided, allowing the device to be cascaded to form longer word lengths. Registers are provided on both the ALU inputs and the output, and may be bypassed. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs for use in chain operations and accumulation. The A or B input to the ALU can be forced to zero allowing unary functions to be performed on either operand.

ALU Operation

Select lines S_0-S_2 determine the operation to be performed. The ALU functions and their select codes are:

S_2	S_1	S_0	Function
0	0	0	CLEAR (F = 0000 0000 0000 0000)
0	0	1	NOT (A) + B
0	1	0	A + NOT (B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F = 1111 1111 1111 1111)
			The functions B minus A, and A minus B can be achieved by setting the carry input (C_0) of the least significant slice and selecting codes 001 and 010 respectively.

ALU Status

The ALU provides Overflow and Zero status bits. Carry, Propagate and Generate outputs are provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all sixteen outputs bits are zero. The Generate, Propagate, C16 and Overflow Flags for the A + B operation are defined:

$$\text{Bit Carry Generate} = g_i = A_iB_i \qquad \text{for } i = 0, 1, \ldots, 15$$
$$\text{Bit Carry Propagate} = p_i = A_i + B_i \qquad \text{for } i = 0, 1, \ldots, 15$$
$$P_0 = p_0 \qquad \text{for } i = 1, 2, \ldots, 15$$
$$P_i = {}_{pi}(P_{i-1})$$

and

$$G0 = g0$$
$$G_i = g_i +_{pi}(G_{i-1}) \qquad \text{for } i = 1,2,\ldots,15$$
$$C_i = G_{i-1} + P_{i-1}(C_{i-1}) \qquad \text{for } i = 1,2,\ldots,15$$

then

$$\overline{G} = \text{NOT}(G_{15})$$
$$\overline{P} = \text{NOT}(P_{15})$$
$$C_{16} = G_{15} + P_{15}C_{15}$$
$$\text{OVF} = C_{15} \text{ XOR } C_{16}$$

Operand Registers

The QPL4C381 has two 16-bit wide input registers for operands A and B. These are triggered by a rising edge on the common clock pin. Each register is independently enabled by control signals $\overline{EN}_A$ and $\overline{EN}_B$.

This allows the QPL4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be made transparent with the FT_{AB} control line. When FT_{AB} control is asserted, the A and B input registers are bypassed. However, they continue to function normally via the $\overline{EN}_A$ and $\overline{EN}_B$ controls. The contents of the input registers will be available to the ALU if the FT_{AB} control is released.

Output Register

The output of the ALU drives the input of a 16-bit register. This rising-edge triggered register is clocked by the same clock as the input registers. The output register is enabled by the $\overline{EN}_F$ control signal. By disabling the output register,

intermediate results can be held while loading new input operands. Tri-state drivers controlled by the $\overline{OE}$ input allow the QPL4C381 to be used in a single bidirectional bus system. The output register can be made transparent by asserting the FT_F control signal. When FT_F is asserted, the output register is bypassed, however, it continues to function normally via the $\overline{EN}_F$ control signal. The contents of the output register will be available on the output pins if FT_F is released. With both FTAB and FTF true (high) the QPL4C381 is functionally identical to four cascaded 54S381 devices.

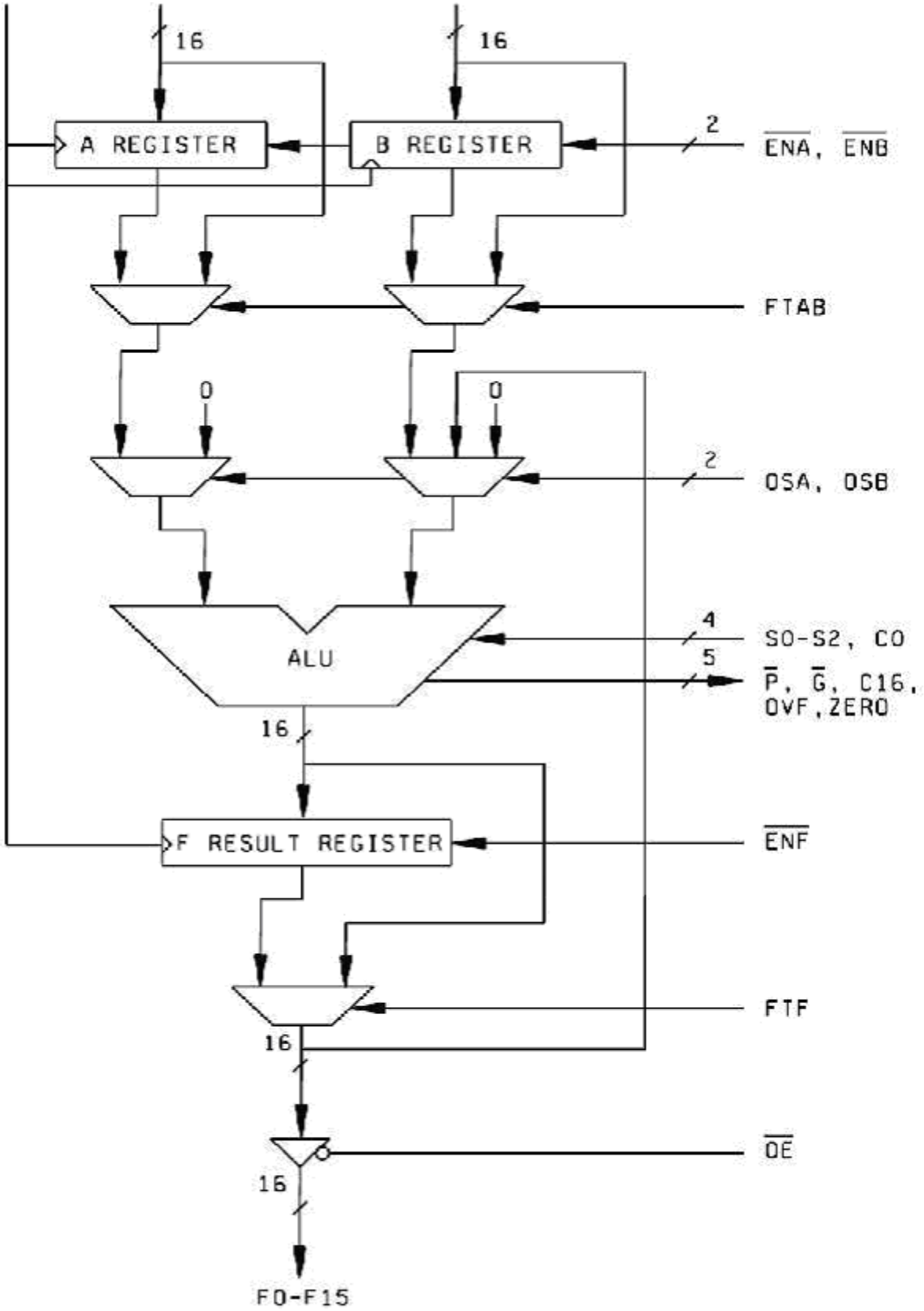
Operand Selection

The two operand selection lines OS_A/OS_B control multiplexers immediately preceding the ALU inputs. The multiplexers provide an operand force to zero function as well as provide a result feedback to the B input. Either A or B operands can be forced to zero.

OS_A	OS_B	Operand B	Operand A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

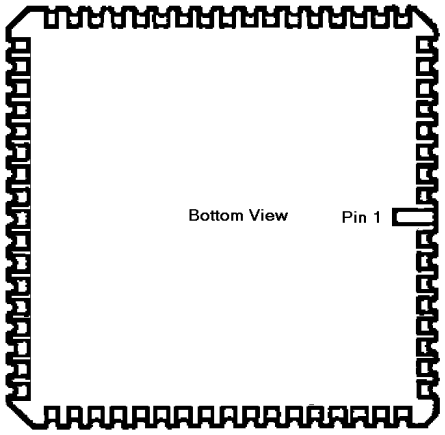
When both operand select lines are zero/low, the QPL4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input of the ALU. This allows accumulation operations to be performed by providing new operands via the A inputs. The accumulator can be preloaded from the A input by setting OS_A as a one/high. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. This feedback operation is not effected by the state of the FT_F control. The F outputs may be driven directly by the ALU (FT_F = one/high). The output register continues to function and provides the ALU B operand source.

Block Diagram

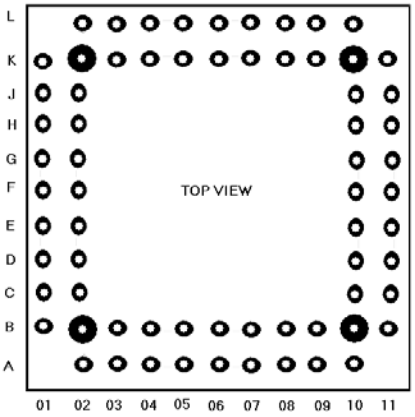


Connection Diagrams

LCC



PGA



FUNCTION	DIP/ LCC	PGA	FUNCTION	DIP/ LCC	PGA	FUNCTION	DIP/ LCC	PGA	FUNCTION	DIP/ LCC	PGA
A_O	1	F02	V_{CC}	18	B06	F_8	35	F10	$\overline{EN}_A$	52	K06
A_1	2	F01	GND	19	A06	F_7	36	F11	B_0	53	L06
A_2	3	E02	C_{16}	20	B07	F_6	37	G10	B_1	54	K05
A_3	4	E01	$\overline{P}$	21	A07	F_5	38	G11	B_2	55	L05
A_4	5	D02	$\overline{G}$	22	B08	F_4	39	H10	B_3	56	K04
A_5	6	D01	ZERO	23	A08	F_3	40	H11	B_4	57	L04
A_6	7	C02	OVF	24	B09	F_2	41	J10	B_5	58	K03
A_7	8	C01	$\overline{ENF}$	27	A09	F_1	42	J11	B_6	59	L03
A_8	9	B01	FTF	26	A10	F_0	43	K11	B_7	60	L02
A_9	10	B02	$\overline{OE}$	27	B10	C_0	44	K10	B_8	61	K02
A_{10}	11	A02	F_{15}	28	B11	S_0	45	L10	B_9	62	K01
A_{11}	12	B03	F_{14}	29	C10	S_1	46	K09	B_{10}	63	J02
A_{12}	13	A03	F_{13}	30	C11	S_2	47	L09	B_{11}	64	J01
A_{13}	14	B04	F_{12}	31	D10	OS_A	48	K08	B_{12}	65	H02
A_{14}	15	A04	F_{11}	32	D11	OS_B	49	L08	B_{13}	66	H01
A_{15}	16	B05	F_{10}	33	E10	FT_{AB}	50	K07	B_{14}	67	G02
CLK	17	A05	F_9	34	E11	$\overline{EN}_B$	51	L07	B_{15}	68	G01

Pin Name	Function
A_0-A_{15}	"A" data input bus. The 16-bit "A" input data bus to the ALU.
B_0-B_{15}	"B" data input bus. The 16-bit "B" input data bus to the ALU.
F_0-F_{15}	"F" data output bus. The 16-bit "F" output data bus from the ALU.
C_O	Carry input. This input is used in arithmetic operations.
C_{16}	Carry out. Output flag that provides the carry propagate information from an arithmetic operation.
$\overline{P}$	Carry propagate output. Output flag that provides the carry propagate information from an arithmetic operation. Used in cascaded systems.
$\overline{G}$	Carry generate output. Output flag that provides the carry generate information from an arithmetic operation. Used in cascaded systems

Pin Name	Function
OVF	Overflow output. Output flag tht provides ALU result overflow information from an arithmetic operation.
ZERO	Zero output. Output flag that provides ALU result overflow information from an arithmetic operation.
$\overline{EN}_A$	"A" register enable input. Control input used to either load or hold data into the "A" register.
$\overline{EN}_B$	"B" register enable input. Control input used to either load or hold data into the "B" register.
FT_{AB}	Feedthrough "AB" input. Control input used to select whether the input registers are bypassed or not.
$\overline{ENF}$	"F" register enable output. Control input used to either load or hold data into the "F" register.
FTF	Feedthrough "F" input. Control input used to select whether the output register is bypassed or not.
OS_A, OS_B	Operand select inputs. Selects input data to the ALU on the "A" and "B" ports.
S_0-S_2	Instruction select inputs. Controls which operation the ALU will perform
$\overline{OE}$	Output enable input. Controls the "F" output bus by enabling and disabling the outputs.
CLK	Clock input. The master clock input for all device registers.
V_{CC}, GND	Power supply.

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
V_{CC} Supply Voltage with respect to GND	-0.5 to +7.0	Volts DC	
Input Signal with respect to GND	-0.5 to V_{CC}+0.5	V	
Signal applied to high impedance outputs	-0.5 to V_{CC}+0.5	V	
Maximum Power Dissapation (P_D)	420	mW	/1
Current into Low Outputs	25	mA	
Storage Temperature Range	-65 to +150	ºC	
Operating Temperature (Ambient)	-55 to +125	ºC	
Lead Temperature (soldering, 10 seconds)	+300	ºC	
Junction Temperature (T_J)	+175	ºC	

1/ - Must withstand the added P_D due to I_{OS}

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
Case Operating Range (T_c)	-55C to +125	ºC	/2

2/ – Maximum PD, Maximum T_J Are Not to Be Exceeded

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$, $V_{SS}=0V$, $4.5V \le V_{CC} \le 5.5V$ Unless Otherwise Specified	Device	Min	Max	Unit
Output High Voltage	V_{OH}	V_{CC}= 4.5V, I_{OH}= -2mA	All	2.4		V
Output Low Voltage	V_{OL}	V_{CC}= 4.5V, I_{OL}= 8mA	All		0.5	V
Input High Voltage	V_{IH}		All	2.0		V
Input Low Voltage	V_{IL}		All	0		V
Input Current	I_{IX}	V_{CC}= 5.5V	All		±20	µA
Output Leakage Current	I_{OZ}	V_{CC}= 5.5V	All		±20	µA
Dynamic Supply Current	I_{CC1}	V_{CC}= 5.5V /5	All		30	mA
Quiescent Power Supply Current	I_{CC2}	V_{CC} = 5.5V /6	All		1.5	mA
Input Capacitance /8	C_{IN}	V_{IN} = 0V, V_{CC} = 5.0V T_A = 25°C, f = 1MHz	All		5	pF
		V_{OUT} = 0V, V_{CC} = 5.0V T_A = 25°C, f = 1MHz	All		8	pF
Clock to F_0-F_{15}	1	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		28	ns
			QPL4C381-35		26	ns
Clock to $\overline{P}$, $\overline{G}$	2	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		34	ns
			QPL4C381-35		28	ns
Clock to OVF, ZERO	3	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		50	ns
			QPL4C381-35		34	ns
Clock to C_{16}	4	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		34	ns
			QPL4C381-35		28	ns
C_0 to OVF, ZERO	5	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		32	ns
			QPL4C381-35		22	ns
C_0 to C_{16}	6	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		23	ns
			QPL4C381-35		22	ns
S_0-S_2,OS_A,OS_B to $\overline{P}$,$\overline{G}$	7	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to OVF, ZERO	8	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to C_{16}	9	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
Clock to F_0-F_{15}	10	FTAB=0, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		56	ns
			QPL4C381-35		34	ns
Clock to $\overline{P}$,$\overline{G}$	11	FTAB=0, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		34	ns
			QPL4C381-35		28	ns
Clock to OVF, ZERO	12	FTAB=0, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		50	ns
			QPL4C381-35		34	ns

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Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Clock to C_{16}	13	FTAB=0, FTF=1,	QPL4C381-45		34	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
C_0 to F_0-F_{15}	14	FTAB=0, FTF=1,	QPL4C381-45		32	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		26	ns
C_0 to OVF, ZERO	15	FTAB=0, FTF=1,	QPL4C381-45		32	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		22	ns
C_0 to C_{16}	16	FTAB=0, FTF=1,	QPL4C381-45		23	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		22	ns
S_0-S_2,OS_A,OS_B to F_0-F_{15}	17	FTAB=0, FTF=1,	QPL4C381-45		46	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		30	ns
S_0-S_2,OS_A,OS_B to $\overline{P}$,$\overline{G}$	18	FTAB=0, FTF=1,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to OVF, ZERO	19	FTAB=0, FTF=1,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to C_{16}	20	FTAB=0, FTF=1,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} to $\overline{P}$,$\overline{G}$	21	FTAB=1, FTF=0,	QPL4C381-45		32	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} to OVF, ZERO	22	FTAB=1, FTF=0,	QPL4C381-45		46	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} to C_{16}	23	FTAB=1, FTF=0,	QPL4C381-45		36	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
Clock to F_0-F_{15}	24	FTAB=1, FTF=0,	QPL4C381-45		28	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		26	ns
C_0 to OVF, ZERO	25	FTAB=1, FTF=0,	QPL4C381-45		32	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		22	ns
C_0 to C_{16}	26	FTAB=1, FTF=0,	QPL4C381-45		23	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		22	ns
S_0-S_2,OS_A,OS_B to $\overline{P}$,$\overline{G}$	27	FTAB=1, FTF=0,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to OVF, ZERO	28	FTAB=1, FTF=0,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to C_{16}	29	FTAB=1, FTF=0,	QPL4C381-45		38	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} to F_0-F_{15}	30	FTAB=1, FTF=1,	QPL4C381-45		45	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		30	ns
A_0-A_{15}, B_0-B_{15} to $\overline{P}$,$\overline{G}$	31	FTAB=1, FTF=1,	QPL4C381-45		32	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} to OVF, ZERO	32	FTAB=1, FTF=1,	QPL4C381-45		46	ns
		C_L=30pF, V_{CC}=4.5V	QPL4C381-35		28	ns

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Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
A_0-A_{15}, B_0-B_{15} to C_{16}	33	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		36	ns
			QPL4C381-35		28	ns
C_0 to F_0-F_{15}	34	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		32	ns
			QPL4C381-35		26	ns
C_0 to OVF, ZERO	35	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		32	ns
			QPL4C381-35		22	ns
C_0 to C_{16}	36	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		23	ns
			QPL4C381-35		22	ns
S_0-S_2,OS_A,OS_B to F_0-F_{15}	37	FTAB=1, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		46	ns
			QPL4C381-35		30	ns
S_0-S_2,OS_A,OS_B to $\overline{P}$,$\overline{G}$	38	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to OVF, ZERO	39	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
S_0-S_2,OS_A,OS_B to C_{16}	40	FTAB=1, FTF=1, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		38	ns
			QPL4C381-35		28	ns
Clock (OS_A,OS_B=0) to F_0-F_{15}	65	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		56	ns
			QPL4C381-35		34	ns
Clock (OS_A,OS_B=0) to $\overline{P}$,$\overline{G}$	41	FTAB=0, FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		34	ns
			QPL4C381-35		28	ns
Clock (OS_A,OS_B=0) to OVF, ZERO	42	FTAB=0 FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		50	ns
			QPL4C381-35		34	ns
Clock (OS_A,OS_B=0) to C_{16}	43	FTAB=0 FTF=0, C_L=30pF, V_{CC}=4.5V	QPL4C381-45		34	ns
			QPL4C381-35		28	ns
A_0-A_{15}, B_0-B_{15} Setup Time	44	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	8		ns
			QPL4C381-35	8		ns
A_0-A_{15}, B_0-B_{15} Hold Time	45	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	3		ns
			QPL4C381-35	3		ns
A_0-A_{15}, B_0-B_{15} Setup Time	46	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	33		ns
			QPL4C381-35	20		ns
A_0-A_{15}, B_0-B_{15} Hold Time	47	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	3		ns
			QPL4C381-35	3		ns
$\overline{EN}_A$, $\overline{EN}_B$ Setup Time	48	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	10		ns
			QPL4C381-35	10		ns
$\overline{EN}_A$, $\overline{EN}_B$ Hold Time	49	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	2		ns
			QPL4C381-35	2		ns
$\overline{ENF}$ Setup Time	50	C_L=30pF, V_{CC}=4.5V	QPL4C381-45	10		ns
			QPL4C381-35	10		ns
$\overline{ENF}$ Hold Time	51	C_L=30pF, V_{CC}=4.5V	QPL4C381-45	2		ns
			QPL4C381-35	2		ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
C_0 Setup Time	52	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	20		ns
			QPL4C381-35	12		ns
C_0 Hold Time	53	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	0		ns
			QPL4C381-35	0		ns
C_0 Setup Time	54	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	20		ns
			QPL4C381-35	12		ns
C_0 Hold Time	55	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	0		ns
			QPL4C381-35	0		ns
S_0-S_2,OS_A,OS_B Setup Time	56	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	36		ns
			QPL4C381-35	20		ns
S_0-S_2,OS_A,OS_B Hold Time	57	FTAB=0 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	0		ns
			QPL4C381-35	0		ns
S_0-S_2,OS_A,OS_B Setup Time	58	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	36		ns
			QPL4C381-35	20		ns
S_0-S_2,OS_A,OS_B Hold Time	59	FTAB=1 C_L=30pF, V_{CC}=4.5V	QPL4C381-45	0		ns
			QPL4C381-35	0		ns
Minimum Cycle Time	60	C_L=30pF, V_{CC}=4.5V	QPL4C381-45	38		ns
			QPL4C381-35	26		ns
High Going Pulse	61	C_L=30pF, V_{CC}=4.5V	QPL4C381-45	15		ns
			QPL4C381-35	12		ns
Low Going Pulse	62	C_L=30pF, V_{CC}=4.5V	QPL4C381-45	15		ns
			QPL4C381-35	12		ns
Tri-State Enable Time	63	C_L=30pF, V_{CC}=4.5V	QPL4C381-45		20	ns
			QPL4C381-35		18	ns
Tri-State Disable Time	64	C_L=30pF, V_{CC}=4.5V /7	QPL4C381-45		20	ns
			QPL4C381-35		18	ns

NOTES

3/ Test Conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OH}, I_{OL} and 30pF. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required device input levels relative to device supply pins. All tests must be performed using worst-case test conditions, unless otherwise specified.

4/ For test purposes, not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. Guaranteed if not tested.

5/ Tested with all outputs changing every cycle and no load at a 5MHz clock rate.

6/ Tested with all inputs within 0.1V of V_{CC} or GND, no load.

7/ Tested with I_{OL} = 10mA, I_{OH} = 10mA.

8/ Tested only for initial qualification and after process or design changes which may effect capacitance.

Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
QPL4C381KMB45-MIL (Similar to: 5962-8995901YA)	CQCC1-N68	QPL4C381KMB45
QPL4C381GMB45-MIL (Similar to: 5962-8995901ZC)	CMGA3-P68	QPL4C381GMB45
QPL4C381KMB30-MIL (Similar to: 5962-8995902YA)	CQCC1-N68	QPL4C381KMB30
QPL4C381GMB30-MIL (Similar to: 5962-8995902ZA)	CMGA3-P68	QPL4C381GMB30

QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

"-MIL" products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com