# Ruggedization levels

<table>
<thead>
<tr>
<th>Airflow Type</th>
<th>Operating Temperature</th>
<th>Non-Operating Temperature</th>
<th>Operating Shock</th>
<th>Relative Humidity</th>
<th>Altitude</th>
<th>Conformal Coating</th>
<th>Conduction Standard</th>
<th>Conduction Rugged</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS (VITA 47 ECC4)</td>
<td>0°C to +55°C (1)</td>
<td>-30°C to +100°C</td>
<td>20g, 11 ms half-sine</td>
<td>0% to 95%</td>
<td>@ 0 to 30,000 ft</td>
<td>No</td>
<td>Conduction Standard</td>
<td>Conduction Rugged</td>
</tr>
<tr>
<td>AR (VITA 47 ECC6)</td>
<td>-40°C to +70°C (1)</td>
<td>-50°C to +100°C</td>
<td>20g, 11 ms half-sine</td>
<td>0% to 95%</td>
<td>@ 0 to 30,000 ft</td>
<td>No</td>
<td>Conduction Standard</td>
<td>Conduction Rugged</td>
</tr>
<tr>
<td>CS (VITA 47 ECC3)</td>
<td>-40°C to +70°C</td>
<td>-50°C to +100°C</td>
<td>40g, 11 ms half-sine</td>
<td>0% to 95%</td>
<td>@ 0 to 30,000 ft</td>
<td>Optional acrylic 1B73</td>
<td>Conduction Standard</td>
<td>Conduction Rugged</td>
</tr>
<tr>
<td>CR (VITA 47 ECC4)</td>
<td>-40°C to +85°C</td>
<td>-55°C to +105°C</td>
<td>40g, 11 ms half-sine</td>
<td>0% to 95%</td>
<td>@ 0 to 60,000 ft</td>
<td>Yes</td>
<td>Conduction Standard</td>
<td>Conduction Rugged</td>
</tr>
</tbody>
</table>

Specifications are subject to change without notice. All trademarks are the property of their respective owners. Copyright © 2011-2014. All rights reserved.

**High speed data conversion & signal processing solutions**

**3U VPX, Virtex 7 FPGA**

Single QSFP+ interfaces

conduction or air-cooled

**Features**

- One QSFP (Quad Small Form-Factor Pluggable) interface
- Supports QSFP copper or optical transceivers up to 10 Gbps/lane
- On-board low jitter reference clock generator
- User programmable Xilinx® Virtex® 7 VX690T or VX980T FPGA
- Two banks 667 MHz 256M64 DDR3 SDRAM
- 3U OpenVPX standard compliant
- Air-cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

**Applications**

- Real-time processing
- Wideband data communication
- Data storage interface

Contact us online at:
e2v-us.com

Phone: +1 408 737 0992
Fax: +1 408 736 8708

Specifications are subject to change without notice. All trademarks are the property of their respective owners. Copyright © 2011-2014. All rights reserved.

AV112

Wideband communication
The AV112 is part of Xilinx’s range of high speed data conversion and signal processing solutions based on the ANSI/VITA 65, OpenVPX standard.

The AV112 is fully compliant with the OpenVPX standard, with default support for the MOD3-RAY-3F2UL-62.2.1.3 and MOD3-RAY-3F2UL-62.2.4 module profiles, PCIe Gen 1 or Gen 2 on data planes and expansion plane plus 100BASE-BX on control planes.

The AV112 combines the very high processing power delivered by Xilinx Virtex 7 FPGA with one QSFP (Quad Small Form-Factor Pluggable) interface, making it ideally suited for embedded signal processing applications for data communication and data storage interface with support for data rate at up to 10 Gbps per link.

The AV112 provides one on board, user programmable, low jitter clock generator supporting reference clocks as required for PCIe, SATA, SRIO, Fiber Channel, Aurora, Gigabit Ethernet or XAUI protocols.

The AV112 includes one Xilinx Virtex 7 FPGA VX690T or VX980T for an impressive processing capability of up to more than 2 TMACS (Multiply Accumulate per second), two banks 667 MHz 256M64 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.

The AV112 features a 32-bit microcontroller with USB 2.0 and 10/100 Ethernet interfaces intended to be used for system monitoring and supervision.

The AV112 comes with complete software drivers for Windows and Linux. An FPGA firmware package is provided including all cores necessary to build user FPGA applications.

Overview

High speed data conversion & signal processing solutions

Quad Small Form-Factor Pluggable Transceiver

The AV112 supports one Quad Small Form Factor Pluggable (QSFP) transceivers.

The AV112 supports optical QSFP transceivers for communication at up to 40 Gbps over distances up to 10 km.

The AV112 supports copper QSFP transceivers for communication at up to 40 Gbps over distances up to a few meters.

Clocks

The AV112 provides one onboard, user programmable, low jitter clock synthesizers generating as required for the high speed serial links (Xilinx Virtex 7 G70).

The clock frequency can be selected among the following:

- 62.5 MHz, supporting GigE
- 75 MHz and 150 MHz, supporting SATA
- 100 MHz, supporting PCIe gen 1
- 106.25 MHz, supporting Serial PCIe and Fibre Channel
- 125 MHz, supporting PCIe gen 2, GigE, Aurora and SRIO - 2.5 and 5 Gbps
- 156.25 MHz, supporting XAUI, SRIO and Aurora - 13.75 Gbps
- 195.375 MHz, supporting 10 G Fibre Channel
- 200 MHz and 250 MHz, supporting PCIe gen 2
- 212.5 MHz, supporting 4 G Fibre Channel
- 312.5 MHz, supporting Aurora 3, and 6.25 Gbps and XGMI
- 625 MHz, supporting 10 G GigE

FPGA

The AV112 is fitted with a Xilinx Virtex 7 VX690T or VX980T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR1 SDRAM and monitoring subsystem, leaving most of the logic and block RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 7 VX690T FPGA includes 693,120,000 logic cells, 4,700 block RAM (18 Kbit each), 5,600 DSP48E1 slices and 3 PCIe interface blocks.

The most powerful version embeds a Xilinx Virtex 7 VX980T which provides 972,200 logic cells, 5,500 block RAM, 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACS.

The VX690T is delivered in 2 speed grades while the VX980T is delivered in 3 speed grades.

Memory

The AV112 includes two 667 MHz 256M64 DDR3 SDRAM memory banks (500 MHz for 980T) and one 1 Gb NOR FLASH memory used to store multiple FPGA configuration files.

VPX interface

The AV112 features an OpenVPX VITA 65 compliant interface with support for two fat pipes for data plane, one fat pipe for expansion plane, two ultra thin pipes for control plane and two user defined ultra thin pipes on Ps.

The VPX interface supports USB 2.0, a 10/100 Ethernet and 28 LVDS differential pairs on P2.

Software support

Software drivers:

- Windows 7
- Linux

Ruggedization

As per VITA 47:

- Air-cooled: EAC4 and EAC6
- Conduction cooled: ECC1 and ECC4

Power dissipation (980T)

- +12V: 6.4 A max (+6.7W)
- +5V: 0.4 A max (+9.8W)
- +3.3V 1.5 A max (+5.1W)
- -3.3V: 0.3 A max (+1.8W)

Weight

Air-cooled: 600g

Conduction cooled: 640g

Specifications

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Xilinx Virtex 7</th>
<th>XC7VX690T-2FFG1930 or</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>2 banks 256M64 DDR3 SDRAM, 667 MHz 500 MHz (980T) clock</td>
<td>One 1 Gb NOR FLASH memory</td>
</tr>
<tr>
<td>VPX Interface</td>
<td>- Data plane: two fat pipes</td>
<td>- Expansion plane: one fat pipe</td>
</tr>
<tr>
<td>- Control plane: two ultra thin pipes</td>
<td>- 28 LVDS differential pairs</td>
<td></td>
</tr>
</tbody>
</table>

Software support

Software drivers:

- Windows 7
- Linux

Application example:

- Windows and Linux

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>FPGA Virtex 7 VX690T-2F</th>
<th>FPGA Virtex 7 VX980T-2F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Options 1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Firmware support

VHD cores for all hardware resources

Base Design

Supported by Xilinx VIVADO 2012.4 and later

Ruggedization

As per VITA 47:

- Air-cooled: EAC4 and EAC6
- Conduction cooled: ECC1 and ECC4

Power dissipation (980T)

- +12V: 6.4 A max (+6.7W)
- +5V: 0.4 A max (+9.8W)
- +3.3V: 1.5 A max (+5.1W)
- -3.3V: 0.3 A max (+1.8W)

Weight

Air-cooled: 600g

Conduction cooled: 640g