

## FEATURES

- 4 e6500 cores built on Power Architecture® technology sharing a 2 MB L2 cache
- 512 KB CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and noncoherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - Queue Manager (QMan) fabric supporting packetlevel queue management and quality of service scheduling
- One 32-/64-bit DDR3 SDRAM memory controller
  - DDR3 and DDR3L with ECC and interleaving support
  - Memory pre-fetch engine
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (Frame Manager 1.1)
  - Queue management for scheduling, packet sequencing, and congestion management (Queue Manager 1.1)
  - Hardware buffer management for buffer allocation and de-allocation (Buffer Manager 1.1)
  - Cryptography Acceleration (SEC 5.2)
  - RegEx Pattern Matching Acceleration (PME 2.1)
  - Decompression/Compression Acceleration (DCE 1.0)
  - DPAA chip-to-chip interconnect via RapidIO Message Manager (RMan 1.0)
- 16 SerDes lanes at up to 10 GBaud
- 8 Ethernet interfaces, supporting combinations of:
  - Up to four 10 Gbps Ethernet MACs
  - Up to eight 1 Gbps Ethernet MACs
  - Up to four 2.5Gbps Ethernet MACs
  - IEEE Std 1588. support
- High-speed peripheral interfaces
  - Four PCI Express controllers (two support PCIe 2.0 and two support PCIe 3.0)
  - Two Serial RapidIO 2.0 controllers running at up to 5 GBaud with Type 11 messaging and Type 9 data streaming support
- Additional peripheral interfaces
  - Two Serial ATA (SATA 2.0) controllers
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller (SD/MMC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Four 2-pin UARTs or two 4-pin UARTs
  - Integrated flash controller supporting NAND and NOR flash
- Three 8-channel DMA engines
- 896 FC-PBGA package, 25 mm × 25 mm, 0.8mm pitch

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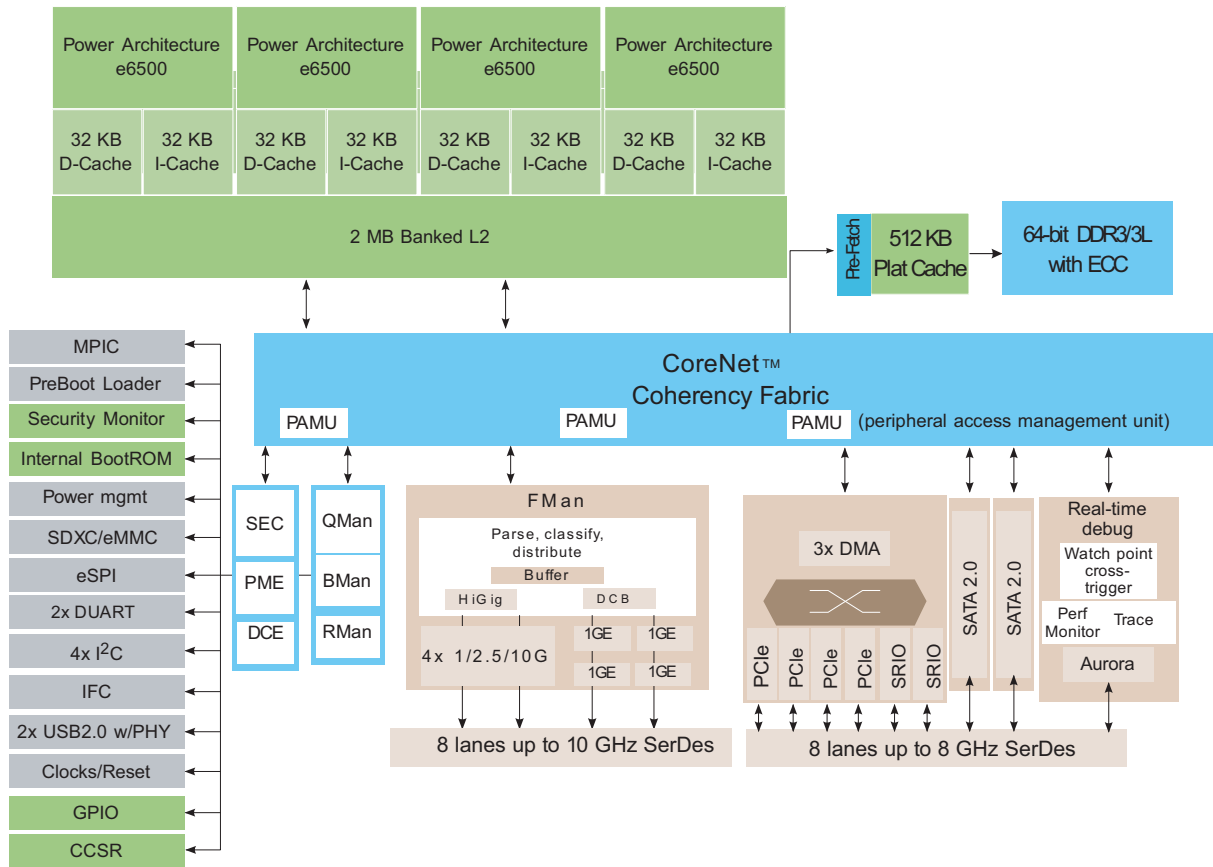
1. OVERVIEW

The T2080 QorIQ integrated multicore communications processor combines 4 dualthreaded cores built on Power Architecture® technology with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying board design.

This figure shows the block diagram of the chip.

Figure 1-1. Block diagram



2. PIN ASSIGNMENTS

2.1 896 ball layout diagrams

This figure shows the complete view of the T2080 ball map diagram. [Figure 2-2](#), [Figure 2-3](#), [Figure 2-4](#), and [Figure 2-5](#) show quadrant views.

Figure 2-1. Complete BGA Map for the T2080

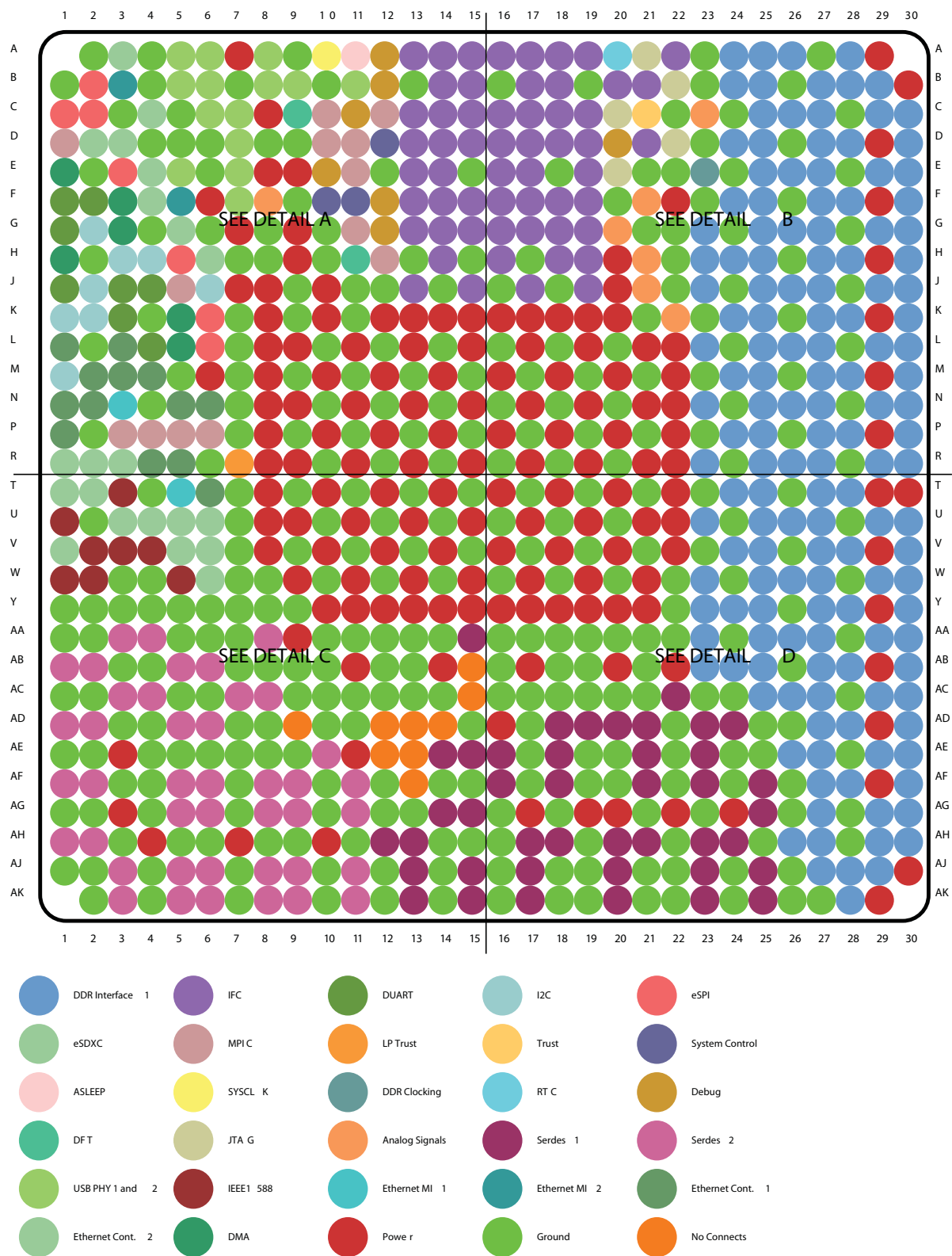


Figure 2-2. Detail A

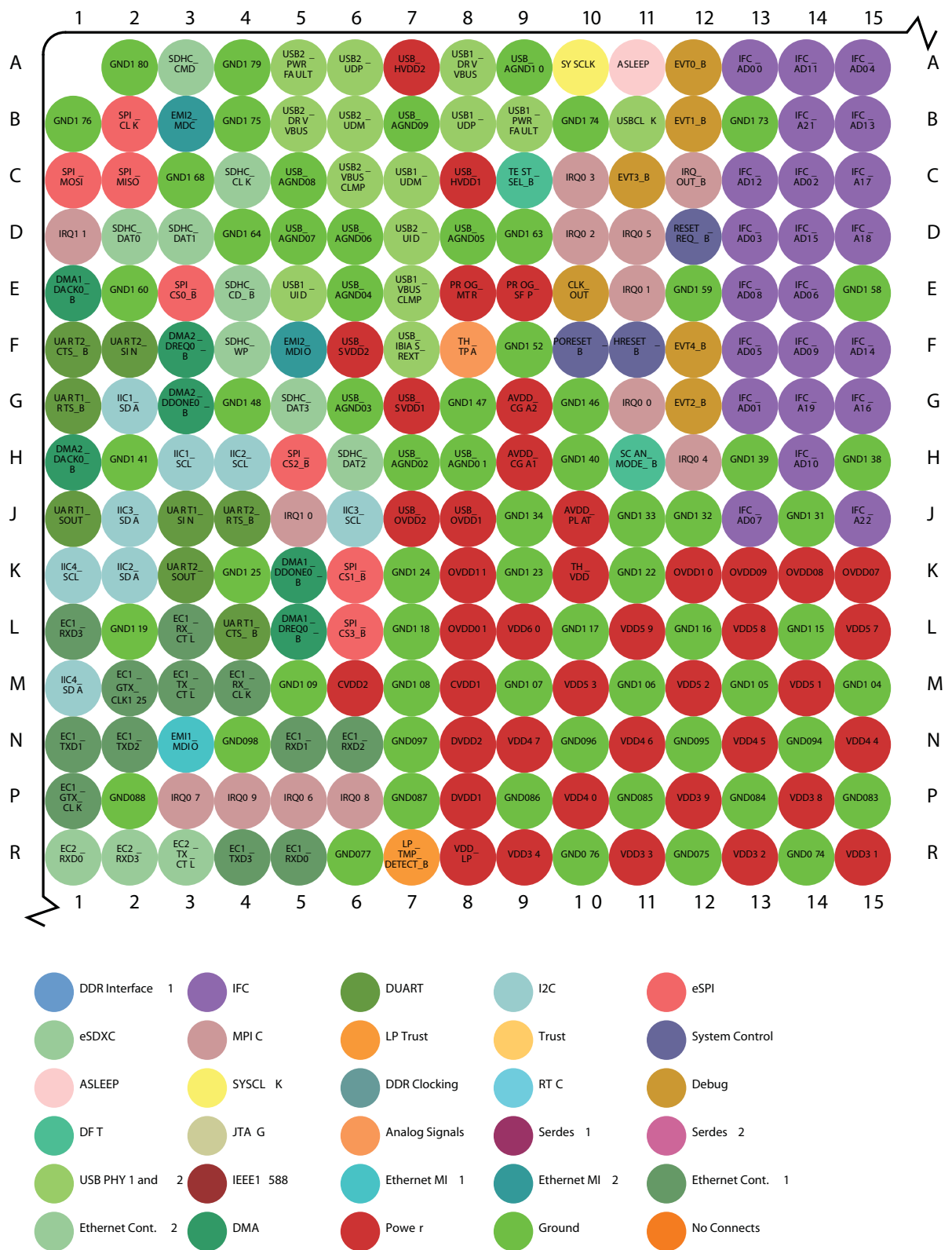


Figure 2-3. Detail B

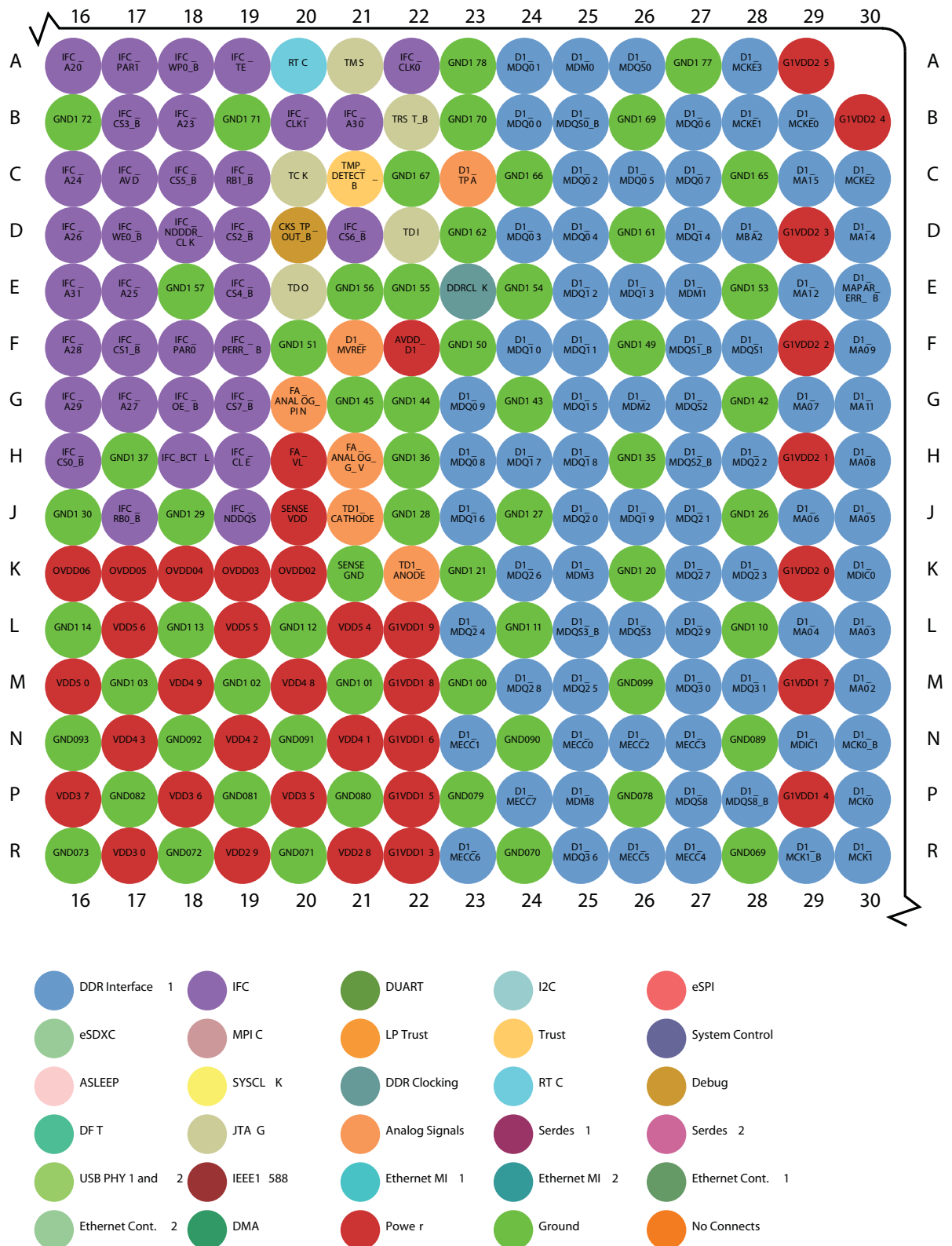


Figure 2-4. Detail C

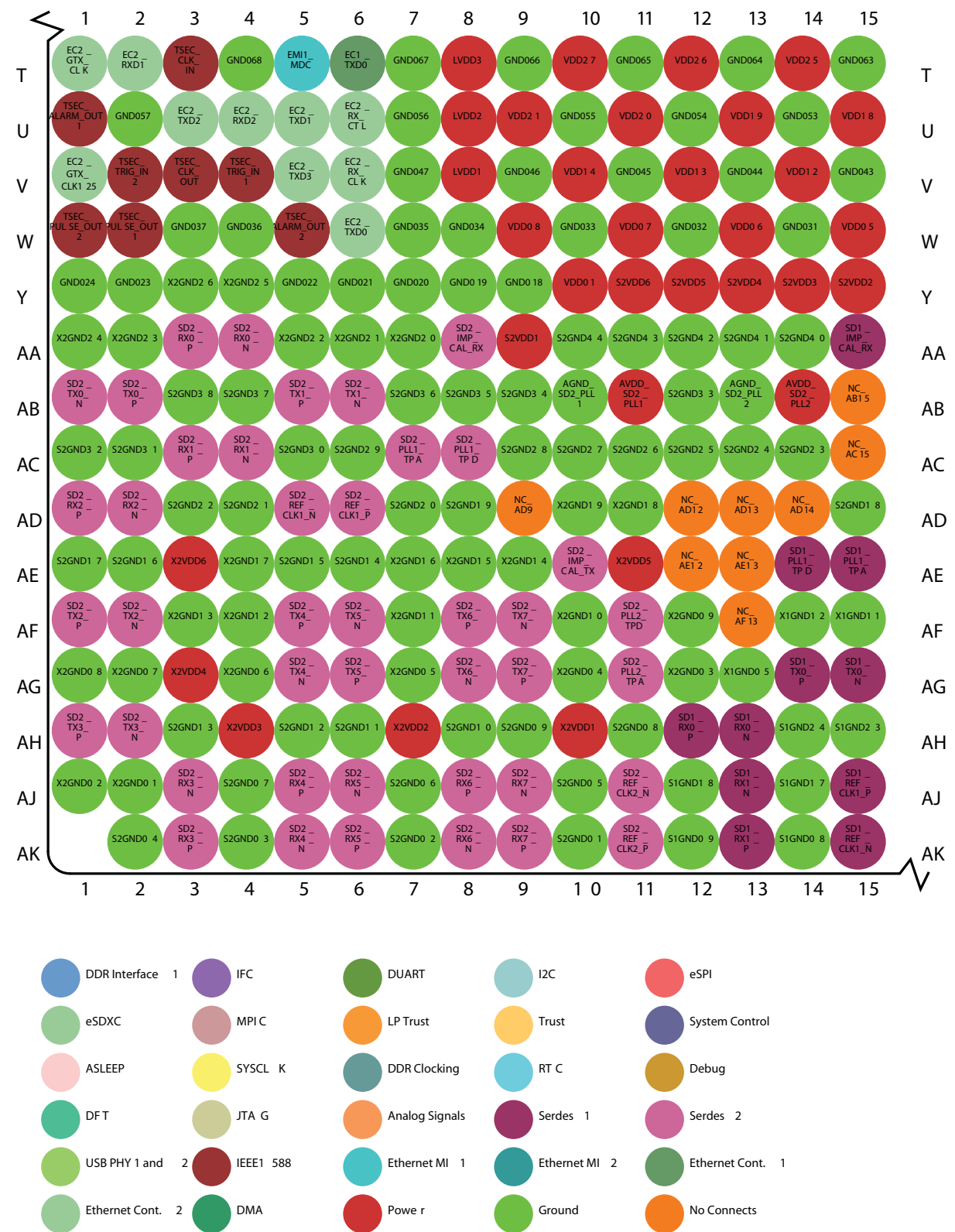
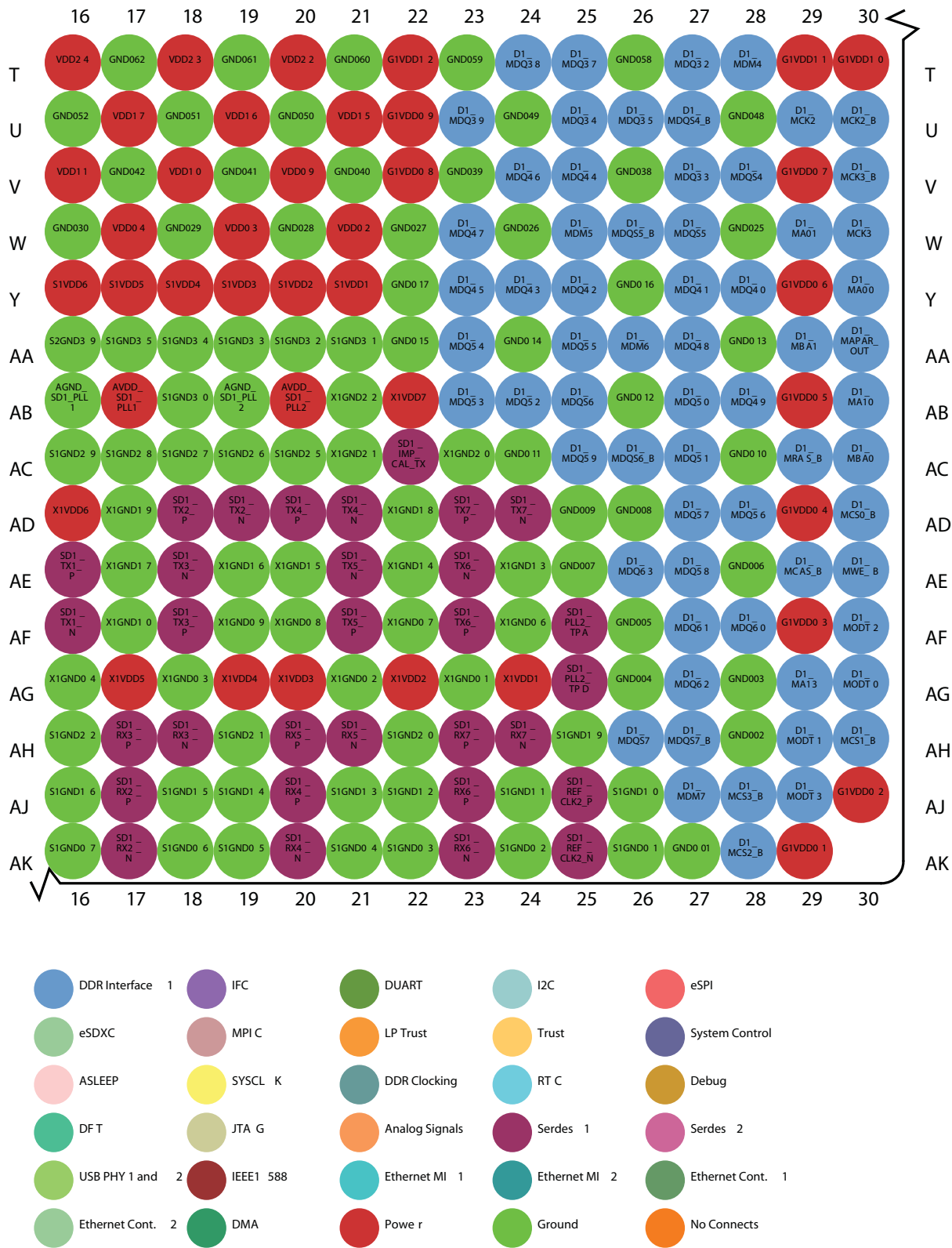


Figure 2-5. Detail D





## 2.2 Pinout list

This table provides the pinout listing for the T2080 by bus. Primary functions are **bolded** in the table.

**Table 2-1.** Pinout list by bus

| Signal                              | Signal description    | Package pin number | Pin type | Power supply      | Notes  |
|-------------------------------------|-----------------------|--------------------|----------|-------------------|--------|
| <b>DDR SDRAM Memory Interface 1</b> |                       |                    |          |                   |        |
| <b>D1_MA00</b>                      | Address               | Y30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA01</b>                      | Address               | W29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA02</b>                      | Address               | M30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA03</b>                      | Address               | L30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA04</b>                      | Address               | L29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA05</b>                      | Address               | J30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA06</b>                      | Address               | J29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA07</b>                      | Address               | G29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA08</b>                      | Address               | H30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA09</b>                      | Address               | F30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA10</b>                      | Address               | AB30               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA11</b>                      | Address               | G30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA12</b>                      | Address               | E29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA13</b>                      | Address               | AG29               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA14</b>                      | Address               | D30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MA15</b>                      | Address               | C29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MAPAR_ERR_B</b>               | Address Parity Error  | E30                | I        | G1V <sub>DD</sub> | (1)(6) |
| <b>D1_MAPAR_OUT</b>                 | Address Parity Out    | AA30               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MBA0</b>                      | Bank Select           | AC30               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MBA1</b>                      | Bank Select           | AA29               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MBA2</b>                      | Bank Select           | D28                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCAS_B</b>                    | Column Address Strobe | AE29               | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK0</b>                      | Clock                 | P30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK0_B</b>                    | Clock Complement      | N30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK1</b>                      | Clock                 | R30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK1_B</b>                    | Clock Complement      | R29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK2</b>                      | Clock                 | U29                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK2_B</b>                    | Clock Complement      | U30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK3</b>                      | Clock                 | W30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCK3_B</b>                    | Clock Complement      | V30                | O        | G1V <sub>DD</sub> | –      |
| <b>D1_MCKE0</b>                     | Clock Enable          | B29                | O        | G1V <sub>DD</sub> | (2)    |
| <b>D1_MCKE1</b>                     | Clock Enable          | B28                | O        | G1V <sub>DD</sub> | (2)    |
| <b>D1_MCKE2</b>                     | Clock Enable          | C30                | O        | G1V <sub>DD</sub> | (2)    |
| <b>D1_MCKE3</b>                     | Clock Enable          | A28                | O        | G1V <sub>DD</sub> | (2)    |



Table 2-1. Pinout list by bus (Continued)

| Signal    | Signal description           | Package pin number | Pin type | Power supply      | Notes |
|-----------|------------------------------|--------------------|----------|-------------------|-------|
| D1_MCS0_B | Chip Select                  | AD30               | O        | G1V <sub>DD</sub> | —     |
| D1_MCS1_B | Chip Select                  | AH30               | O        | G1V <sub>DD</sub> | —     |
| D1_MCS2_B | Chip Select                  | AK28               | O        | G1V <sub>DD</sub> | —     |
| D1_MCS3_B | Chip Select                  | AJ28               | O        | G1V <sub>DD</sub> | —     |
| D1_MDIC0  | Driver Impedance Calibration | K30                | IO       | G1V <sub>DD</sub> | (3)   |
| D1_MDIC1  | Driver Impedance Calibration | N29                | IO       | G1V <sub>DD</sub> | (3)   |
| D1_MDM0   | Data Mask                    | A25                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM1   | Data Mask                    | E27                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM2   | Data Mask                    | G26                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM3   | Data Mask                    | K25                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM4   | Data Mask                    | T28                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM5   | Data Mask                    | W25                | O        | G1V <sub>DD</sub> | —     |
| D1_MDM6   | Data Mask                    | AA26               | O        | G1V <sub>DD</sub> | —     |
| D1_MDM7   | Data Mask                    | AJ27               | O        | G1V <sub>DD</sub> | —     |
| D1_MDM8   | Data Mask                    | P25                | O        | G1V <sub>DD</sub> | —     |
| D1_MDQ00  | Data                         | B24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ01  | Data                         | A24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ02  | Data                         | C25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ03  | Data                         | D24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ04  | Data                         | D25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ05  | Data                         | C26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ06  | Data                         | B27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ07  | Data                         | C27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ08  | Data                         | H23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ09  | Data                         | G23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ10  | Data                         | F24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ11  | Data                         | F25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ12  | Data                         | E25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ13  | Data                         | E26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ14  | Data                         | D27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ15  | Data                         | G25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ16  | Data                         | J23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ17  | Data                         | H24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ18  | Data                         | H25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ19  | Data                         | J26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ20  | Data                         | J25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ21  | Data                         | J27                | IO       | G1V <sub>DD</sub> | —     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal   | Signal description | Package pin number | Pin type | Power supply      | Notes |
|----------|--------------------|--------------------|----------|-------------------|-------|
| D1_MDQ22 | Data               | H28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ23 | Data               | K28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ24 | Data               | L23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ25 | Data               | M25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ26 | Data               | K24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ27 | Data               | K27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ28 | Data               | M24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ29 | Data               | L27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ30 | Data               | M27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ31 | Data               | M28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ32 | Data               | T27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ33 | Data               | V27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ34 | Data               | U25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ35 | Data               | U26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ36 | Data               | R25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ37 | Data               | T25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ38 | Data               | T24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ39 | Data               | U23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ40 | Data               | Y28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ41 | Data               | Y27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ42 | Data               | Y25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ43 | Data               | Y24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ44 | Data               | V25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ45 | Data               | Y23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ46 | Data               | V24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ47 | Data               | W23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ48 | Data               | AA27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ49 | Data               | AB28               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ50 | Data               | AB27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ51 | Data               | AC27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ52 | Data               | AB24               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ53 | Data               | AB23               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ54 | Data               | AA23               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ55 | Data               | AA25               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ56 | Data               | AD28               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ57 | Data               | AD27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ58 | Data               | AE27               | IO       | G1V <sub>DD</sub> | —     |

Table 2-1. Pinout list by bus (Continued)

| Signal     | Signal description    | Package pin number | Pin type | Power supply      | Notes |
|------------|-----------------------|--------------------|----------|-------------------|-------|
| D1_MDQ59   | Data                  | AC25               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ60   | Data                  | AF28               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ61   | Data                  | AF27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ62   | Data                  | AG27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQ63   | Data                  | AE26               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS0   | Data Strobe           | A26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS0_B | Data Strobe           | B25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS1   | Data Strobe           | F28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS1_B | Data Strobe           | F27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS2   | Data Strobe           | G27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS2_B | Data Strobe           | H27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS3   | Data Strobe           | L26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS3_B | Data Strobe           | L25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS4   | Data Strobe           | V28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS4_B | Data Strobe           | U27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS5   | Data Strobe           | W27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS5_B | Data Strobe           | W26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS6   | Data Strobe           | AB25               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS6_B | Data Strobe           | AC26               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS7   | Data Strobe           | AH26               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS7_B | Data Strobe           | AH27               | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS8   | Data Strobe           | P27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MDQS8_B | Data Strobe           | P28                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC0   | Error Correcting Code | N25                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC1   | Error Correcting Code | N23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC2   | Error Correcting Code | N26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC3   | Error Correcting Code | N27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC4   | Error Correcting Code | R27                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC5   | Error Correcting Code | R26                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC6   | Error Correcting Code | R23                | IO       | G1V <sub>DD</sub> | —     |
| D1_MECC7   | Error Correcting Code | P24                | IO       | G1V <sub>DD</sub> | —     |
| D1_MODT0   | On Die Termination    | AG30               | O        | G1V <sub>DD</sub> | (2)   |
| D1_MODT1   | On Die Termination    | AH29               | O        | G1V <sub>DD</sub> | (2)   |
| D1_MODT2   | On Die Termination    | AF30               | O        | G1V <sub>DD</sub> | (2)   |
| D1_MODT3   | On Die Termination    | AJ29               | O        | G1V <sub>DD</sub> | (2)   |
| D1_MRAS_B  | Row Address Strobe    | AC29               | O        | G1V <sub>DD</sub> | —     |
| D1_MWE_B   | Write Enable          | AE30               | O        | G1V <sub>DD</sub> | —     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal                             | Signal description                      | Package pin number | Pin type | Power supply     | Notes  |
|------------------------------------|---|--------------------|----------|------------------|--------|
| <b>Integrated Flash Controller</b> |   |                    |          |                  |        |
| IFC_A16                            | IFC Address                             | G15                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_A17                            | IFC Address                             | C15                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_A18                            | IFC Address                             | D15                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_A19                            | IFC Address                             | G14                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_A20                            | IFC Address                             | A16                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_A21/cfg_dram_type              | IFC Address                             | B14                | O        | OV <sub>DD</sub> | (1)(4) |
| IFC_A22                            | IFC Address                             | J15                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A23                            | IFC Address                             | B18                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A24                            | IFC Address                             | C16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A25/GPIO2_25/IFC_WP1_B         | IFC Address                             | E17                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A26/GPIO2_26/IFC_WP2_B         | IFC Address                             | D16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A27/GPIO2_27/IFC_WP3_B         | IFC Address                             | G17                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A28/GPIO2_28                   | IFC Address                             | F16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A29/GPIO2_29/IFC_RB2_B         | IFC Address                             | G16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A30/GPIO2_30/IFC_RB3_B         | IFC Address                             | B21                | O        | OV <sub>DD</sub> | (1)    |
| IFC_A31/GPIO2_31/IFC_RB4_B         | IFC Address                             | E16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_AD00/cfg_gpinout0              | IFC Address / Data                      | A13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD01/cfg_gpinout1              | IFC Address / Data                      | G13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD02/cfg_gpinout2              | IFC Address / Data                      | C14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD03/cfg_gpinout3              | IFC Address / Data                      | D13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD04/cfg_gpinout4              | IFC Address / Data                      | A15                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD05/cfg_gpinout5              | IFC Address / Data                      | F13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD06/cfg_gpinout6              | IFC Address / Data                      | E14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD07/cfg_gpinout7              | IFC Address / Data                      | J13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD08/cfg_rcw_src0              | IFC Address / Data                      | E13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD09/cfg_rcw_src1              | IFC Address / Data                      | F14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD10/cfg_rcw_src2              | IFC Address / Data                      | H14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD11/cfg_rcw_src3              | IFC Address / Data                      | A14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD12/cfg_rcw_src4              | IFC Address / Data                      | C13                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD13/cfg_rcw_src5              | IFC Address / Data                      | B15                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD14/cfg_rcw_src6              | IFC Address / Data                      | F15                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AD15/cfg_rcw_src7              | IFC Address / Data                      | D14                | IO       | OV <sub>DD</sub> | (4)    |
| IFC_AVD                            | IFC Address Valid                       | C17                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_BCTL                           | IFC Buffer control                      | H18                | O        | OV <sub>DD</sub> | (2)    |
| IFC_CLE/cfg_rcw_src8               | IFC Command Latch Enable / Write Enable | H19                | O        | OV <sub>DD</sub> | (1)(4) |
| IFC_CLK0                           | IFC Clock                               | A22                | O        | OV <sub>DD</sub> | (2)    |

Table 2-1. Pinout list by bus (Continued)

| Signal                          | Signal description              | Package pin number | Pin type | Power supply     | Notes  |
|---------------------------------|---------------------------------|--------------------|----------|------------------|--------|
| IFC_CLK1                        | IFC Clock                       | B20                | O        | OV <sub>DD</sub> | (2)    |
| IFC_CS0_B                       | IFC Chip Select                 | H16                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS1_B/GPIO2_10              | IFC Chip Select                 | F17                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS2_B/GPIO2_11              | IFC Chip Select                 | D19                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS3_B/GPIO2_12              | IFC Chip Select                 | B17                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS4_B/GPIO1_09              | IFC Chip Select                 | E19                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS5_B/GPIO1_10              | IFC Chip Select                 | C18                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS6_B/GPIO1_11              | IFC Chip Select                 | D21                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_CS7_B/GPIO1_12              | IFC Chip Select                 | G19                | O        | OV <sub>DD</sub> | (1)(6) |
| IFC_NDDDR_CLK                   | IFC NAND DDR Clock              | D18                | O        | OV <sub>DD</sub> | (2)    |
| IFC_NDDQS                       | IFC DQS Strobe                  | J19                | IO       | OV <sub>DD</sub> | —      |
| IFC_OE_B                        | IFC Output Enable               | G18                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_PAR0/GPIO2_13               | IFC Address & Data Parity       | F18                | IO       | OV <sub>DD</sub> | —      |
| IFC_PAR1/GPIO2_14               | IFC Address & Data Parity       | A17                | IO       | OV <sub>DD</sub> | —      |
| IFC_PERR_B/GPIO2_15             | IFC Parity Error                | F19                | I        | OV <sub>DD</sub> | (1)    |
| IFC_RB0_B                       | IFC Ready / Busy CS0            | J17                | I        | OV <sub>DD</sub> | (8)    |
| IFC_RB1_B                       | IFC Ready / Busy CS1            | C19                | I        | OV <sub>DD</sub> | (8)    |
| IFC_RB2_B/IFC_A29/GPIO2_29      | IFC Ready / Busy CS 2           | G16                | I        | OV <sub>DD</sub> | (1)    |
| IFC_RB3_B/IFC_A30/GPIO2_30      | IFC Ready / Busy CS 3           | B21                | I        | OV <sub>DD</sub> | (1)    |
| IFC_RB4_B/IFC_A31/GPIO2_31      | IFC Ready / Busy CS 4           | E16                | I        | OV <sub>DD</sub> | (1)    |
| IFC_TE/cfg_ifc_te               | IFC External Transceiver Enable | A19                | O        | OV <sub>DD</sub> | (1)(4) |
| IFC_WE0_B                       | IFC Write Enable                | D17                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_WP0_B                       | IFC Write Protect               | A18                | O        | OV <sub>DD</sub> | (1)(5) |
| IFC_WP1_B/IFC_A25/GPIO2_25      | IFC Write Protect               | E17                | O        | OV <sub>DD</sub> | (1)    |
| IFC_WP2_B/IFC_A26/GPIO2_26      | IFC Write Protect               | D16                | O        | OV <sub>DD</sub> | (1)    |
| IFC_WP3_B/IFC_A27/GPIO2_27      | IFC Write Protect               | G17                | O        | OV <sub>DD</sub> | (1)    |
| DUART                           |                                 |                    |          |                  |        |
| UART1_CTS_B/GPIO1_21/UART3_SIN  | Clear To Send                   | L4                 | I        | DV <sub>DD</sub> | (1)    |
| UART1_RTS_B/GPIO1_19/UART3_SOUT | Ready to Send                   | G1                 | O        | DV <sub>DD</sub> | (1)    |
| UART1_SIN/GPIO1_17              | Receive Data                    | J3                 | I        | DV <sub>DD</sub> | (1)    |
| UART1_SOUT/GPIO1_15             | Transmit Data                   | J1                 | O        | DV <sub>DD</sub> | (1)    |
| UART2_CTS_B/GPIO1_22/UART4_SIN  | Clear To Send                   | F1                 | I        | DV <sub>DD</sub> | (1)    |
| UART2_RTS_B/GPIO1_20/UART4_SOUT | Ready to Send                   | J4                 | O        | DV <sub>DD</sub> | (1)    |
| UART2_SIN/GPIO1_18              | Receive Data                    | F2                 | I        | DV <sub>DD</sub> | (1)    |
| UART2_SOUT/GPIO1_16             | Transmit Data                   | K3                 | O        | DV <sub>DD</sub> | (1)    |
| UART3_SIN/UART1_CTS_B/GPIO1_21  | Receive Data                    | L4                 | I        | DV <sub>DD</sub> | (1)    |

**Table 2-1.** Pinout list by bus (Continued)

| Signal   | Signal description          | Package pin number | Pin type | Power supply     | Notes   |
|--|-----------------------------|--------------------|----------|------------------|---------|
| UART3_SOUT/<br>UART1_RTS_B/GPIO1_19                | Transmit Data               | G1                 | O        | DV <sub>DD</sub> | (1)     |
| UART4_SIN/UART2_CTS_B/GPIO1_22                     | Receive Data                | F1                 | I        | DV <sub>DD</sub> | (1)     |
| UART4_SOUT/<br>UART2_RTS_B/GPIO1_20                | Transmit Data               | J4                 | O        | DV <sub>DD</sub> | (1)     |
| <b>I2C</b>   |                             |                    |          |                  |         |
| IIC1_SCL   | Serial Clock (supports PBL) | H3                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC1_SDA   | Serial Data (supports PBL)  | G2                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC2_SCL   | Serial Clock                | H4                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC2_SDA   | Serial Data                 | K2                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC3_SCL/GPIO4_00                                  | Serial Clock                | J6                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC3_SDA/GPIO4_01                                  | Serial Data                 | J2                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC4_SCL/GPIO4_02/EVT5_B                           | Serial Clock                | K1                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| IIC4_SDA/GPIO4_03/EVT6_B                           | Serial Data                 | M1                 | IO       | DV <sub>DD</sub> | (7)(8)  |
| <b>eSPI Interface</b>                              |                             |                    |          |                  |         |
| SPI_CLK  | SPI Clock                   | B2                 | O        | CV <sub>DD</sub> | (1)     |
| SPI_CS0_B/GPIO2_00/SDHC_DAT4                       | SPI Chip Select             | E3                 | O        | CV <sub>DD</sub> | (1)(18) |
| SPI_CS1_B/GPIO2_01/SDHC_DAT5                       | SPI Chip Select             | K6                 | O        | CV <sub>DD</sub> | (1)(18) |
| SPI_CS2_B/GPIO2_02/SDHC_DAT6                       | SPI Chip Select             | H5                 | O        | CV <sub>DD</sub> | (1)(18) |
| SPI_CS3_B/GPIO2_03/SDHC_DAT7/<br>SDHC_CLK_SYNC_OUT | SPI Chip Select             | L6                 | O        | CV <sub>DD</sub> | (1)(18) |
| SPI_MISO   | Master In Slave Out         | C2                 | I        | CV <sub>DD</sub> | (1)     |
| SPI_MOSI   | Master Out Slave In         | C1                 | IO       | CV <sub>DD</sub> | —       |
| <b>eSDHC</b>                                       |                             |                    |          |                  |         |
| SDHC_CD_B/GPIO4_24                                 | SDHC Card Detect            | E4                 | I        | OV <sub>DD</sub> | (1)     |
| SDHC_CLK/GPIO2_09                                  | Host to Card Clock          | C4                 | IO       | OV <sub>DD</sub> | —       |
| SDHC_CLK_SYNC_IN/IRQ10/ GPIO1_30                   | IN                          | J5                 | I        | CV <sub>DD</sub> | (1)     |
| SDHC_CLK_SYNC_OUT/SPI_CS3_B/<br>GPIO2_03/SDHC_DAT7 | OUT                         | L6                 | O        | OV <sub>DD</sub> | (1)     |
| SDHC_CMD/GPIO2_04                                  | Command/Response            | A3                 | IO       | OV <sub>DD</sub> | (18)    |
| SDHC_DAT0/GPIO2_05                                 | Data                        | D2                 | IO       | OV <sub>DD</sub> | (18)    |
| SDHC_DAT1/GPIO2_06                                 | Data                        | D3                 | IO       | OV <sub>DD</sub> | (18)    |
| SDHC_DAT2/GPIO2_07                                 | Data                        | H6                 | IO       | OV <sub>DD</sub> | (18)    |
| SDHC_DAT3/GPIO2_08                                 | Data                        | G5                 | IO       | OV <sub>DD</sub> | (18)    |
| SDHC_DAT4/SPI_CS0_B/GPIO2_00                       | Data                        | E3                 | IO       | CV <sub>DD</sub> | —       |
| SDHC_DAT5/SPI_CS1_B/GPIO2_01                       | Data                        | K6                 | IO       | CV <sub>DD</sub> | —       |
| SDHC_DAT6/SPI_CS2_B/GPIO2_02                       | Data                        | H5                 | IO       | CV <sub>DD</sub> | —       |
| SDHC_DAT7/SPI_CS3_B/GPIO2_03/<br>SDHC_CLK_SYNC_OUT | Data                        | L6                 | IO       | CV <sub>DD</sub> | —       |

Table 2-1. Pinout list by bus (Continued)

| Signal                                   | Signal description          | Package pin number | Pin type | Power supply       | Notes     |
|--|-----------------------------|--------------------|----------|--------------------|-----------|
| SDHC_WP/GPIO4_25                         | SDHC Write Protect          | F4                 | I        | OV <sub>DD</sub>   | (1)       |
| <b>Programmable Interrupt Controller</b> |                             |                    |          |                    |           |
| IRQ00                                    | External Interrupt          | G11                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ01                                    | External Interrupt          | E11                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ02                                    | External Interrupt          | D10                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ03/GPIO1_23                           | External Interrupt          | C10                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ04/GPIO1_24                           | External Interrupt          | H12                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ05/GPIO1_25                           | External Interrupt          | D11                | I        | OV <sub>DD</sub>   | (1)       |
| IRQ06/GPIO1_26                           | External Interrupt          | P5                 | I        | LV <sub>DD</sub>   | (1)       |
| IRQ07/GPIO1_27                           | External Interrupt          | P3                 | I        | LV <sub>DD</sub>   | (1)       |
| IRQ08/GPIO1_28                           | External Interrupt          | P6                 | I        | LV <sub>DD</sub>   | (1)       |
| IRQ09/GPIO1_29                           | External Interrupt          | P4                 | I        | LV <sub>DD</sub>   | (1)       |
| IRQ10/GPIO1_30/SDHC_CLK_SYNC_IN          | External Interrupt          | J5                 | I        | CV <sub>DD</sub>   | (1)       |
| IRQ11/GPIO1_31                           | External Interrupt          | D1                 | I        | DV <sub>DD</sub>   | (1)       |
| IRQ_OUT_B/EVT9_B                         | Interrupt Output            | C12                | O        | OV <sub>DD</sub>   | (1)(6)(7) |
| <b>LP Trust</b>                          |                             |                    |          |                    |           |
| LP_TMP_DETECT_B                          | Low Power Tamper Detect     | R7                 | I        | V <sub>DD-LP</sub> | —         |
| <b>Trust</b>                             |                             |                    |          |                    |           |
| TMP_DETECT_B                             | Tamper Detect               | C21                | I        | OV <sub>DD</sub>   | (1)       |
| <b>System Control</b>                    |                             |                    |          |                    |           |
| HRESET_B                                 | Hard Reset                  | F11                | IO       | OV <sub>DD</sub>   | (6)(7)    |
| PORESET_B                                | Power On Reset              | F10                | I        | OV <sub>DD</sub>   | —         |
| RESET_REQ_B                              | Reset Request (POR or Hard) | D12                | O        | OV <sub>DD</sub>   | (1)(5)    |
| <b>Power Management</b>                  |                             |                    |          |                    |           |
| ASLEEP/GPIO1_13/<br>cfg_xvdd_sel         | Asleep                      | A11                | O        | OV <sub>DD</sub>   | (1)(5)    |
| <b>SYSCLK</b>                            |                             |                    |          |                    |           |
| SYSCLK                                   | System Clock                | A10                | I        | OV <sub>DD</sub>   | —         |
| <b>DDR Clocking</b>                      |                             |                    |          |                    |           |
| DDRCLK                                   | DDR Controller Clock        | E23                | I        | OV <sub>DD</sub>   | —         |
| <b>RTC</b>                               |                             |                    |          |                    |           |
| RTC/GPIO1_14                             | Real Time Clock             | A20                | I        | OV <sub>DD</sub>   | (1)       |
| <b>Debug</b>                             |                             |                    |          |                    |           |
| CKSTP_OUT_B                              | Checkstop Out               | D20                | O        | OV <sub>DD</sub>   | (1)(6)(7) |
| CLK_OUT                                  | Clock Out                   | E10                | O        | OV <sub>DD</sub>   | (2)       |
| EVT0_B                                   | Event 0                     | A12                | IO       | OV <sub>DD</sub>   | (9)       |
| EVT1_B                                   | Event 1                     | B12                | IO       | OV <sub>DD</sub>   | —         |



**Table 2-1.** Pinout list by bus (Continued)

| Signal                        | Signal description                      | Package pin number | Pin type | Power supply         | Notes |
|-------------------------------|---|--------------------|----------|----------------------|-------|
| EVT2_B                        | Event 2                                 | G12                | IO       | OV <sub>DD</sub>     | —     |
| EVT3_B                        | Event 3                                 | C11                | IO       | OV <sub>DD</sub>     | —     |
| EVT4_B                        | Event 4                                 | F12                | IO       | OV <sub>DD</sub>     | —     |
| EVT5_B/IIC4_SCL/GPIO4_02      | Event 5                                 | K1                 | IO       | DV <sub>DD</sub>     | —     |
| EVT6_B/IIC4_SDA/GPIO4_03      | Event 6                                 | M1                 | IO       | DV <sub>DD</sub>     | —     |
| EVT7_B/DMA2_DACK0_B/GPIO4_08  | Event 7                                 | H1                 | IO       | DV <sub>DD</sub>     | —     |
| EVT8_B/DMA2_DDONE0_B/GPIO4_09 | Event 8                                 | G3                 | IO       | DV <sub>DD</sub>     | —     |
| EVT9_B/IRQ_OUT_B              | Event 9                                 | C12                | IO       | OV <sub>DD</sub>     | —     |
| <b>DFT</b>                    |   |                    |          |                      |       |
| SCAN_MODE_B                   | Reserved                                | H11                | I        | OV <sub>DD</sub>     | (10)  |
| TEST_SEL_B                    | Reserved                                | C9                 | I        | OV <sub>DD</sub>     | (10)  |
| <b>JTAG</b>                   |   |                    |          |                      |       |
| TCK                           | Test Clock                              | C20                | I        | OV <sub>DD</sub>     | —     |
| TDI                           | Test Data In                            | D22                | I        | OV <sub>DD</sub>     | (9)   |
| TDO                           | Test Data Out                           | E20                | O        | OV <sub>DD</sub>     | (2)   |
| TMS                           | Test Mode Select                        | A21                | I        | OV <sub>DD</sub>     | (9)   |
| TRST_B                        | Test Reset                              | B22                | I        | OV <sub>DD</sub>     | (9)   |
| <b>Analog Signals</b>         |   |                    |          |                      |       |
| D1_MVREF                      | SSTL Reference Voltage                  | F21                | IO       | G1V <sub>DD</sub> /2 | —     |
| D1_TPA                        | DDR Controller 1 Test Point Analog      | C23                | IO       | —                    | (12)  |
| FA_ANALOG_G_V                 | Reserved                                | H21                | IO       | —                    | (15)  |
| FA_ANALOG_PIN                 | Reserved                                | G20                | IO       | —                    | (15)  |
| TD1_ANODE                     | Thermal diode anode                     | K22                | IO       | Internal Diode       | (17)  |
| TD1_CATHODE                   | Thermal diode cathode                   | J21                | IO       | Internal Diode       | (17)  |
| TH_TPA                        | Thermal Test Point Analog               | F8                 | —        | —                    | (12)  |
| <b>Serdes 1</b>               |   |                    |          |                      |       |
| SD1_IMP_CAL_RX                | SerDes Receive Impedance Calibration    | AA15               | I        | S1V <sub>DD</sub>    | (11)  |
| SD1_IMP_CAL_TX                | SerDes Transmit Impedance Calibration   | AC22               | I        | X1V <sub>DD</sub>    | (16)  |
| SD1_PLL1_TPA                  | Reserved for internal use only          | AE15               | O        | AVDD_SD1_PLL1        | (12)  |
| SD1_PLL1_TPD                  | Reserved for internal use only          | AE14               | O        | X1V <sub>DD</sub>    | (12)  |
| SD1_PLL2_TPA                  | Reserved for internal use only          | AF25               | O        | AVDD_SD1_PLL2        | (12)  |
| SD1_PLL2_TPD                  | Reserved for internal use only          | AG25               | O        | X1V <sub>DD</sub>    | (12)  |
| SD1_REF_CLK1_N                | SerDes PLL 1 Reference Clock Complement | AK15               | I        | S1V <sub>DD</sub>    | —     |
| SD1_REF_CLK1_P                | SerDes PLL 1 Reference Clock            | AJ15               | I        | S1V <sub>DD</sub>    | —     |
| SD1_REF_CLK2_N                | SerDes PLL 2 Reference Clock Complement | AK25               | I        | S1V <sub>DD</sub>    | —     |
| SD1_REF_CLK2_P                | SerDes PLL 2 Reference Clock            | AJ25               | I        | S1V <sub>DD</sub>    | —     |
| SD1_RX0_N                     | SerDes Receive Data (negative)          | AH13               | I        | S1V <sub>DD</sub>    | —     |

Table 2-1. Pinout list by bus (Continued)

| Signal          | Signal description                    | Package pin number | Pin type | Power supply      | Notes |
|-----------------|---------------------------------------|--------------------|----------|-------------------|-------|
| SD1_RX0_P       | SerDes Receive Data (positive)        | AH12               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX1_N       | SerDes Receive Data (negative)        | AJ13               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX1_P       | SerDes Receive Data (positive)        | AK13               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX2_N       | SerDes Receive Data (negative)        | AK17               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX2_P       | SerDes Receive Data (positive)        | AJ17               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX3_N       | SerDes Receive Data (negative)        | AH18               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX3_P       | SerDes Receive Data (positive)        | AH17               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX4_N       | SerDes Receive Data (negative)        | AK20               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX4_P       | SerDes Receive Data (positive)        | AJ20               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX5_N       | SerDes Receive Data (negative)        | AH21               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX5_P       | SerDes Receive Data (positive)        | AH20               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX6_N       | SerDes Receive Data (negative)        | AK23               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX6_P       | SerDes Receive Data (positive)        | AJ23               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX7_N       | SerDes Receive Data (negative)        | AH24               | I        | S1V <sub>DD</sub> | –     |
| SD1_RX7_P       | SerDes Receive Data (positive)        | AH23               | I        | S1V <sub>DD</sub> | –     |
| SD1_TX0_N       | SerDes Transmit Data (negative)       | AG15               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX0_P       | SerDes Transmit Data (positive)       | AG14               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX1_N       | SerDes Transmit Data (negative)       | AF16               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX1_P       | SerDes Transmit Data (positive)       | AE16               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX2_N       | SerDes Transmit Data (negative)       | AD19               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX2_P       | SerDes Transmit Data (positive)       | AD18               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX3_N       | SerDes Transmit Data (negative)       | AE18               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX3_P       | SerDes Transmit Data (positive)       | AF18               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX4_N       | SerDes Transmit Data (negative)       | AD21               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX4_P       | SerDes Transmit Data (positive)       | AD20               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX5_N       | SerDes Transmit Data (negative)       | AE21               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX5_P       | SerDes Transmit Data (positive)       | AF21               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX6_N       | SerDes Transmit Data (negative)       | AE23               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX6_P       | SerDes Transmit Data (positive)       | AF23               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX7_N       | SerDes Transmit Data (negative)       | AD24               | O        | X1V <sub>DD</sub> | –     |
| SD1_TX7_P       | SerDes Transmit Data (positive)       | AD23               | O        | X1V <sub>DD</sub> | –     |
| <b>Serdes 2</b> |                                       |                    |          |                   |       |
| SD2_IMP_CAL_RX  | SerDes Receive Impedance Calibration  | AA8                | I        | S2V <sub>DD</sub> | (11)  |
| SD2_IMP_CAL_TX  | SerDes Transmit Impedance Calibration | AE10               | I        | X2V <sub>DD</sub> | (16)  |
| SD2_PLL1_TPA    | Reserved for internal use only        | AC7                | O        | AVDD_SD2_PLL1     | (12)  |
| SD2_PLL1_TPD    | Reserved for internal use only        | AC8                | O        | X2V <sub>DD</sub> | (12)  |
| SD2_PLL2_TPA    | Reserved for internal use only        | AG11               | O        | AVDD_SD2_PLL2     | (12)  |

**Table 2-1.** Pinout list by bus (Continued)

| Signal         | Signal description                      | Package pin number | Pin type | Power supply      | Notes |
|----------------|---|--------------------|----------|-------------------|-------|
| SD2_PLL2_TPD   | Reserved for internal use only          | AF11               | O        | X2V <sub>DD</sub> | (12)  |
| SD2_REF_CLK1_N | SerDes PLL 1 Reference Clock Complement | AD5                | I        | S2V <sub>DD</sub> | –     |
| SD2_REF_CLK1_P | SerDes PLL 1 Reference Clock            | AD6                | I        | S2V <sub>DD</sub> | –     |
| SD2_REF_CLK2_N | SerDes PLL 2 Reference Clock Complement | AJ11               | I        | S2V <sub>DD</sub> | –     |
| SD2_REF_CLK2_P | SerDes PLL 2 Reference Clock            | AK11               | I        | S2V <sub>DD</sub> | –     |
| SD2_RX0_N      | SerDes Receive Data (negative)          | AA4                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX0_P      | SerDes Receive Data (positive)          | AA3                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX1_N      | SerDes Receive Data (negative)          | AC4                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX1_P      | SerDes Receive Data (positive)          | AC3                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX2_N      | SerDes Receive Data (negative)          | AD2                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX2_P      | SerDes Receive Data (positive)          | AD1                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX3_N      | SerDes Receive Data (negative)          | AJ3                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX3_P      | SerDes Receive Data (positive)          | AK3                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX4_N      | SerDes Receive Data (negative)          | AK5                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX4_P      | SerDes Receive Data (positive)          | AJ5                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX5_N      | SerDes Receive Data (negative)          | AJ6                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX5_P      | SerDes Receive Data (positive)          | AK6                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX6_N      | SerDes Receive Data (negative)          | AK8                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX6_P      | SerDes Receive Data (positive)          | AJ8                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX7_N      | SerDes Receive Data (negative)          | AJ9                | I        | S2V <sub>DD</sub> | –     |
| SD2_RX7_P      | SerDes Receive Data (positive)          | AK9                | I        | S2V <sub>DD</sub> | –     |
| SD2_TX0_N      | SerDes Transmit Data (negative)         | AB1                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX0_P      | SerDes Transmit Data (positive)         | AB2                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX1_N      | SerDes Transmit Data (negative)         | AB6                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX1_P      | SerDes Transmit Data (positive)         | AB5                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX2_N      | SerDes Transmit Data (negative)         | AF2                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX2_P      | SerDes Transmit Data (positive)         | AF1                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX3_N      | SerDes Transmit Data (negative)         | AH2                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX3_P      | SerDes Transmit Data (positive)         | AH1                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX4_N      | SerDes Transmit Data (negative)         | AG5                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX4_P      | SerDes Transmit Data (positive)         | AF5                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX5_N      | SerDes Transmit Data (negative)         | AF6                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX5_P      | SerDes Transmit Data (positive)         | AG6                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX6_N      | SerDes Transmit Data (negative)         | AG8                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX6_P      | SerDes Transmit Data (positive)         | AF8                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX7_N      | SerDes Transmit Data (negative)         | AF9                | O        | X2V <sub>DD</sub> | –     |
| SD2_TX7_P      | SerDes Transmit Data (positive)         | AG9                | O        | X2V <sub>DD</sub> | –     |

Table 2-1. Pinout list by bus (Continued)

| Signal                                 | Signal description                       | Package pin number | Pin type | Power supply         | Notes   |
|--|--|--------------------|----------|----------------------|---------|
| <b>USB PHY 1 &amp; 2</b>               |  |                    |          |                      |         |
| USB1_DRVVBUS                           | USB PHY Digital signal – Drive VBUS      | A8                 | O        | USB_HV <sub>DD</sub> | –       |
| USB1_PWRFAULT                          | USB PHY Digital signal – Power Fault     | B9                 | I        | USB_HV <sub>DD</sub> | –       |
| USB1_UDM                               | USB PHY Data Minus                       | C7                 | IO       | USB_HV <sub>DD</sub> | –       |
| USB1_UDP                               | USB PHY Data Plus                        | B8                 | IO       | USB_HV <sub>DD</sub> | –       |
| USB1_UID                               | USB PHY ID Detect                        | E5                 | I        | USB_OV <sub>DD</sub> | –       |
| USB1_VBUSCLMP                          | USB PHY VBUS                             | E7                 | I        | USB_HV <sub>DD</sub> | –       |
| USB2_DRVVBUS                           | USB PHY Digital signal – Drive VBUS      | B5                 | O        | USB_HV <sub>DD</sub> | –       |
| USB2_PWRFAULT                          | USB PHY Digital signal – Power Fault     | A5                 | I        | USB_HV <sub>DD</sub> | –       |
| USB2_UDM                               | USB PHY Data Minus                       | B6                 | IO       | USB_HV <sub>DD</sub> | –       |
| USB2_UDP                               | USB PHY Data Plus                        | A6                 | IO       | USB_HV <sub>DD</sub> | –       |
| USB2_UID                               | USB PHY ID Detect                        | D7                 | I        | USB_OV <sub>DD</sub> | –       |
| USB2_VBUSCLMP                          | USB PHY VBUS                             | C6                 | I        | USB_HV <sub>DD</sub> | –       |
| USBCLK                                 | USB PHY Clock In                         | B11                | I        | OV <sub>DD</sub>     | –       |
| USB_IBIAS_REXT                         | USB PHY Impedance Calibration            | F7                 | IO       | USB_OV <sub>DD</sub> | (19)    |
| <b>IEEE1588</b>                        |  |                    |          |                      |         |
| TSEC_1588_ALARM_OUT1/GPIO3_03          | Alarm Out 1                              | U1                 | O        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_ALARM_OUT2/GPIO3_04          | Alarm Out 2                              | W5                 | O        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_CLK_IN/GPIO3_00              | Clock In                                 | T3                 | I        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_CLK_OUT/GPIO3_05             | Clock Out                                | V3                 | O        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_PULSE_OUT1/GPIO3_06          | Pulse Out 1                              | W2                 | O        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_PULSE_OUT2/GPIO3_07          | Pulse Out 2                              | W1                 | O        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_TRIG_IN1/GPIO3_01            | Trigger In 1                             | V4                 | I        | LV <sub>DD</sub>     | (1)     |
| TSEC_1588_TRIG_IN2/GPIO3_02            | Trigger In 2                             | V2                 | I        | LV <sub>DD</sub>     | (1)     |
| <b>Ethernet Management Interface 1</b> |  |                    |          |                      |         |
| EMI1_MDC                               | Management Data Clock                    | T5                 | O        | LV <sub>DD</sub>     | –       |
| EMI1_MDIO                              | Management Data In/Out                   | N3                 | IO       | LV <sub>DD</sub>     | –       |
| <b>Ethernet Management Interface 2</b> |  |                    |          |                      |         |
| EMI2_MDC                               | Management Data Clock (1.2V open drain)  | B3                 | O        | OV <sub>DD</sub>     | (7)(13) |
| EMI2_MDIO                              | Management Data In/Out (1.2V open drain) | F5                 | IO       | OV <sub>DD</sub>     | (7)(13) |
| <b>Ethernet Controller (RGMII) 1</b>   |  |                    |          |                      |         |
| EC1_GTX_CLK/GPIO3_16                   | Transmit Clock Out                       | P1                 | O        | LV <sub>DD</sub>     | (1)     |
| EC1_GTX_CLK125/GPIO3_17                | Reference Clock                          | M2                 | I        | LV <sub>DD</sub>     | (1)     |
| EC1_RXD0/GPIO3_21                      | Receive Data                             | R5                 | I        | LV <sub>DD</sub>     | (1)     |
| EC1_RXD1/GPIO3_20                      | Receive Data                             | N5                 | I        | LV <sub>DD</sub>     | (1)     |
| EC1_RXD2/GPIO3_19                      | Receive Data                             | N6                 | I        | LV <sub>DD</sub>     | (1)     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal                               | Signal description                  | Package pin number | Pin type | Power supply     | Notes   |
|--------------------------------------|-------------------------------------|--------------------|----------|------------------|---------|
| EC1_RXD3/GPIO3_18                    | Receive Data                        | L1                 | I        | LV <sub>DD</sub> | (1)     |
| EC1_RX_CLK/GPIO3_23                  | Receive Clock                       | M4                 | I        | LV <sub>DD</sub> | (1)     |
| EC1_RX_CTL/GPIO3_22                  | Receive Data Valid                  | L3                 | I        | LV <sub>DD</sub> | (1)     |
| EC1_TXD0/GPIO3_14                    | Transmit Data                       | T6                 | O        | LV <sub>DD</sub> | (1)     |
| EC1_TXD1/GPIO3_13                    | Transmit Data                       | N1                 | O        | LV <sub>DD</sub> | (1)     |
| EC1_TXD2/GPIO3_12                    | Transmit Data                       | N2                 | O        | LV <sub>DD</sub> | (1)     |
| EC1_TXD3/GPIO3_11                    | Transmit Data                       | R4                 | O        | LV <sub>DD</sub> | (1)     |
| EC1_TX_CTL/GPIO3_15                  | Transmit Enable                     | M3                 | O        | LV <sub>DD</sub> | (1)(14) |
| <b>Ethernet Controller (RGMII) 2</b> |                                     |                    |          |                  |         |
| EC2_GTX_CLK/GPIO4_28                 | Transmit Clock Out                  | T1                 | O        | LV <sub>DD</sub> | (1)     |
| EC2_GTX_CLK125/GPIO4_29              | Reference Clock                     | V1                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RXD0/GPIO3_31                    | Receive Data                        | R1                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RXD1/GPIO3_30                    | Receive Data                        | T2                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RXD2/GPIO3_29                    | Receive Data                        | U4                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RXD3/GPIO3_28                    | Receive Data                        | R2                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RX_CLK/GPIO4_31                  | Receive Clock                       | V6                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_RX_CTL/GPIO4_30                  | Receive Data Valid                  | U6                 | I        | LV <sub>DD</sub> | (1)     |
| EC2_TXD0/GPIO3_27                    | Transmit Data                       | W6                 | O        | LV <sub>DD</sub> | (1)     |
| EC2_TXD1/GPIO3_26                    | Transmit Data                       | U5                 | O        | LV <sub>DD</sub> | (1)     |
| EC2_TXD2/GPIO3_25                    | Transmit Data                       | U3                 | O        | LV <sub>DD</sub> | (1)     |
| EC2_TXD3/GPIO3_24                    | Transmit Data                       | V5                 | O        | LV <sub>DD</sub> | (1)     |
| EC2_TX_CTL/GPIO4_27                  | Transmit Enable                     | R3                 | O        | LV <sub>DD</sub> | (1)(14) |
| <b>DMA</b>                           |                                     |                    |          |                  |         |
| DMA1_DACK0_B/GPIO4_05                | DMA1 channel 0 acknowledge          | E1                 | O        | DV <sub>DD</sub> | (1)     |
| DMA1_DDONE0_B/GPIO4_06               | DMA1 channel 0 done                 | K5                 | O        | DV <sub>DD</sub> | (1)     |
| DMA1_DREQ0_B/GPIO4_04                | DMA1 channel 0 request              | L5                 | I        | DV <sub>DD</sub> | (1)     |
| DMA2_DACK0_B/GPIO4_08/EVT7_B         | DMA2 channel 0 acknowledge          | H1                 | O        | DV <sub>DD</sub> | (1)     |
| DMA2_DDONE0_B/GPIO4_09/EVT8_B        | DMA2 channel 0 done                 | G3                 | O        | DV <sub>DD</sub> | (1)     |
| DMA2_DREQ0_B/GPIO4_07                | DMA2 channel 0 request              | F3                 | I        | DV <sub>DD</sub> | (1)     |
| <b>Power-On-Reset Configuration</b>  |                                     |                    |          |                  |         |
| cfg_dram_type/IFC_A21                | Power-On-Reset Configuration Signal | B14                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput0/IFC_AD00                | Power-On-Reset Configuration Signal | A13                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput1/IFC_AD01                | Power-On-Reset Configuration Signal | G13                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput2/IFC_AD02                | Power-On-Reset Configuration Signal | C14                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput3/IFC_AD03                | Power-On-Reset Configuration Signal | D13                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput4/IFC_AD04                | Power-On-Reset Configuration Signal | A15                | I        | OV <sub>DD</sub> | (1)(4)  |
| cfg_gpinput5/IFC_AD05                | Power-On-Reset Configuration Signal | F13                | I        | OV <sub>DD</sub> | (1)(4)  |

**Table 2-1.** Pinout list by bus (Continued)

| Signal                              | Signal description                  | Package pin number | Pin type | Power supply     | Notes  |
|-------------------------------------|-------------------------------------|--------------------|----------|------------------|--------|
| cfg_gpinout6/IFC_AD06               | Power-On-Reset Configuration Signal | E14                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_gpinout7/IFC_AD07               | Power-On-Reset Configuration Signal | J13                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_ifc_te/IFC_TE                   | Power-On-Reset Configuration Signal | A19                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src0/IFC_AD08               | Power-On-Reset Configuration Signal | E13                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src1/IFC_AD09               | Power-On-Reset Configuration Signal | F14                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src2/IFC_AD10               | Power-On-Reset Configuration Signal | H14                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src3/IFC_AD11               | Power-On-Reset Configuration Signal | A14                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src4/IFC_AD12               | Power-On-Reset Configuration Signal | C13                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src5/IFC_AD13               | Power-On-Reset Configuration Signal | B15                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src6/IFC_AD14               | Power-On-Reset Configuration Signal | F15                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src7/IFC_AD15               | Power-On-Reset Configuration Signal | D14                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_rcw_src8/IFC_CLE                | Power-On-Reset Configuration Signal | H19                | I        | OV <sub>DD</sub> | (1)(4) |
| cfg_xvdd_sel/ASLEEP/GPIO1_13        | Power-On-Reset Configuration Signal | A11                | I        | OV <sub>DD</sub> | (1)(5) |
| <b>General Purpose Input/Output</b> |                                     |                    |          |                  |        |
| GPIO1_09/IFC_CS4_B                  | General Purpose Input/Output        | E19                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_10/IFC_CS5_B                  | General Purpose Input/Output        | C18                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_11/IFC_CS6_B                  | General Purpose Input/Output        | D21                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_12/IFC_CS7_B                  | General Purpose Input/Output        | G19                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_13/ASLEEP/<br>cfg_xvdd_sel    | General Purpose Input/Output        | A11                | O        | OV <sub>DD</sub> | (1)(5) |
| GPIO1_14/RTC                        | General Purpose Input/Output        | A20                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_15/UART1_SOUT                 | General Purpose Input/Output        | J1                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_16/UART2_SOUT                 | General Purpose Input/Output        | K3                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_17/UART1_SIN                  | General Purpose Input/Output        | J3                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_18/UART2_SIN                  | General Purpose Input/Output        | F2                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_19/UART1_RTS_B/UART3_SOUT     | General Purpose Input/Output        | G1                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_20/UART2_RTS_B/UART4_SOUT     | General Purpose Input/Output        | J4                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_21/UART1_CTS_B/UART3_SIN      | General Purpose Input/Output        | L4                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_22/UART2_CTS_B/UART4_SIN      | General Purpose Input/Output        | F1                 | IO       | DV <sub>DD</sub> | —      |
| GPIO1_23/IRQ03                      | General Purpose Input/Output        | C10                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_24/IRQ04                      | General Purpose Input/Output        | H12                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_25/IRQ05                      | General Purpose Input/Output        | D11                | IO       | OV <sub>DD</sub> | —      |
| GPIO1_26/IRQ06                      | General Purpose Input/Output        | P5                 | IO       | LV <sub>DD</sub> | —      |
| GPIO1_27/IRQ07                      | General Purpose Input/Output        | P3                 | IO       | LV <sub>DD</sub> | —      |
| GPIO1_28/IRQ08                      | General Purpose Input/Output        | P6                 | IO       | LV <sub>DD</sub> | —      |
| GPIO1_29/IRQ09                      | General Purpose Input/Output        | P4                 | IO       | LV <sub>DD</sub> | —      |
| GPIO1_30/IRQ10/SDHC_CLK_SYNC_IN     | General Purpose Input/Output        | J5                 | IO       | CV <sub>DD</sub> | —      |

**Table 2-1.** Pinout list by bus (Continued)

| Signal   | Signal description           | Package pin number | Pin type | Power supply     | Notes |
|--|------------------------------|--------------------|----------|------------------|-------|
| GPIO1_31/IRQ11                                     | General Purpose Input/Output | D1                 | IO       | DV <sub>DD</sub> | –     |
| GPIO2_00/SPI_CS0_B/SDHC_DAT4                       | General Purpose Input/Output | E3                 | IO       | CV <sub>DD</sub> | –     |
| GPIO2_01/SPI_CS1_B/SDHC_DAT5                       | General Purpose Input/Output | K6                 | IO       | CV <sub>DD</sub> | –     |
| GPIO2_02/SPI_CS2_B/SDHC_DAT6                       | General Purpose Input/Output | H5                 | IO       | CV <sub>DD</sub> | –     |
| GPIO2_03/SPI_CS3_B/SDHC_DAT7/<br>SDHC_CLK_SYNC_OUT | General Purpose Input/Output | L6                 | IO       | CV <sub>DD</sub> | –     |
| GPIO2_04/SDHC_CMD                                  | General Purpose Input/Output | A3                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_05/SDHC_DAT0                                 | General Purpose Input/Output | D2                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_06/SDHC_DAT1                                 | General Purpose Input/Output | D3                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_07/SDHC_DAT2                                 | General Purpose Input/Output | H6                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_08/SDHC_DAT3                                 | General Purpose Input/Output | G5                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_09/SDHC_CLK                                  | General Purpose Input/Output | C4                 | IO       | OV <sub>DD</sub> | –     |
| GPIO2_10/IFC_CS1_B                                 | General Purpose Input/Output | F17                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_11/IFC_CS2_B                                 | General Purpose Input/Output | D19                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_12/IFC_CS3_B                                 | General Purpose Input/Output | B17                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_13/IFC_PAR0                                  | General Purpose Input/Output | F18                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_14/IFC_PAR1                                  | General Purpose Input/Output | A17                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_15/IFC_PERR_B                                | General Purpose Input/Output | F19                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_25/IFC_A25/IFC_WP1_B                         | General Purpose Input/Output | E17                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_26/IFC_A26/IFC_WP2_B                         | General Purpose Input/Output | D16                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_27/IFC_A27/IFC_WP3_B                         | General Purpose Input/Output | G17                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_28/IFC_A28                                   | General Purpose Input/Output | F16                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_29/IFC_A29/IFC_RB2_B                         | General Purpose Input/Output | G16                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_30/IFC_A30/IFC_RB3_B                         | General Purpose Input/Output | B21                | IO       | OV <sub>DD</sub> | –     |
| GPIO2_31/IFC_A31/IFC_RB4_B                         | General Purpose Input/Output | E16                | IO       | OV <sub>DD</sub> | –     |
| GPIO3_00/<br>TSEC_1588_CLK_IN                      | General Purpose Input/Output | T3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_01/<br>TSEC_1588_TRIG_IN1                    | General Purpose Input/Output | V4                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_02/<br>TSEC_1588_TRIG_IN2                    | General Purpose Input/Output | V2                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_03/<br>TSEC_1588_ALARM_OUT1                  | General Purpose Input/Output | U1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_04/<br>TSEC_1588_ALARM_OUT2                  | General Purpose Input/Output | W5                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_05/<br>TSEC_1588_CLK_OUT                     | General Purpose Input/Output | V3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_06/<br>TSEC_1588_PULSE_OUT1                  | General Purpose Input/Output | W2                 | IO       | LV <sub>DD</sub> | –     |



**Table 2-1.** Pinout list by bus (Continued)

| Signal                            | Signal description           | Package pin number | Pin type | Power supply     | Notes |
|-----------------------------------|------------------------------|--------------------|----------|------------------|-------|
| GPIO3_07/<br>TSEC_1588_PULSE_OUT2 | General Purpose Input/Output | W1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_11/EC1_TXD3                 | General Purpose Input/Output | R4                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_12/EC1_TXD2                 | General Purpose Input/Output | N2                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_13/EC1_TXD1                 | General Purpose Input/Output | N1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_14/EC1_TXD0                 | General Purpose Input/Output | T6                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_15/EC1_TX_CTL               | General Purpose Input/Output | M3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_16/EC1_GTX_CLK              | General Purpose Input/Output | P1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_17/EC1_GTX_CLK125           | General Purpose Input/Output | M2                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_18/EC1_RXD3                 | General Purpose Input/Output | L1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_19/EC1_RXD2                 | General Purpose Input/Output | N6                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_20/EC1_RXD1                 | General Purpose Input/Output | N5                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_21/EC1_RXD0                 | General Purpose Input/Output | R5                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_22/EC1_RX_CTL               | General Purpose Input/Output | L3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_23/EC1_RX_CLK               | General Purpose Input/Output | M4                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_24/EC2_TXD3                 | General Purpose Input/Output | V5                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_25/EC2_TXD2                 | General Purpose Input/Output | U3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_26/EC2_TXD1                 | General Purpose Input/Output | U5                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_27/EC2_TXD0                 | General Purpose Input/Output | W6                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_28/EC2_RXD3                 | General Purpose Input/Output | R2                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_29/EC2_RXD2                 | General Purpose Input/Output | U4                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_30/EC2_RXD1                 | General Purpose Input/Output | T2                 | IO       | LV <sub>DD</sub> | –     |
| GPIO3_31/EC2_RXD0                 | General Purpose Input/Output | R1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO4_00/IIC3_SCL                 | General Purpose Input/Output | J6                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_01/IIC3_SDA                 | General Purpose Input/Output | J2                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_02/IIC4_SCL/EVT5_B          | General Purpose Input/Output | K1                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_03/IIC4_SDA/EVT6_B          | General Purpose Input/Output | M1                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_04/DMA1_DREQ0_B             | General Purpose Input/Output | L5                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_05/DMA1_DACK0_B             | General Purpose Input/Output | E1                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_06/DMA1_DDONE0_B            | General Purpose Input/Output | K5                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_07/DMA2_DREQ0_B             | General Purpose Input/Output | F3                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_08/DMA2_DACK0_B/EVT7_B      | General Purpose Input/Output | H1                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_09/<br>DMA2_DDONE0_B/EVT8_B | General Purpose Input/Output | G3                 | IO       | DV <sub>DD</sub> | –     |
| GPIO4_24/SDHC_CD_B                | General Purpose Input/Output | E4                 | IO       | OV <sub>DD</sub> | –     |
| GPIO4_25/SDHC_WP                  | General Purpose Input/Output | F4                 | IO       | OV <sub>DD</sub> | –     |
| GPIO4_27/EC2_TX_CTL               | General Purpose Input/Output | R3                 | IO       | LV <sub>DD</sub> | –     |
| GPIO4_28/EC2_GTX_CLK              | General Purpose Input/Output | T1                 | IO       | LV <sub>DD</sub> | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal                          | Signal description           | Package pin number | Pin type | Power supply     | Notes |
|---------------------------------|------------------------------|--------------------|----------|------------------|-------|
| GPIO4_29/EC2_GTX_CLK125         | General Purpose Input/Output | V1                 | IO       | LV <sub>DD</sub> | –     |
| GPIO4_30/EC2_RX_CTL             | General Purpose Input/Output | U6                 | IO       | LV <sub>DD</sub> | –     |
| GPIO4_31/EC2_RX_CLK             | General Purpose Input/Output | V6                 | IO       | LV <sub>DD</sub> | –     |
| <b>Power and Ground Signals</b> |                              |                    |          |                  |       |
| GND001                          | GND                          | AK27               | –        | –                | –     |
| GND002                          | GND                          | AH28               | –        | –                | –     |
| GND003                          | GND                          | AG28               | –        | –                | –     |
| GND004                          | GND                          | AG26               | –        | –                | –     |
| GND005                          | GND                          | AF26               | –        | –                | –     |
| GND006                          | GND                          | AE28               | –        | –                | –     |
| GND007                          | GND                          | AE25               | –        | –                | –     |
| GND008                          | GND                          | AD26               | –        | –                | –     |
| GND009                          | GND                          | AD25               | –        | –                | –     |
| GND010                          | GND                          | AC28               | –        | –                | –     |
| GND011                          | GND                          | AC24               | –        | –                | –     |
| GND012                          | GND                          | AB26               | –        | –                | –     |
| GND013                          | GND                          | AA28               | –        | –                | –     |
| GND014                          | GND                          | AA24               | –        | –                | –     |
| GND015                          | GND                          | AA22               | –        | –                | –     |
| GND016                          | GND                          | Y26                | –        | –                | –     |
| GND017                          | GND                          | Y22                | –        | –                | –     |
| GND018                          | GND                          | Y9                 | –        | –                | –     |
| GND019                          | GND                          | Y8                 | –        | –                | –     |
| GND020                          | GND                          | Y7                 | –        | –                | –     |
| GND021                          | GND                          | Y6                 | –        | –                | –     |
| GND022                          | GND                          | Y5                 | –        | –                | –     |
| GND023                          | GND                          | Y2                 | –        | –                | –     |
| GND024                          | GND                          | Y1                 | –        | –                | –     |
| GND025                          | GND                          | W28                | –        | –                | –     |
| GND026                          | GND                          | W24                | –        | –                | –     |
| GND027                          | GND                          | W22                | –        | –                | –     |
| GND028                          | GND                          | W20                | –        | –                | –     |
| GND029                          | GND                          | W18                | –        | –                | –     |
| GND030                          | GND                          | W16                | –        | –                | –     |
| GND031                          | GND                          | W14                | –        | –                | –     |
| GND032                          | GND                          | W12                | –        | –                | –     |
| GND033                          | GND                          | W10                | –        | –                | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|--------|--------------------|--------------------|----------|--------------|-------|
| GND034 | GND                | W8                 | –        | –            | –     |
| GND035 | GND                | W7                 | –        | –            | –     |
| GND036 | GND                | W4                 | –        | –            | –     |
| GND037 | GND                | W3                 | –        | –            | –     |
| GND038 | GND                | V26                | –        | –            | –     |
| GND039 | GND                | V23                | –        | –            | –     |
| GND040 | GND                | V21                | –        | –            | –     |
| GND041 | GND                | V19                | –        | –            | –     |
| GND042 | GND                | V17                | –        | –            | –     |
| GND043 | GND                | V15                | –        | –            | –     |
| GND044 | GND                | V13                | –        | –            | –     |
| GND045 | GND                | V11                | –        | –            | –     |
| GND046 | GND                | V9                 | –        | –            | –     |
| GND047 | GND                | V7                 | –        | –            | –     |
| GND048 | GND                | U28                | –        | –            | –     |
| GND049 | GND                | U24                | –        | –            | –     |
| GND050 | GND                | U20                | –        | –            | –     |
| GND051 | GND                | U18                | –        | –            | –     |
| GND052 | GND                | U16                | –        | –            | –     |
| GND053 | GND                | U14                | –        | –            | –     |
| GND054 | GND                | U12                | –        | –            | –     |
| GND055 | GND                | U10                | –        | –            | –     |
| GND056 | GND                | U7                 | –        | –            | –     |
| GND057 | GND                | U2                 | –        | –            | –     |
| GND058 | GND                | T26                | –        | –            | –     |
| GND059 | GND                | T23                | –        | –            | –     |
| GND060 | GND                | T21                | –        | –            | –     |
| GND061 | GND                | T19                | –        | –            | –     |
| GND062 | GND                | T17                | –        | –            | –     |
| GND063 | GND                | T15                | –        | –            | –     |
| GND064 | GND                | T13                | –        | –            | –     |
| GND065 | GND                | T11                | –        | –            | –     |
| GND066 | GND                | T9                 | –        | –            | –     |
| GND067 | GND                | T7                 | –        | –            | –     |
| GND068 | GND                | T4                 | –        | –            | –     |
| GND069 | GND                | R28                | –        | –            | –     |
| GND070 | GND                | R24                | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|--------|--------------------|--------------------|----------|--------------|-------|
| GND071 | GND                | R20                | –        | –            | –     |
| GND072 | GND                | R18                | –        | –            | –     |
| GND073 | GND                | R16                | –        | –            | –     |
| GND074 | GND                | R14                | –        | –            | –     |
| GND075 | GND                | R12                | –        | –            | –     |
| GND076 | GND                | R10                | –        | –            | –     |
| GND077 | GND                | R6                 | –        | –            | –     |
| GND078 | GND                | P26                | –        | –            | –     |
| GND079 | GND                | P23                | –        | –            | –     |
| GND080 | GND                | P21                | –        | –            | –     |
| GND081 | GND                | P19                | –        | –            | –     |
| GND082 | GND                | P17                | –        | –            | –     |
| GND083 | GND                | P15                | –        | –            | –     |
| GND084 | GND                | P13                | –        | –            | –     |
| GND085 | GND                | P11                | –        | –            | –     |
| GND086 | GND                | P9                 | –        | –            | –     |
| GND087 | GND                | P7                 | –        | –            | –     |
| GND088 | GND                | P2                 | –        | –            | –     |
| GND089 | GND                | N28                | –        | –            | –     |
| GND090 | GND                | N24                | –        | –            | –     |
| GND091 | GND                | N20                | –        | –            | –     |
| GND092 | GND                | N18                | –        | –            | –     |
| GND093 | GND                | N16                | –        | –            | –     |
| GND094 | GND                | N14                | –        | –            | –     |
| GND095 | GND                | N12                | –        | –            | –     |
| GND096 | GND                | N10                | –        | –            | –     |
| GND097 | GND                | N7                 | –        | –            | –     |
| GND098 | GND                | N4                 | –        | –            | –     |
| GND099 | GND                | M26                | –        | –            | –     |
| GND100 | GND                | M23                | –        | –            | –     |
| GND101 | GND                | M21                | –        | –            | –     |
| GND102 | GND                | M19                | –        | –            | –     |
| GND103 | GND                | M17                | –        | –            | –     |
| GND104 | GND                | M15                | –        | –            | –     |
| GND105 | GND                | M13                | –        | –            | –     |
| GND106 | GND                | M11                | –        | –            | –     |
| GND107 | GND                | M9                 | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|--------|--------------------|--------------------|----------|--------------|-------|
| GND108 | GND                | M7                 | –        | –            | –     |
| GND109 | GND                | M5                 | –        | –            | –     |
| GND110 | GND                | L28                | –        | –            | –     |
| GND111 | GND                | L24                | –        | –            | –     |
| GND112 | GND                | L20                | –        | –            | –     |
| GND113 | GND                | L18                | –        | –            | –     |
| GND114 | GND                | L16                | –        | –            | –     |
| GND115 | GND                | L14                | –        | –            | –     |
| GND116 | GND                | L12                | –        | –            | –     |
| GND117 | GND                | L10                | –        | –            | –     |
| GND118 | GND                | L7                 | –        | –            | –     |
| GND119 | GND                | L2                 | –        | –            | –     |
| GND120 | GND                | K26                | –        | –            | –     |
| GND121 | GND                | K23                | –        | –            | –     |
| GND122 | GND                | K11                | –        | –            | –     |
| GND123 | GND                | K9                 | –        | –            | –     |
| GND124 | GND                | K7                 | –        | –            | –     |
| GND125 | GND                | K4                 | –        | –            | –     |
| GND126 | GND                | J28                | –        | –            | –     |
| GND127 | GND                | J24                | –        | –            | –     |
| GND128 | GND                | J22                | –        | –            | –     |
| GND129 | GND                | J18                | –        | –            | –     |
| GND130 | GND                | J16                | –        | –            | –     |
| GND131 | GND                | J14                | –        | –            | –     |
| GND132 | GND                | J12                | –        | –            | –     |
| GND133 | GND                | J11                | –        | –            | –     |
| GND134 | GND                | J9                 | –        | –            | –     |
| GND135 | GND                | H26                | –        | –            | –     |
| GND136 | GND                | H22                | –        | –            | –     |
| GND137 | GND                | H17                | –        | –            | –     |
| GND138 | GND                | H15                | –        | –            | –     |
| GND139 | GND                | H13                | –        | –            | –     |
| GND140 | GND                | H10                | –        | –            | –     |
| GND141 | GND                | H2                 | –        | –            | –     |
| GND142 | GND                | G28                | –        | –            | –     |
| GND143 | GND                | G24                | –        | –            | –     |
| GND144 | GND                | G22                | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal     | Signal description      | Package pin number | Pin type | Power supply | Notes |
|------------|-------------------------|--------------------|----------|--------------|-------|
| GND145     | GND                     | G21                | –        | –            | –     |
| GND146     | GND                     | G10                | –        | –            | –     |
| GND147     | GND                     | G8                 | –        | –            | –     |
| GND148     | GND                     | G4                 | –        | –            | –     |
| GND149     | GND                     | F26                | –        | –            | –     |
| GND150     | GND                     | F23                | –        | –            | –     |
| GND151     | GND                     | F20                | –        | –            | –     |
| GND152     | GND                     | F9                 | –        | –            | –     |
| GND153     | GND                     | E28                | –        | –            | –     |
| GND154     | GND                     | E24                | –        | –            | –     |
| GND155     | GND                     | E22                | –        | –            | –     |
| GND156     | GND                     | E21                | –        | –            | –     |
| GND157     | GND                     | E18                | –        | –            | –     |
| GND158     | GND                     | E15                | –        | –            | –     |
| GND159     | GND                     | E12                | –        | –            | –     |
| GND160     | GND                     | E2                 | –        | –            | –     |
| GND161     | GND                     | D26                | –        | –            | –     |
| GND162     | GND                     | D23                | –        | –            | –     |
| GND163     | GND                     | D9                 | –        | –            | –     |
| GND164     | GND                     | D4                 | –        | –            | –     |
| GND165     | GND                     | C28                | –        | –            | –     |
| GND166     | GND                     | C24                | –        | –            | –     |
| GND167     | GND                     | C22                | –        | –            | –     |
| GND168     | GND                     | C3                 | –        | –            | –     |
| GND169     | GND                     | B26                | –        | –            | –     |
| GND170     | GND                     | B23                | –        | –            | –     |
| GND171     | GND                     | B19                | –        | –            | –     |
| GND172     | GND                     | B16                | –        | –            | –     |
| GND173     | GND                     | B13                | –        | –            | –     |
| GND174     | GND                     | B10                | –        | –            | –     |
| GND175     | GND                     | B4                 | –        | –            | –     |
| GND176     | GND                     | B1                 | –        | –            | –     |
| GND177     | GND                     | A27                | –        | –            | –     |
| GND178     | GND                     | A23                | –        | –            | –     |
| GND179     | GND                     | A4                 | –        | –            | –     |
| GND180     | GND                     | A2                 | –        | –            | –     |
| USB_AGND01 | USB PHY Transceiver GND | H8                 | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal     | Signal description      | Package pin number | Pin type | Power supply | Notes |
|------------|-------------------------|--------------------|----------|--------------|-------|
| USB_AGND02 | USB PHY Transceiver GND | H7                 | –        | –            | –     |
| USB_AGND03 | USB PHY Transceiver GND | G6                 | –        | –            | –     |
| USB_AGND04 | USB PHY Transceiver GND | E6                 | –        | –            | –     |
| USB_AGND05 | USB PHY Transceiver GND | D8                 | –        | –            | –     |
| USB_AGND06 | USB PHY Transceiver GND | D6                 | –        | –            | –     |
| USB_AGND07 | USB PHY Transceiver GND | D5                 | –        | –            | –     |
| USB_AGND08 | USB PHY Transceiver GND | C5                 | –        | –            | –     |
| USB_AGND09 | USB PHY Transceiver GND | B7                 | –        | –            | –     |
| USB_AGND10 | USB PHY Transceiver GND | A9                 | –        | –            | –     |
| X1GND01    | Serdes1 transceiver GND | AG23               | –        | –            | –     |
| X1GND02    | Serdes1 transceiver GND | AG21               | –        | –            | –     |
| X1GND03    | Serdes1 transceiver GND | AG18               | –        | –            | –     |
| X1GND04    | Serdes1 transceiver GND | AG16               | –        | –            | –     |
| X1GND05    | Serdes1 transceiver GND | AG13               | –        | –            | –     |
| X1GND06    | Serdes1 transceiver GND | AF24               | –        | –            | –     |
| X1GND07    | Serdes1 transceiver GND | AF22               | –        | –            | –     |
| X1GND08    | Serdes1 transceiver GND | AF20               | –        | –            | –     |
| X1GND09    | Serdes1 transceiver GND | AF19               | –        | –            | –     |
| X1GND10    | Serdes1 transceiver GND | AF17               | –        | –            | –     |
| X1GND11    | Serdes1 transceiver GND | AF15               | –        | –            | –     |
| X1GND12    | Serdes1 transceiver GND | AF14               | –        | –            | –     |
| X1GND13    | Serdes1 transceiver GND | AE24               | –        | –            | –     |
| X1GND14    | Serdes1 transceiver GND | AE22               | –        | –            | –     |
| X1GND15    | Serdes1 transceiver GND | AE20               | –        | –            | –     |
| X1GND16    | Serdes1 transceiver GND | AE19               | –        | –            | –     |
| X1GND17    | Serdes1 transceiver GND | AE17               | –        | –            | –     |
| X1GND18    | Serdes1 transceiver GND | AD22               | –        | –            | –     |
| X1GND19    | Serdes1 transceiver GND | AD17               | –        | –            | –     |
| X1GND20    | Serdes1 transceiver GND | AC23               | –        | –            | –     |
| X1GND21    | Serdes1 transceiver GND | AC21               | –        | –            | –     |
| X1GND22    | Serdes1 transceiver GND | AB21               | –        | –            | –     |
| S1GND01    | Serdes core logic GND   | AK26               | –        | –            | –     |
| S1GND02    | Serdes core logic GND   | AK24               | –        | –            | –     |
| S1GND03    | Serdes core logic GND   | AK22               | –        | –            | –     |
| S1GND04    | Serdes core logic GND   | AK21               | –        | –            | –     |
| S1GND05    | Serdes core logic GND   | AK19               | –        | –            | –     |
| S1GND06    | Serdes core logic GND   | AK18               | –        | –            | –     |



**Table 2-1.** Pinout list by bus (Continued)

| Signal  | Signal description      | Package pin number | Pin type | Power supply | Notes |
|---------|-------------------------|--------------------|----------|--------------|-------|
| S1GND07 | Serdes core logic GND   | AK16               | –        | –            | –     |
| S1GND08 | Serdes core logic GND   | AK14               | –        | –            | –     |
| S1GND09 | Serdes core logic GND   | AK12               | –        | –            | –     |
| S1GND10 | Serdes core logic GND   | AJ26               | –        | –            | –     |
| S1GND11 | Serdes core logic GND   | AJ24               | –        | –            | –     |
| S1GND12 | Serdes core logic GND   | AJ22               | –        | –            | –     |
| S1GND13 | Serdes core logic GND   | AJ21               | –        | –            | –     |
| S1GND14 | Serdes core logic GND   | AJ19               | –        | –            | –     |
| S1GND15 | Serdes core logic GND   | AJ18               | –        | –            | –     |
| S1GND16 | Serdes core logic GND   | AJ16               | –        | –            | –     |
| S1GND17 | Serdes core logic GND   | AJ14               | –        | –            | –     |
| S1GND18 | Serdes core logic GND   | AJ12               | –        | –            | –     |
| S1GND19 | Serdes core logic GND   | AH25               | –        | –            | –     |
| S1GND20 | Serdes core logic GND   | AH22               | –        | –            | –     |
| S1GND21 | Serdes core logic GND   | AH19               | –        | –            | –     |
| S1GND22 | Serdes core logic GND   | AH16               | –        | –            | –     |
| S1GND23 | Serdes core logic GND   | AH15               | –        | –            | –     |
| S1GND24 | Serdes core logic GND   | AH14               | –        | –            | –     |
| S1GND25 | Serdes core logic GND   | AC20               | –        | –            | –     |
| S1GND26 | Serdes core logic GND   | AC19               | –        | –            | –     |
| S1GND27 | Serdes core logic GND   | AC18               | –        | –            | –     |
| S1GND28 | Serdes core logic GND   | AC17               | –        | –            | –     |
| S1GND29 | Serdes core logic GND   | AC16               | –        | –            | –     |
| S1GND30 | Serdes core logic GND   | AB18               | –        | –            | –     |
| S1GND31 | Serdes core logic GND   | AA21               | –        | –            | –     |
| S1GND32 | Serdes core logic GND   | AA20               | –        | –            | –     |
| S1GND33 | Serdes core logic GND   | AA19               | –        | –            | –     |
| S1GND34 | Serdes core logic GND   | AA18               | –        | –            | –     |
| S1GND35 | Serdes core logic GND   | AA17               | –        | –            | –     |
| X2GND01 | Serdes1 transceiver GND | AJ2                | –        | –            | –     |
| X2GND02 | Serdes1 transceiver GND | AJ1                | –        | –            | –     |
| X2GND03 | Serdes1 transceiver GND | AG12               | –        | –            | –     |
| X2GND04 | Serdes1 transceiver GND | AG10               | –        | –            | –     |
| X2GND05 | Serdes1 transceiver GND | AG7                | –        | –            | –     |
| X2GND06 | Serdes1 transceiver GND | AG4                | –        | –            | –     |
| X2GND07 | Serdes1 transceiver GND | AG2                | –        | –            | –     |
| X2GND08 | Serdes1 transceiver GND | AG1                | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal  | Signal description      | Package pin number | Pin type | Power supply | Notes |
|---------|-------------------------|--------------------|----------|--------------|-------|
| X2GND09 | Serdes1 transceiver GND | AF12               | –        | –            | –     |
| X2GND10 | Serdes1 transceiver GND | AF10               | –        | –            | –     |
| X2GND11 | Serdes1 transceiver GND | AF7                | –        | –            | –     |
| X2GND12 | Serdes1 transceiver GND | AF4                | –        | –            | –     |
| X2GND13 | Serdes1 transceiver GND | AF3                | –        | –            | –     |
| X2GND14 | Serdes1 transceiver GND | AE9                | –        | –            | –     |
| X2GND15 | Serdes1 transceiver GND | AE8                | –        | –            | –     |
| X2GND16 | Serdes1 transceiver GND | AE7                | –        | –            | –     |
| X2GND17 | Serdes1 transceiver GND | AE4                | –        | –            | –     |
| X2GND18 | Serdes1 transceiver GND | AD11               | –        | –            | –     |
| X2GND19 | Serdes1 transceiver GND | AD10               | –        | –            | –     |
| X2GND20 | Serdes1 transceiver GND | AA7                | –        | –            | –     |
| X2GND21 | Serdes1 transceiver GND | AA6                | –        | –            | –     |
| X2GND22 | Serdes1 transceiver GND | AA5                | –        | –            | –     |
| X2GND23 | Serdes1 transceiver GND | AA2                | –        | –            | –     |
| X2GND24 | Serdes1 transceiver GND | AA1                | –        | –            | –     |
| X2GND25 | Serdes1 transceiver GND | Y4                 | –        | –            | –     |
| X2GND26 | Serdes1 transceiver GND | Y3                 | –        | –            | –     |
| S2GND01 | Serdes core logic GND   | AK10               | –        | –            | –     |
| S2GND02 | Serdes core logic GND   | AK7                | –        | –            | –     |
| S2GND03 | Serdes core logic GND   | AK4                | –        | –            | –     |
| S2GND04 | Serdes core logic GND   | AK2                | –        | –            | –     |
| S2GND05 | Serdes core logic GND   | AJ10               | –        | –            | –     |
| S2GND06 | Serdes core logic GND   | AJ7                | –        | –            | –     |
| S2GND07 | Serdes core logic GND   | AJ4                | –        | –            | –     |
| S2GND08 | Serdes core logic GND   | AH11               | –        | –            | –     |
| S2GND09 | Serdes core logic GND   | AH9                | –        | –            | –     |
| S2GND10 | Serdes core logic GND   | AH8                | –        | –            | –     |
| S2GND11 | Serdes core logic GND   | AH6                | –        | –            | –     |
| S2GND12 | Serdes core logic GND   | AH5                | –        | –            | –     |
| S2GND13 | Serdes core logic GND   | AH3                | –        | –            | –     |
| S2GND14 | Serdes core logic GND   | AE6                | –        | –            | –     |
| S2GND15 | Serdes core logic GND   | AE5                | –        | –            | –     |
| S2GND16 | Serdes core logic GND   | AE2                | –        | –            | –     |
| S2GND17 | Serdes core logic GND   | AE1                | –        | –            | –     |
| S2GND18 | Serdes core logic GND   | AD15               | –        | –            | –     |
| S2GND19 | Serdes core logic GND   | AD8                | –        | –            | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal        | Signal description    | Package pin number | Pin type | Power supply     | Notes |
|---------------|-----------------------|--------------------|----------|------------------|-------|
| S2GND20       | Serdes core logic GND | AD7                | —        | —                | —     |
| S2GND21       | Serdes core logic GND | AD4                | —        | —                | —     |
| S2GND22       | Serdes core logic GND | AD3                | —        | —                | —     |
| S2GND23       | Serdes core logic GND | AC14               | —        | —                | —     |
| S2GND24       | Serdes core logic GND | AC13               | —        | —                | —     |
| S2GND25       | Serdes core logic GND | AC12               | —        | —                | —     |
| S2GND26       | Serdes core logic GND | AC11               | —        | —                | —     |
| S2GND27       | Serdes core logic GND | AC10               | —        | —                | —     |
| S2GND28       | Serdes core logic GND | AC9                | —        | —                | —     |
| S2GND29       | Serdes core logic GND | AC6                | —        | —                | —     |
| S2GND30       | Serdes core logic GND | AC5                | —        | —                | —     |
| S2GND31       | Serdes core logic GND | AC2                | —        | —                | —     |
| S2GND32       | Serdes core logic GND | AC1                | —        | —                | —     |
| S2GND33       | Serdes core logic GND | AB12               | —        | —                | —     |
| S2GND34       | Serdes core logic GND | AB9                | —        | —                | —     |
| S2GND35       | Serdes core logic GND | AB8                | —        | —                | —     |
| S2GND36       | Serdes core logic GND | AB7                | —        | —                | —     |
| S2GND37       | Serdes core logic GND | AB4                | —        | —                | —     |
| S2GND38       | Serdes core logic GND | AB3                | —        | —                | —     |
| S2GND39       | Serdes core logic GND | AA16               | —        | —                | —     |
| S2GND40       | Serdes core logic GND | AA14               | —        | —                | —     |
| S2GND41       | Serdes core logic GND | AA13               | —        | —                | —     |
| S2GND42       | Serdes core logic GND | AA12               | —        | —                | —     |
| S2GND43       | Serdes core logic GND | AA11               | —        | —                | —     |
| S2GND44       | Serdes core logic GND | AA10               | —        | —                | —     |
| AGND_SD1_PLL1 | Serdes 1 PLL 1 GND    | AB16               | —        | —                | —     |
| AGND_SD1_PLL2 | Serdes 1 PLL 2 GND    | AB19               | —        | —                | —     |
| AGND_SD2_PLL1 | Serdes 2 PLL 1 GND    | AB10               | —        | —                | —     |
| AGND_SD2_PLL2 | Serdes 2 PLL 2 GND    | AB13               | —        | —                | —     |
| SENSEGND      | GND Sense pin         | K21                | —        | —                | —     |
| OVDD01        | General I/O supply    | L8                 | —        | OV <sub>DD</sub> | —     |
| OVDD02        | General I/O supply    | K20                | —        | OV <sub>DD</sub> | —     |
| OVDD03        | General I/O supply    | K19                | —        | OV <sub>DD</sub> | —     |
| OVDD04        | General I/O supply    | K18                | —        | OV <sub>DD</sub> | —     |
| OVDD05        | General I/O supply    | K17                | —        | OV <sub>DD</sub> | —     |
| OVDD06        | General I/O supply    | K16                | —        | OV <sub>DD</sub> | —     |
| OVDD07        | General I/O supply    | K15                | —        | OV <sub>DD</sub> | —     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal  | Signal description                                 | Package pin number | Pin type | Power supply      | Notes |
|---------|--|--------------------|----------|-------------------|-------|
| OVDD08  | General I/O supply                                 | K14                | –        | OV <sub>DD</sub>  | –     |
| OVDD09  | General I/O supply                                 | K13                | –        | OV <sub>DD</sub>  | –     |
| OVDD10  | General I/O supply                                 | K12                | –        | OV <sub>DD</sub>  | –     |
| OVDD11  | General I/O supply                                 | K8                 | –        | OV <sub>DD</sub>  | –     |
| DVDD1   | UART/I2C/DMA supply                                | P8                 | –        | DV <sub>DD</sub>  | –     |
| DVDD2   | UART/I2C/DMA supply                                | N8                 | –        | DV <sub>DD</sub>  | –     |
| CVDD1   | eSPI supply  | M8                 | –        | CV <sub>DD</sub>  | –     |
| CVDD2   | eSPI supply  | M6                 | –        | CV <sub>DD</sub>  | –     |
| LVDD1   | Ethernet controllers (RGMII), EMI2 and GPIO supply | V8                 | –        | LV <sub>DD</sub>  | –     |
| LVDD2   | Ethernet controllers (RGMII), EMI2 and GPIO supply | U8                 | –        | LV <sub>DD</sub>  | –     |
| LVDD3   | Ethernet controllers (RGMII), EMI2 and GPIO supply | T8                 | –        | LV <sub>DD</sub>  | –     |
| G1VDD01 | DDR supply   | AK29               | –        | G1V <sub>DD</sub> | –     |
| G1VDD02 | DDR supply   | AJ30               | –        | G1V <sub>DD</sub> | –     |
| G1VDD03 | DDR supply   | AF29               | –        | G1V <sub>DD</sub> | –     |
| G1VDD04 | DDR supply   | AD29               | –        | G1V <sub>DD</sub> | –     |
| G1VDD05 | DDR supply   | AB29               | –        | G1V <sub>DD</sub> | –     |
| G1VDD06 | DDR supply   | Y29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD07 | DDR supply   | V29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD08 | DDR supply   | V22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD09 | DDR supply   | U22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD10 | DDR supply   | T30                | –        | G1V <sub>DD</sub> | –     |
| G1VDD11 | DDR supply   | T29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD12 | DDR supply   | T22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD13 | DDR supply   | R22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD14 | DDR supply   | P29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD15 | DDR supply   | P22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD16 | DDR supply   | N22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD17 | DDR supply   | M29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD18 | DDR supply   | M22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD19 | DDR supply   | L22                | –        | G1V <sub>DD</sub> | –     |
| G1VDD20 | DDR supply   | K29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD21 | DDR supply   | H29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD22 | DDR supply   | F29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD23 | DDR supply   | D29                | –        | G1V <sub>DD</sub> | –     |
| G1VDD24 | DDR supply   | B30                | –        | G1V <sub>DD</sub> | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal   | Signal description                        | Package pin number | Pin type | Power supply       | Notes |
|----------|---|--------------------|----------|--------------------|-------|
| G1VDD25  | DDR supply                                | A29                | –        | G1V <sub>DD</sub>  | –     |
| S1VDD1   | SerDes1 core logic supply                 | Y21                | –        | S1V <sub>DD</sub>  | –     |
| S1VDD2   | SerDes1 core logic supply                 | Y20                | –        | S1V <sub>DD</sub>  | –     |
| S1VDD3   | SerDes1 core logic supply                 | Y19                | –        | S1V <sub>DD</sub>  | –     |
| S1VDD4   | SerDes1 core logic supply                 | Y18                | –        | S1V <sub>DD</sub>  | –     |
| S1VDD5   | SerDes1 core logic supply                 | Y17                | –        | S1V <sub>DD</sub>  | –     |
| S1VDD6   | SerDes1 core logic supply                 | Y16                | –        | S1V <sub>DD</sub>  | –     |
| S2VDD1   | SerDes1 core logic supply                 | AA9                | –        | S2V <sub>DD</sub>  | –     |
| S2VDD2   | SerDes1 core logic supply                 | Y15                | –        | S2V <sub>DD</sub>  | –     |
| S2VDD3   | SerDes1 core logic supply                 | Y14                | –        | S2V <sub>DD</sub>  | –     |
| S2VDD4   | SerDes1 core logic supply                 | Y13                | –        | S2V <sub>DD</sub>  | –     |
| S2VDD5   | SerDes1 core logic supply                 | Y12                | –        | S2V <sub>DD</sub>  | –     |
| S2VDD6   | SerDes1 core logic supply                 | Y11                | –        | S2V <sub>DD</sub>  | –     |
| X1VDD1   | SerDes1 transceiver supply                | AG24               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD2   | SerDes1 transceiver supply                | AG22               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD3   | SerDes1 transceiver supply                | AG20               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD4   | SerDes1 transceiver supply                | AG19               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD5   | SerDes1 transceiver supply                | AG17               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD6   | SerDes1 transceiver supply                | AD16               | –        | X1V <sub>DD</sub>  | –     |
| X1VDD7   | SerDes1 transceiver supply                | AB22               | –        | X1V <sub>DD</sub>  | –     |
| X2VDD1   | SerDes1 transceiver supply                | AH10               | –        | X2V <sub>DD</sub>  | –     |
| X2VDD2   | SerDes1 transceiver supply                | AH7                | –        | X2V <sub>DD</sub>  | –     |
| X2VDD3   | SerDes1 transceiver supply                | AH4                | –        | X2V <sub>DD</sub>  | –     |
| X2VDD4   | SerDes1 transceiver supply                | AG3                | –        | X2V <sub>DD</sub>  | –     |
| X2VDD5   | SerDes1 transceiver supply                | AE11               | –        | X2V <sub>DD</sub>  | –     |
| X2VDD6   | SerDes1 transceiver supply                | AE3                | –        | X2V <sub>DD</sub>  | –     |
| FA_VL    | Reserved for internal use only            | H20                | –        | FA_VL              | (15)  |
| PROG_MTR | Reserved for internal use only            | E8                 | –        | PROG_MTR           | (15)  |
| PROG_SFP | Security Fuse Programming Override supply | E9                 | –        | PROG_SFP           | –     |
| TH_VDD   | Thermal Monitor Unit supply               | K10                | –        | TH_V <sub>DD</sub> | –     |
| VDD01    | Supply for cores and platform             | Y10                | –        | V <sub>DD</sub>    | –     |
| VDD02    | Supply for cores and platform             | W21                | –        | V <sub>DD</sub>    | –     |
| VDD03    | Supply for cores and platform             | W19                | –        | V <sub>DD</sub>    | –     |
| VDD04    | Supply for cores and platform             | W17                | –        | V <sub>DD</sub>    | –     |
| VDD05    | Supply for cores and platform             | W15                | –        | V <sub>DD</sub>    | –     |
| VDD06    | Supply for cores and platform             | W13                | –        | V <sub>DD</sub>    | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal | Signal description            | Package pin number | Pin type | Power supply    | Notes |
|--------|-------------------------------|--------------------|----------|-----------------|-------|
| VDD07  | Supply for cores and platform | W11                | –        | V <sub>DD</sub> | –     |
| VDD08  | Supply for cores and platform | W9                 | –        | V <sub>DD</sub> | –     |
| VDD09  | Supply for cores and platform | V20                | –        | V <sub>DD</sub> | –     |
| VDD10  | Supply for cores and platform | V18                | –        | V <sub>DD</sub> | –     |
| VDD11  | Supply for cores and platform | V16                | –        | V <sub>DD</sub> | –     |
| VDD12  | Supply for cores and platform | V14                | –        | V <sub>DD</sub> | –     |
| VDD13  | Supply for cores and platform | V12                | –        | V <sub>DD</sub> | –     |
| VDD14  | Supply for cores and platform | V10                | –        | V <sub>DD</sub> | –     |
| VDD15  | Supply for cores and platform | U21                | –        | V <sub>DD</sub> | –     |
| VDD16  | Supply for cores and platform | U19                | –        | V <sub>DD</sub> | –     |
| VDD17  | Supply for cores and platform | U17                | –        | V <sub>DD</sub> | –     |
| VDD18  | Supply for cores and platform | U15                | –        | V <sub>DD</sub> | –     |
| VDD19  | Supply for cores and platform | U13                | –        | V <sub>DD</sub> | –     |
| VDD20  | Supply for cores and platform | U11                | –        | V <sub>DD</sub> | –     |
| VDD21  | Supply for cores and platform | U9                 | –        | V <sub>DD</sub> | –     |
| VDD22  | Supply for cores and platform | T20                | –        | V <sub>DD</sub> | –     |
| VDD23  | Supply for cores and platform | T18                | –        | V <sub>DD</sub> | –     |
| VDD24  | Supply for cores and platform | T16                | –        | V <sub>DD</sub> | –     |
| VDD25  | Supply for cores and platform | T14                | –        | V <sub>DD</sub> | –     |
| VDD26  | Supply for cores and platform | T12                | –        | V <sub>DD</sub> | –     |
| VDD27  | Supply for cores and platform | T10                | –        | V <sub>DD</sub> | –     |
| VDD28  | Supply for cores and platform | R21                | –        | V <sub>DD</sub> | –     |
| VDD29  | Supply for cores and platform | R19                | –        | V <sub>DD</sub> | –     |
| VDD30  | Supply for cores and platform | R17                | –        | V <sub>DD</sub> | –     |
| VDD31  | Supply for cores and platform | R15                | –        | V <sub>DD</sub> | –     |
| VDD32  | Supply for cores and platform | R13                | –        | V <sub>DD</sub> | –     |
| VDD33  | Supply for cores and platform | R11                | –        | V <sub>DD</sub> | –     |
| VDD34  | Supply for cores and platform | R9                 | –        | V <sub>DD</sub> | –     |
| VDD35  | Supply for cores and platform | P20                | –        | V <sub>DD</sub> | –     |
| VDD36  | Supply for cores and platform | P18                | –        | V <sub>DD</sub> | –     |
| VDD37  | Supply for cores and platform | P16                | –        | V <sub>DD</sub> | –     |
| VDD38  | Supply for cores and platform | P14                | –        | V <sub>DD</sub> | –     |
| VDD39  | Supply for cores and platform | P12                | –        | V <sub>DD</sub> | –     |
| VDD40  | Supply for cores and platform | P10                | –        | V <sub>DD</sub> | –     |
| VDD41  | Supply for cores and platform | N21                | –        | V <sub>DD</sub> | –     |
| VDD42  | Supply for cores and platform | N19                | –        | V <sub>DD</sub> | –     |
| VDD43  | Supply for cores and platform | N17                | –        | V <sub>DD</sub> | –     |

**Table 2-1.** Pinout list by bus (Continued)

| Signal                    | Signal description                | Package pin number | Pin type | Power supply         | Notes |
|---------------------------|-----------------------------------|--------------------|----------|----------------------|-------|
| VDD44                     | Supply for cores and platform     | N15                | –        | V <sub>DD</sub>      | –     |
| VDD45                     | Supply for cores and platform     | N13                | –        | V <sub>DD</sub>      | –     |
| VDD46                     | Supply for cores and platform     | N11                | –        | V <sub>DD</sub>      | –     |
| VDD47                     | Supply for cores and platform     | N9                 | –        | V <sub>DD</sub>      | –     |
| VDD48                     | Supply for cores and platform     | M20                | –        | V <sub>DD</sub>      | –     |
| VDD49                     | Supply for cores and platform     | M18                | –        | V <sub>DD</sub>      | –     |
| VDD50                     | Supply for cores and platform     | M16                | –        | V <sub>DD</sub>      | –     |
| VDD51                     | Supply for cores and platform     | M14                | –        | V <sub>DD</sub>      | –     |
| VDD52                     | Supply for cores and platform     | M12                | –        | V <sub>DD</sub>      | –     |
| VDD53                     | Supply for cores and platform     | M10                | –        | V <sub>DD</sub>      | –     |
| VDD54                     | Supply for cores and platform     | L21                | –        | V <sub>DD</sub>      | –     |
| VDD55                     | Supply for cores and platform     | L19                | –        | V <sub>DD</sub>      | –     |
| VDD56                     | Supply for cores and platform     | L17                | –        | V <sub>DD</sub>      | –     |
| VDD57                     | Supply for cores and platform     | L15                | –        | V <sub>DD</sub>      | –     |
| VDD58                     | Supply for cores and platform     | L13                | –        | V <sub>DD</sub>      | –     |
| VDD59                     | Supply for cores and platform     | L11                | –        | V <sub>DD</sub>      | –     |
| VDD60                     | Supply for cores and platform     | L9                 | –        | V <sub>DD</sub>      | –     |
| VDD_LP                    | Low Power Security Monitor supply | R8                 | –        | V <sub>DD_LP</sub>   | –     |
| AVDD_CGA1                 | e6500 Cluster Group A PLL1 supply | H9                 | –        | AVDD_CGA1            | –     |
| AVDD_CGA2                 | e6500 Cluster Group A PLL2 supply | G9                 | –        | AVDD_CGA2            | –     |
| AVDD_PLAT                 | Platform PLL supply               | J10                | –        | AVDD_PLAT            | –     |
| AVDD_D1                   | DDR1 PLL supply                   | F22                | –        | AVDD_D1              | –     |
| AVDD_SD1_PLL1             | SerDes 1 PLL 1 supply             | AB17               | –        | AVDD_SD1_PLL1        | –     |
| AVDD_SD1_PLL2             | SerDes 1 PLL 2 supply             | AB20               | –        | AVDD_SD1_PLL2        | –     |
| AVDD_SD2_PLL1             | SerDes 2 PLL 1 supply             | AB11               | –        | AVDD_SD2_PLL1        | –     |
| AVDD_SD2_PLL2             | SerDes 2 PLL 2 supply             | AB14               | –        | AVDD_SD2_PLL2        | –     |
| SENSEVDD                  | Vdd Sense pin                     | J20                | –        | SENSEVDD             | –     |
| USB_HVDD1                 | USB PHY Transceiver 3.3V Supply   | C8                 | –        | USB_HV <sub>DD</sub> | –     |
| USB_HVDD2                 | USB PHY Transceiver 3.3V Supply   | A7                 | –        | USB_HV <sub>DD</sub> | –     |
| USB_OVDD1                 | USB PHY Transceiver 1.8V Supply   | J8                 | –        | USB_OV <sub>DD</sub> | –     |
| USB_OVDD2                 | USB PHY Transceiver 1.8V Supply   | J7                 | –        | USB_OV <sub>DD</sub> | –     |
| USB_SVDD1                 | USB PHY Analog 1.0V Supply        | G7                 | –        | USB_SV <sub>DD</sub> | –     |
| USB_SVDD2                 | USB PHY Analog 1.0V Supply        | F6                 | –        | USB_SV <sub>DD</sub> | –     |
| <b>No Connection Pins</b> |                                   |                    |          |                      |       |
| NC_AB15                   | No Connection                     | AB15               | –        | –                    | (12)  |
| NC_AC15                   | No Connection                     | AC15               | –        | –                    | (12)  |
| NC_AD12                   | No Connection                     | AD12               | –        | –                    | (12)  |

**Table 2-1.** Pinout list by bus (Continued)

| Signal  | Signal description | Package pin number | Pin type | Power supply | Notes |
|---------|--------------------|--------------------|----------|--------------|-------|
| NC_AD13 | No Connection      | AD13               | —        | —            | (12)  |
| NC_AD14 | No Connection      | AD14               | —        | —            | (12)  |
| NC_AD9  | No Connection      | AD9                | —        | —            | (12)  |
| NC_AE12 | No Connection      | AE12               | —        | —            | (12)  |
| NC_AE13 | No Connection      | AE13               | —        | —            | (12)  |
| NC_AF13 | No Connection      | AF13               | —        | —            | (12)  |

- Notes:
- Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
  - This output is actively driven during reset rather than being tri-stated during reset.
  - MDIC[0] is grounded through a 187 $\Omega$  precision 1% resistor and MDIC[1] is connected to GV<sub>DD</sub> through a 187 $\Omega$  precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 187 $\Omega$ . Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3/DDR3L IOs. The MDIC[0:1] pins must be connected to 187 $\Omega$  precision 1% resistors.
  - This pin is a reset configuration pin. It has a weak (~20 k $\Omega$ ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 k $\Omega$  resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.
  - Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
  - Recommend that a weak pull-up resistor (4.7 k $\Omega$ ) be placed on this pin to the respective power supply.
  - This pin is an open-drain signal.
  - Recommend that a weak pull-up resistor (1 k $\Omega$ ) be placed on this pin to the respective power supply.
  - This pin has a weak (~20 k $\Omega$ ) internal pull-up P-FET that is always enabled.
  - This is a test signal for factory use only and must be pulled up (100 $\Omega$  to 1-k $\Omega$ ) to the respective power supply for normal operation.
  - This pin requires a 200 $\Omega$  pull-up to respective power-supply.
  - Do not connect. This pin should be left floating.
  - These pins must be pulled up to 1.2V through a 180 $\Omega \pm 1\%$  resistor for MDC and a 330 $\Omega \pm 1\%$  resistor for MDIO.
  - This pin requires an external 1-k $\Omega$  pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
  - Must be pulled to ground (GND).
  - This pin requires a 698 $\Omega$  pull-up to respective power-supply.
  - This pin should be tied to ground if the diode is not utilized for temperature monitoring.
  - If used as an SDHC signal, pull up 10k $\Omega$  to 100k $\Omega$  to the respective IO supply.
  - New board designs should leave a placeholder for a parallel series resistor and capacitor filter to be used in very close proximity to the USB\_IBAIS\_REXT pin of TELEDYNE e2v QorIQ chips. When needed, this allows for flexibility in populating them, which helps avoid board-coupled noise to this pin. A 100nF low-ESL SMD ceramic chip capacitor in series with a 100 $\Omega$  SMD resistor performs the needed filtration with slight variations that suit each board case.



## Warning

See "Section 4.5 "Connection recommendations" on page 139" for additional details on properly connecting these pins for specific applications.

## 3. ELECTRICAL CHARACTERISTICS

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

### 3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

#### 3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

**Table 3-1.** Absolute maximum ratings<sup>(1)</sup>

| Characteristic  | Symbol   | Max Value                    | Unit | Notes |
|---|--|------------------------------|------|-------|
| Core and platform supply voltage  | $V_{DD}$   | –0.3 to 1.1                  | V    | (2)   |
| PLL supply voltage (core, platform, DDR)  | $AV_{DD\_CGA1}$<br>$AV_{DD\_CGA2}$<br>$AV_{DD\_PLAT}$<br>$AV_{DD\_D1}$ | –0.3 to 1.98                 | V    | –     |
| PLL supply voltage (SerDes, filtered from $XnV_{DD}$ )  | $AV_{DD\_SDn\_PLLn}$   | –0.3 to 1.48                 | V    | –     |
| Fuse programming override supply  | PROG_SFP   | –0.3 to 1.98                 | V    | –     |
| Thermal monitor unit supply   | TH_ $V_{DD}$   | –0.3 to 1.98                 | V    | –     |
| eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage | OV_ $V_{DD}$   | –0.3 to 1.98                 | V    | –     |
| eSPI  | CV_ $V_{DD}$   | –0.3 to 2.75<br>–0.3 to 1.98 | V    | –     |
| DMA, DUART, I <sup>2</sup> C I/O voltage  | DV_ $V_{DD}$   | –0.3 to 2.75<br>–0.3 to 1.98 | V    | –     |
| DDR3 and DDR3L DRAM I/O voltage   | G1V_ $V_{DD}$  | –0.3 to 1.65<br>–0.3 to 1.45 | V    | –     |
| Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers                      | SnV_ $V_{DD}$  | –0.3 to 1.1                  | V    | –     |
| Pad power supply for SerDes transmitters  | XnV_ $V_{DD}$  | –0.3 to 1.45                 | V    | –     |
| Ethernet I/O, Ethernet management interface 1 (EMI1) 1588, GPIO I/O voltage                                       | LV_ $V_{DD}$   | –0.3 to 2.75                 | V    | –     |
|   |  | –0.3 to 1.98                 |      |       |
| Ethernet management interface 2 (EMI2) I/O voltage  | –  | –0.3 to 1.32                 | V    | (4)   |
| USB PHY Transceiver supply voltage  | USB_ $HV_{DD}$   | –0.3 to 3.63                 | V    | –     |
|   | USB_ $OV_{DD}$   | –0.3 to 1.98                 | V    | –     |
| USB PHY Analog supply voltage   | USB_ $SV_{DD}$   | –0.3 to 1.1                  | V    | –     |
| Low Power Security Monitor supply   | $V_{DD\_LP}$   | –0.3 to 1.1                  | V    | –     |

**Table 3-1.** Absolute maximum ratings<sup>(1)</sup> (Continued)

| Characteristic            |   | Symbol                | Max Value                            | Unit | Notes  |
|---------------------------|---|-----------------------|--------------------------------------|------|--------|
| Input voltage             | DDR3 and DDR3L DRAM signals   | MV <sub>IN</sub>      | −0.3 to (GV <sub>DD</sub> + 0.3)     | V    | (5)    |
|                           | DDR3 and DDR3L DRAM reference   | D1_MV <sub>REF</sub>  | −0.3 to (GV <sub>DD</sub> /2+0.3)    | V    | (6)    |
|                           | Ethernet signals (except EMI2)  | LV <sub>IN</sub>      | −0.3 to (LV <sub>DD</sub> + 0.3)     | V    | (6)(7) |
|                           | eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG signals | OV <sub>IN</sub>      | −0.3 to (OV <sub>DD</sub> + 0.3)     | V    | (6)(8) |
|                           | eSPI  | CV <sub>IN</sub>      | −0.3 to (CV <sub>DD</sub> + 0.3)     | V    | (6)(8) |
|                           | DMA, DUART, I <sup>2</sup> C signals  | DV <sub>IN</sub>      | −0.3 to (DV <sub>DD</sub> + 0.3)     | V    | (8)(9) |
|                           | SerDes signals  | SVI <sub>IN</sub>     | −0.4 to (SV <sub>DD</sub> + 0.3)     | V    | (6)    |
|                           | USB PHY Transceiver signals   | USB_HV <sub>IN</sub>  | −0.3 to (USB_HV <sub>DD</sub> + 0.3) | V    | (6)    |
|                           |   | USB_OVI <sub>IN</sub> | −0.3 to (USB_OV <sub>DD</sub> + 0.3) | V    | (6)    |
|                           | Ethernet management interface 2 signals   | —                     | −0.3 to (1.2 + 0.3)                  | V    | —      |
| Storage temperature range |   | T <sub>STG</sub>      | −55 to 150                           | °C   | —      |

- Notes:
- Functional operating conditions are given in [Table 3-2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
  - Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
  - 
  - Ethernet MII management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels.
  - Caution:** MV<sub>IN</sub> must not exceed GV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
  - C, S, G, L, O, D) V<sub>IN</sub>, USBn\_V<sub>IN</sub>\_3P3, USBn\_V<sub>IN</sub>\_1P8 and D1\_MV<sub>REF</sub> may overshoot/undershoot to a voltage and for a maximum duration as shown in [Figure 3-1](#).
  - Caution:** LV<sub>IN</sub> must not exceed LV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
  - Caution:** CV<sub>IN</sub> and OV<sub>IN</sub> must not exceed CV<sub>DD</sub> and OV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
  - Caution:** DV<sub>IN</sub> must not exceed DV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

## 3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

### NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

**Table 3-2.** Recommended operating conditions

| Characteristic  |                         | Symbol   | Recommended Value   | Unit | Notes        |
|---|-------------------------|--|---|------|--------------|
| Core and platform supply voltage  | At initial start-up     | $V_{DD}$   | $1.025 \pm 30 \text{ mV}$   | V    | (1)(2)(3)(7) |
|   | During normal operation |  | $VID \pm 30 \text{ mV}$   | V    | (1)(2)(3)(7) |
| PLL supply voltage (core, platform, DDR)  |                         | $AV_{DD\_CGA1}$<br>$AV_{DD\_CGA2}$<br>$AV_{DD\_PLAT}$<br>$AV_{DD\_D1}$ | $1.8 \text{ V} \pm 90 \text{ mV}$                                       | V    | (8)          |
| PLL supply voltage (SerDes, filtered from $XnV_{DD}$ )  |                         | $AV_{DD\_SDn\_PLLn}$ (n = 1 or 2)                                      | $1.35 \text{ V} \pm 67 \text{ mV}$                                      | V    | —            |
| Fuse programming override supply  |                         | PROG_SFP   | $1.80 \text{ V} \pm 90 \text{ mV}$                                      | V    | (4)          |
| Thermal monitor unit supply   |                         | TH_ $V_{DD}$   | $1.8 \text{ V} \pm 90 \text{ mV}$                                       | V    | —            |
| eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage |                         | OV $_{DD}$   | $1.8 \text{ V} \pm 90 \text{ mV}$                                       | V    | —            |
| eSPI  |                         | CV $_{DD}$   | $2.5 \text{ V} \pm 125 \text{ mV}$<br>$1.8 \text{ V} \pm 90 \text{ mV}$ | V    | —            |
| DMA, DUART, I <sup>2</sup> C I/O voltage  |                         | DV $_{DD}$   | $2.5 \text{ V} \pm 125 \text{ mV}$<br>$1.8 \text{ V} \pm 90 \text{ mV}$ | V    | —            |
| DDR DRAM I/O voltage  | DDR3                    | G1V $_{DD}$  | $1.5 \text{ V} \pm 75 \text{ mV}$                                       | V    | —            |
|   | DDR3L                   |  | $1.35 \text{ V} \pm 67 \text{ mV}$                                      |      |              |
| Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers                      |                         | SnV $_{DD}$ (n = 1 or 2)   | $1.0 \text{ V} \pm 50 \text{ mV}$<br>$1.0 \text{ V} - 30 \text{ mV}$    | V    | —            |
| Pad power supply for SerDes transmitters  |                         | XnV $_{DD}$ (n = 1 or 2)   | $1.35 \text{ V} \pm 67 \text{ mV}$                                      | V    | —            |
| Ethernet, Ethernet management interface 1 (EMI1), 1588, GPIO I/O voltage  |                         | LV $_{DD}$   | $2.5 \text{ V} \pm 125 \text{ mV}$<br>$1.8 \text{ V} \pm 90 \text{ mV}$ | V    | (5)          |
| Ethernet management interface 2 (EMI2) I/O voltage  |                         | —  | $1.2 \text{ V} \pm 60 \text{ mV}$                                       | V    | —            |
| USB PHY Transceiver supply voltage  |                         | USB_HV $_{DD}$   | $3.3 \text{ V} \pm 165 \text{ mV}$                                      | V    | —            |
|   |                         | USB_OV $_{DD}$   | $1.8 \text{ V} \pm 90 \text{ mV}$                                       | V    | —            |
| USB PHY Analog supply voltage   | At initial start-up     | USB_SV $_{DD}$   | $1.025 \pm 30 \text{ mV}$   | V    | (1)(3)       |
|   | During normal operation |  | $VID \pm 30 \text{ mV}$   |      |              |

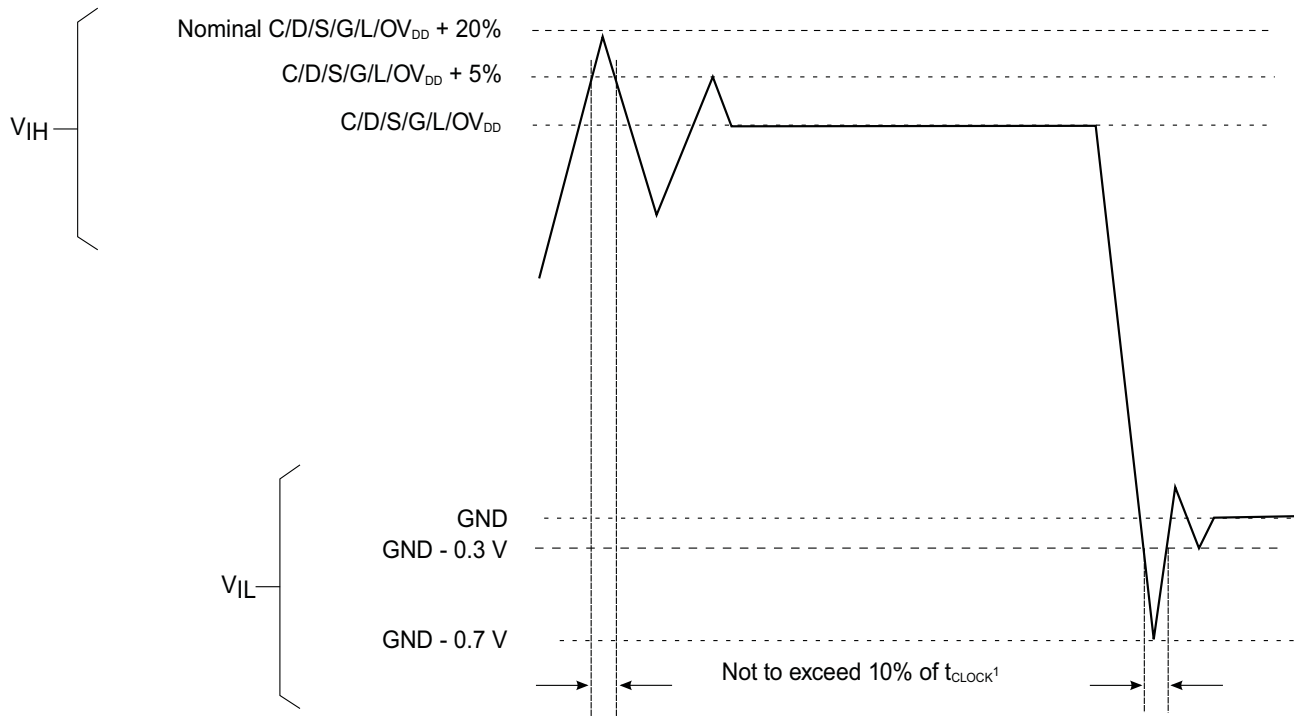
**Table 3-2.** Recommended operating conditions (Continued)

| Characteristic                    |   | Symbol           | Recommended Value                         | Unit | Notes |
|-----------------------------------|---|------------------|---|------|-------|
| Low Power Security Monitor supply |   | $V_{DD\_LP}$     | 1.0 V $\pm$ 50 mV                         | V    | –     |
| Input voltage                     | DDR3 and DDR3L DRAM signals   | $MV_{IN}$        | GND to $GV_{DD}$                          | V    | –     |
|                                   | DDR3 and DDR3L DRAM reference   | $D1\_MV_{REF}$   | $GV_{DD}/2 \pm 1\%$                       | V    | –     |
|                                   | Ethernet signals (except EMI2), USB, 1588, GPIO signals   | $LV_{IN}$        | GND to $LV_{DD}$                          | V    | –     |
|                                   | eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG signals | $OV_{IN}$        | GND to $OV_{DD}$                          | V    | –     |
|                                   | eSPI  | $CV_{IN}$        | GND to $CV_{DD}$                          | V    | –     |
|                                   | DMA, DUART, I <sup>2</sup> C signals  | $DV_{IN}$        | GND to $DV_{DD}$                          | V    | –     |
|                                   | SerDes signals  | $SV_{IN}$        | GND to $SV_{DD}$                          | V    | –     |
|                                   | USB PHY Transceiver signals   | $USB\_HV_{IN}$   | GND to $USB\_HV_{DD}$                     | V    | –     |
|                                   |   | $USB\_OV_{IN}$   | GND to $USB\_OV_{DD}$                     | V    | –     |
|                                   | Ethernet management interface 2 (EMI2) signals  | –                | GND to 1.2V                               | V    | (6)   |
| Operating temperature range       | A range   | $T_C$ ,<br>$T_J$ | $T_C = -40$ (min)<br>to $T_J = 105$ (max) | °C   | –     |
|                                   | F range   | $T_C$ ,<br>$T_J$ | $T_C = -40$ (min)<br>to $T_J = 125$ (max) | °C   | –     |
|                                   | M range   | $T_C$ ,<br>$T_J$ | $T_C = -55$ (min)<br>to $T_J = 125$ (max) | °C   | –     |
|                                   | Secure boot fuse programming  | $T_A$ ,<br>$T_J$ | $T_A = 0$ (min)<br>to $T_J = 70$ (max)    | °C   | (2)   |

- Notes:
1. See Voltage ID (VID) controllable supply and Core and platform supply voltage filtering for additional information.
  2. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
  3. Operation at 1.1 V is allowable for up to 25 ms at initial power on.
  4. PROG\_SFP must be supplied 1.80 V and the chip must operate in the specified fuse programming temperature range (0 - 70°C) only during secure boot fuse programming. For all other operating conditions, PROG\_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.
  5. Selecting RGMII limits to  $LV_{DD} = 2.5$  V.
  6. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels.
  7. Voltage ID (VID) operating range is between 0.975 to 1.025V. Regulator selection should be based on Vout range of at least 0.9 to 1.1 V, with resolution of 12.5 mV or better.
  8. Keep the filter close to the pin. Voltage and tolerance for  $AV_{DD}$  is defined at the input of the PLL supply filter and not the pin of  $AV_{DD}$ .

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

**Figure 3-1.** Overshoot/Undershoot voltage for CVDD/GVDD/LVDD/OVDD/XVDD/DVDD



Note:

$t_{CLOCK}$  refers to the clock period associated with the respective interface:

For I2C ODVDD,  $t_{CLOCK}$  references SYSCLK.

For DDR GVDD,  $t_{CLOCK}$  references Dn\_MCLK.

For eSPI OCVDD,  $t_{CLOCK}$  references SPI\_CLK.

For JTAG OVDD,  $t_{CLOCK}$  references TCK.

For SerDes XVDD,  $t_{CLOCK}$  references SD\_REF\_CLK.

For Ethernet LVDD,  $t_{CLOCK}$  references ECn\_GTX\_CLK125.

The core and platform voltages must always be provided at nominal VID. See [Table 3-2](#) for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in [Table 3-2](#). The input voltage threshold scales with respect to the associated I/O supply voltage. DVDD, OVDD and LVDD based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D1\_MV<sub>REF</sub> signal (nominally set to GVDD/2) as is appropriate for the SSTL\_1.35/SSTL\_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

### 3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

**NOTE**

These values are preliminary estimates.

**Table 3-3.** Output drive capability

| Driver type  | Output impedance ( $\Omega$ ) |  |                        | Supply Voltage                      | Notes |
|--|-------------------------------|--|------------------------|-------------------------------------|-------|
|  | Minimum <sup>(2)</sup>        | Typical  | Maximum <sup>(3)</sup> |                                     |       |
| DDR3 signal  | —                             | 18 (full-strength mode)<br>27 (half-strength mode) | —                      | $G1V_{DD} = 1.5\text{ V}$           | (1)   |
| DDR3L signal   | —                             | 18 (full-strength mode)<br>27 (half-strength mode) | —                      | $G1V_{DD} = 1.35\text{ V}$          | (1)   |
| Ethernet signals   | 45                            | —  | 90                     | $L1V_{DD} / LV_{DD} = 3.3\text{ V}$ | —     |
|  | 40                            | —  | 90                     | $L1V_{DD} / LV_{DD} = 2.5\text{ V}$ |       |
|  | 40                            | —  | 75                     | $L1V_{DD} / LV_{DD} = 1.8\text{ V}$ |       |
| MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage | 23                            | —  | 51                     | $OV_{DD}, O1V_{DD} = 1.8\text{ V}$  | —     |
| DUART, DMA, MPIC, QE, TDM, I <sup>2</sup> C, DIU   | 45                            | —  | 90                     | $DV_{DD} = 3.3\text{ V}$            | —     |
|  | 40                            | —  | 90                     | $DV_{DD} = 2.5\text{ V}$            |       |
|  | 40                            | —  | 75                     | $DV_{DD} = 1.8\text{ V}$            |       |
| eSPI, SDHC_WP, SDHC_CD   | 45                            | —  | 90                     | $CV_{DD} = 3.3\text{ V}$            | —     |
|  | 40                            | —  | 75                     | $CV_{DD} = 1.8\text{ V}$            |       |
| eSDHC  | 45                            | —  | 90                     | $EV_{DD} = 3.3\text{ V}$            | —     |
|  | 40                            | —  | 75                     | $EV_{DD} = 1.8\text{ V}$            |       |

Notes: 1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at  $T_j = 105\text{ }^\circ\text{C}$  and at  $G1V_{DD}(\text{min})$ .

2. Estimated number based on best case processed device.

3. Estimated number based on worst case processed device.

### 3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. Bring up  $V_{DD}$ ,  $SnV_{DD}$ ,  $USB\_SV_{DD}$ ,  $V_{DD\_LP}$ ,  $USB\_HV_{DD}$ ,  $LV_{DD}$ ,  $DV_{DD}$ ,  $CV_{DD}$ ,  $USB\_OV_{DD}$ ,  $OV_{DD}$ ,  $TH\_V_{DD}$ ,  $AV_{DD}$  (cores, platform, DDR),  $G1V_{DD}$ ,  $XnV_{DD}$ , and  $AV_{DD\_SDn\_PLLn}$ . Drive  $PROG\_SFP = GND$ .  
–  $PORESET\_B$  input must be driven asserted and held during this step.

Power supplies in step 1 have no ordering requirement with respect to one another except for the USB power supplies per the following note.

**NOTE**

- a.  $USB\_SV_{DD}$  supply must ramp before or after the  $USB\_HV_{DD}$  and  $USB\_OV_{DD}$  supplies have ramped. The supply set that ramp first must reach 90% of its final value before a supply from the other set can be ramped up.
- b.  $USB\_HV_{DD}$  and  $USB\_OV_{DD}$  supplies among themselves are sequence independent.
- c.  $USB\_HV_{DD}$  rise time (10% to 90%) has a minimum of 100  $\mu\text{s}$ .

2. Negate PORESET\_B input as long as the required assertion/hold time has been met per [Table 3-18](#).
3. For secure boot fuse programming, use the following steps:
  - a. After negation of PORESET\_B, drive PROG\_SFP = 1.80 V after a required minimum delay per [Table 3-4](#).
  - b. After fuse programming is completed, it is required to return PROG\_SFP = GND before the system is power cycled (PORESET\_B assertion) or powered down ( $V_{DD}$  ramp down) per the required timing specified in [Table 3-4](#). See Security fuse processor, for additional details.

## Warning

No activity other than that required for secure boot fuse programming is permitted while PROG\_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG\_SFP = GND.

From a system standpoint, if any of the I/O power supplies ramp prior to the  $V_{DD}$  supplies, there will be a brief period as the  $V_{DD}$  powers up that the I/Os associated with that I/O supply may go from being tri- stated to an indeterminate state (either driven to a logic one or zero) and extra current may be drawn by the device.

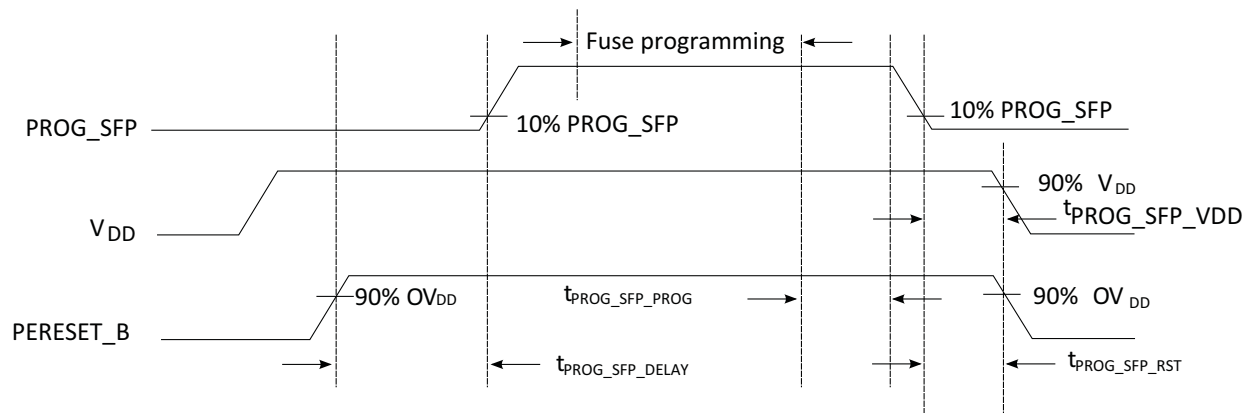
Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

If using Trust Architecture Security Monitor battery-backed features, prior to  $V_{DD}$  ramping up to the 0.5 V level, ensure that OVDD is ramped to the recommended operational voltage and SYSCLK is running. The clock should have a minimum frequency of 800 Hz and a maximum frequency no greater than the supported system clock frequency for the device.

All supplies must be at their stable values within 400 ms.

This figure provides the PROG\_SFP timing diagram.

**Figure 3-2.** PROG\_SFP timing diagram



NOTE: PROG\_SFP must be stable at 1.80 V prior to initiating fuse programming.

This table provides information on the power-down and power-up sequence parameters for PROG\_SFP.

**Table 3-4.** PROG\_SFP timing<sup>(5)</sup>

| Driver type                   | Min | Max | Unit          | Notes |
|-------------------------------|-----|-----|---------------|-------|
| $t_{\text{PROG\_SFP\_DELAY}}$ | 100 | —   | SYSCLKs       | (1)   |
| $t_{\text{PROG\_SFP\_PROG}}$  | 0   | —   | $\mu\text{s}$ | (2)   |
| $t_{\text{PROG\_SFP\_VDD}}$   | 0   | —   | $\mu\text{s}$ | (3)   |
| $t_{\text{PROG\_SFP\_RST}}$   | 0   | —   | $\mu\text{s}$ | (4)   |

- Notes:
1. Delay required from the deassertion of PORESET\_B to driving PROG\_SFP ramp up. Delay measured from PORESET\_B deassertion at 90%  $OV_{DD}$  to 10% PROG\_SFP ramp up.
  2. Delay required from fuse programming finished to PROG\_SFP ramp down start. Fuse programming must complete while PROG\_SFP is stable at 1.80 V. No activity other than that required for secure boot fuse programming is permitted while PROG\_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG\_SFP = GND. After fuse programming is completed, it is required to return PROG\_SFP = GND.
  3. Delay required from PROG\_SFP ramp down complete to  $V_{DD}$  ramp down start. PROG\_SFP must be grounded to minimum 10% PROG\_SFP before  $V_{DD}$  is at 90%  $V_{DD}$ .
  4. Delay required from PROG\_SFP ramp down complete to PORESET\_B assertion. PROG\_SFP must be grounded to minimum 10% PROG\_SFP before PORESET\_B assertion reaches 90%  $OV_{DD}$ .
  5. Only two secure boot fuse programming events are permitted per lifetime of a device.

### 3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that PROG\_SFP = GND before the system is power cycled (PORESET\_B assertion) or powered down ( $V_{DD}$  ramp down) per the required timing specified in [Table 3-4](#).

#### NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.



## 3.4 Power characteristics

This table shows the power dissipations of the  $V_{DD}$  and  $SnV_{DD}$  supply for various operating platform clock frequencies versus the core and DDR clock frequencies when AltiVec power is gated off. See the e6500 core reference manual, section 8.6.1, "AltiVec power down—software controlled entry" for details on how to place AltiVec in low power state. Note that these numbers are preliminary. More accurate power numbers will be available after the measurement on the silicon is complete.

**Table 3-5.** T2080 power dissipation with AltiVec power-gated off<sup>(1)</sup>

| Power mode | Core freq (MHz)             | Plat freq (MHz) | DDR data rate (MT/s) | FMan freq (MHz) | $V_{DD}^{(8)}$ (V) | $SnV_{DD}$ (V) | Junction temperature (°C) | Core and platform power <sup>(1)</sup> (W) | $V_{DD}$ power (W) | $SnV_{DD}$ power (W) | Notes        |
|------------|-----------------------------|-----------------|----------------------|-----------------|--------------------|----------------|---------------------------|--|--------------------|----------------------|--------------|
| Typical    | 1800<br>(low-power version) | 600             | 2133                 | 700             | VID                | 1.0            | 65                        | 12.9                                       | 11.9               | 1.0                  | (2)(3)(9)    |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 18.9                                       | 17.9               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 21.1                                       | 20.1               | 1.0                  | (5)(6)(7)(9) |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 20.4                                       | 19.4               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 22.6                                       | 21.6               | 1.0                  | (5)(6)(7)(9) |
| Typical    | 1800<br>(standard version)  | 600             | 1867                 | 700             | VID                | 1.0            | 65                        | 13.0                                       | 12.0               | 1.0                  | (2)(3)       |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 21.1                                       | 20.1               | 1.0                  | (4)(5)       |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 23.3                                       | 22.3               | 1.0                  | (5)(6)(7)    |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 22.6                                       | 21.6               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 24.8                                       | 23.8               | 1.0                  | (5)(6)(7)(9) |
| Typical    | 1533<br>(low-power version) | 600             | 2133                 | 700             | VID                | 1.0            | 65                        | 11.9                                       | 10.9               | 1.0                  | (2)(3)(9)    |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 15.4                                       | 14.4               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 17.3                                       | 16.3               | 1.0                  | (5)(6)(7)(9) |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 16.9                                       | 15.9               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 18.8                                       | 17.8               | 1.0                  | (5)(6)(7)(9) |
| Typical    | 1533<br>(standard version)  | 600             | 1867                 | 700             | VID                | 1.0            | 65                        | 11.9                                       | 10.9               | 1.0                  | (2)(3)       |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 17.2                                       | 16.2               | 1.0                  | (4)(5)       |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 19.1                                       | 18.1               | 1.0                  | (5)(6)(7)    |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 18.7                                       | 17.7               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 20.6                                       | 19.6               | 1.0                  | (5)(6)(7)(9) |
| Typical    | 1200<br>(low-power version) | 533             | 1600                 | 600             | VID                | 1.0            | 65                        | 10.4                                       | 9.4                | 1.0                  | (2)(3)(9)    |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 12.6                                       | 11.6               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 14.1                                       | 13.1               | 1.0                  | (5)(6)(7)(9) |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 14.1                                       | 13.1               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 15.6                                       | 14.6               | 1.0                  | (5)(6)(7)(9) |
| Typical    | 1200<br>(standard version)  | 533             | 1600                 | 600             | VID                | 1.0            | 65                        | 10.4                                       | 9.4                | 1.0                  | (2)(3)       |
| Thermal    |                             |                 |                      |                 |                    |                | 105                       | 13.9                                       | 12.9               | 1.0                  | (4)(5)       |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 15.4                                       | 14.4               | 1.0                  | (5)(6)(7)    |
| Thermal    |                             |                 |                      |                 |                    |                | 125                       | 15.4                                       | 14.1               | 1.0                  | (4)(5)(9)    |
| Maximum    |                             |                 |                      |                 |                    |                |                           | 16.9                                       | 15.9               | 1.0                  | (5)(6)(7)(9) |

- Notes:
1. Combined power of  $V_{DD}$  and  $SnV_{DD}$  with platform at power-on reset default state, the DDR controller and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.
  2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and is executing DMA on the platform with 100% activity factor.
  3. Typical power based on nominal, processed distribution for this device.
  4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.
  5. Thermal and maximum power are based on worst-case process distribution for this device.
  6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.
  7. Maximum power provided for power supply design sizing.
  8. Voltage ID (VID) operating range is between 0.975V to 1.025V.
  9. The difference between low-power and standard is shown in the product part number.

## T2080 [Preliminary]

This table shows the power dissipation of the  $V_{DD}$  and  $SnV_{DD}$  supply for various operating platform clock frequencies versus the core and DDR clock frequencies when Altivec power is gated on. See the e6500 core reference manual, section 8.6.4, "Altivec power up—software-controlled entry" for details on how to enable Altivec. These numbers are preliminary. More accurate power numbers will be available after the measurement on the silicon is complete.

**Table 3-6.** T2080 preliminary power dissipation with Altivec power-gated on<sup>(1)</sup>

| Power mode | Core freq (MHz)     | Plat freq (MHz) | DDR data rate (MT/s) | FMan freq (MHz) | V <sub>DD</sub> <sup>(8)</sup> (V) | SnV <sub>DD</sub> (V) | Junction temperature (°C) | Core and platform power <sup>(1)</sup> (W) | V <sub>DD</sub> power (W) | SnV <sub>DD</sub> power (W) | Notes        |
|------------|---------------------|-----------------|----------------------|-----------------|------------------------------------|-----------------------|---------------------------|--|---------------------------|-----------------------------|--------------|
| Typical    | 1800                | 600             | 2133                 | 700             | VID                                | 1.0                   | 65                        | 13.8                                       | 12.8                      | 1.0                         | (2)(3)(9)    |
| Thermal    | (low-power version) | 600             | 2133                 | 700             | VID                                | 1.0                   | 105                       | 20.2                                       | 19.2                      | 1.0                         | (4)(5)(9)    |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 22.3                                       | 21.3                      | 1.0                         | (5)(6)(7)(9) |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 21.7                                       | 20.7                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 23.8                                       | 22.8                      | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |
| Typical    | 1800                | 600             | 1867                 | 700             | VID                                | 1.0                   | 65                        | 13.9                                       | 12.9                      | 1.0                         | (2)(3)       |
| Thermal    | (standard version)  | 600             | 1867                 | 700             | VID                                | 1.0                   | 105                       | 22.4                                       | 21.4                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 24.5                                       | 23.5                      | 1.0                         | (5)(6)(7)    |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 23.9                                       | 22.9                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 24   | 25                        | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |
| Typical    | 1533                | 600             | 2133                 | 700             | VID                                | 1.0                   | 65                        | 12.8                                       | 11.8                      | 1.0                         | (2)(3)(9)    |
| Thermal    | (low-power version) | 600             | 2133                 | 700             | VID                                | 1.0                   | 105                       | 16.3                                       | 15.3                      | 1.0                         | (4)(5)(9)    |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 18.1                                       | 17.1                      | 1.0                         | (5)(6)(7)(9) |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 17.8                                       | 16.8                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 19.6                                       | 18.6                      | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |
| Typical    | 1533                | 600             | 1867                 | 700             | VID                                | 1.0                   | 65                        | 12.7                                       | 11.7                      | 1.0                         | (2)(3)       |
| Thermal    | (standard version)  | 600             | 1867                 | 700             | VID                                | 1.0                   | 105                       | 18.2                                       | 17.2                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 20.0                                       | 19.0                      | 1.0                         | (5)(6)(7)    |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 19.7                                       | 18.7                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 21.5                                       | 20.5                      | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |
| Typical    | 1200                | 533             | 1600                 | 600             | VID                                | 1.0                   | 65                        | 11.0                                       | 10.0                      | 1.0                         | (2)(3)(9)    |
| Thermal    | (low-power version) | 533             | 1600                 | 600             | VID                                | 1.0                   | 105                       | 13.3                                       | 12.3                      | 1.0                         | (4)(5)(9)    |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 16.1                                       | 15.1                      | 1.0                         | (5)(6)(7)(9) |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 14.8                                       | 13.8                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 17.6                                       | 16.6                      | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |
| Typical    | 1200                | 533             | 1600                 | 600             | VID                                | 1.0                   | 65                        | 11.0                                       | 10.0                      | 1.0                         | (2)(3)       |
| Thermal    | (standard version)  | 533             | 1600                 | 600             | VID                                | 1.0                   | 105                       | 14.7                                       | 13.7                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 16.1                                       | 15.1                      | 1.0                         | (5)(6)(7)    |
| Thermal    |                     |                 |                      |                 |                                    |                       | 125                       | 16.2                                       | 15.2                      | 1.0                         | (4)(5)       |
| Maximum    |                     |                 |                      |                 |                                    |                       |                           | 17.6                                       | 16.6                      | 1.0                         | (5)(6)(7)    |
|            |                     |                 |                      |                 |                                    |                       |                           |  |                           |                             |              |

Notes: 1. Combined power of  $V_{DD}$  and  $SnV_{DD}$  with platform at power-on reset default state, the DDR controller and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and is executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Thermal and maximum power are based on worst-case processed device.
6. Maximum power assumes Dhrystone running with work power activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.
7. Maximum power provided for power supply design sizing.
8. Voltage ID (VID) operating range is between 0.975V to 1.025V.
9. The difference between low-power and standard is shown in the product part number. The low-power version part numbers end in "T1B", "P1B", and "QLB".

This table provides all the estimated I/O power supply values based on preliminary measurements.

**Table 3-7.** T2080 I/O power dissipation

| I/O Power supply     |                            | Parameter       | Typical (mW) | Maximum (mW) | Notes        |
|----------------------|----------------------------|-----------------|--------------|--------------|--------------|
| LVC MOS              | OV <sub>DD</sub> 1.8 V     | —               | 50           | 60           | (1)(3)(4)(6) |
| LVC MOS              | CV <sub>DD</sub> 1.8 V     | —               | 40           | 70           |              |
| LVC MOS              | CV <sub>DD</sub> 2.5 V     | —               | 50           | 80           |              |
| LVC MOS              | LV <sub>DD</sub> 1.8 V     | —               | 230          | 360          |              |
| LVC MOS              | LV <sub>DD</sub> 2.5 V     | —               | 310          | 440          |              |
| LVC MOS              | DV <sub>DD</sub> 1.8 V     | —               | 50           | 90           |              |
| LVC MOS              | DV <sub>DD</sub> 2.5 V     | —               | 70           | 130          |              |
| DDR I/O              | GV <sub>DD</sub> 1.5 V     | 2133 MT/s       | 1144         | 2200         | (1)(2)(5)(6) |
| DDR I/O              | GV <sub>DD</sub> 1.35 V    | 1867 MT/s       | 840          | 1610         |              |
| DDR I/O              | GV <sub>DD</sub> 1.5 V     | 1867 MT/s       | 1030         | 1990         |              |
| DDR I/O              | GV <sub>DD</sub> 1.35 V    | 1600 MT/s       | 720          | 1380         |              |
| DDR I/O              | GV <sub>DD</sub> 1.5 V     | 1600 MT/s       | 890          | 1700         |              |
| USB_PHY              | USB_OV <sub>DD</sub> 1.8 V | —               | 40           | 60           | (1)(6)       |
| USB_PHY              | USB_HV <sub>DD</sub> 3.3 V | —               | 100          | 110          |              |
| USB_SV <sub>DD</sub> | USB_SV <sub>DD</sub>       | —               | 7            | 7            |              |
| PLL core and system  | AVDD_CGA*, AVDD_PLAT       | —               | 20           | 20           | (1)(6)       |
| PLL DDR              | AVDD_D1                    | —               | 30           | 40           |              |
| PLL LYNX             | AVDD_SRDS*                 | —               | 50           | 50           |              |
| SerDes, 1.35 V       | XV <sub>DD</sub> SGMII     | 1x 1.25 G-baud  | 50           | 60           | (1)(6)(7)    |
| SerDes, 1.35 V       | XV <sub>DD</sub>           | 2x 1.25 G-baud  | 70           | 90           |              |
| SerDes, 1.35 V       | XV <sub>DD</sub>           | 4x 1.25 G-baud  | 130          | 140          |              |
| SerDes, 1.35 V       | XV <sub>DD</sub>           | 8x 1.25 G-baud  | 230          | 240          |              |
| SerDes, 1.35 V       | XV <sub>DD</sub>           | 1x 3.125 G-baud | 50           | 60           |              |
| SerDes, 1.35 V       | XV <sub>DD</sub>           | 2x 3.125 G-baud | 80           | 90           |              |

**Table 3-7.** T2080 I/O power dissipation (Continued)

| I/O Power supply          |                       | Parameter       | Typical (mW) | Maximum (mW) | Notes  |
|---------------------------|-----------------------|-----------------|--------------|--------------|--------|
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 3.125 G-baud | 140          | 150          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub> SATA | 1x 3 G-baud     | 50           | 60           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 3 G-baud     | 70           | 80           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub> SRIO | 1x 2.5 G-baud   | 50           | 60           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 2.5 G-baud   | 80           | 90           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 2.5 G-baud   | 140          | 150          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 1x 3.125 G-baud | 50           | 60           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 3.125 G-baud | 80           | 90           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 3.125 G-baud | 140          | 150          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 1x 5 G-baud     | 50           | 70           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 5 G-baud     | 90           | 100          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 5 G-baud     | 150          | 160          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub> PEX2 | 1x 5 G-baud     | 50           | 70           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 5 G-baud     | 90           | 100          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 5 G-baud     | 150          | 160          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 8x 5 G-baud     | 280          | 290          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub> PEX3 | 1x 8 G-baud     | 60           | 70           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 8 G-baud     | 100          | 110          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 8 G-baud     | 170          | 190          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub> XFI  | 1x 10 G-baud    | 60           | 70           |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 2x 10 G-baud    | 100          | 110          |        |
| SerDes, 1.35 V            | XV <sub>DD</sub>      | 4x 10 G-baud    | 170          | 190          |        |
| Fuse Programming Override | PROG_SFG              | –               | –            | 173          | (1)(8) |
| Thermal Monitor Unit      | TH_V <sub>DD</sub>    | –               | –            | 18           | (1)    |

- Notes:
1. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105 °C junction temperature.
  2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
  3. Assuming 15 pF total capacitance load.
  4. GPIOs are supported on 1.8 V and 2.5 V rails as specified in the hardware specification.
  5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
  6. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming at 65° C junction temperature.
  7. The total power numbers of XV<sub>DD</sub> is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the XV<sub>DD</sub> power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.
  8. The max power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.

This table shows the preliminary power dissipation on the  $V_{DD\_LP}$  supply for the T2080 at allowable voltage levels.

**Table 3-8.**  $V_{DD\_LP}$  Power Dissipation

| Supply                        | Maximum | Unit | Notes |
|-------------------------------|---------|------|-------|
| $V_{DD\_LP}$ (T2080 on, 65C)  | 1.5     | mW   | (1)   |
| $V_{DD\_LP}$ (T2080 off, 65C) | 360     | uW   | (2)   |
| $V_{DD\_LP}$ (T2080 off, 40C) | 132     | uW   | (2)   |

- Notes:
1.  $V_{DD\_LP} = 1.0$  V,  $T_J = 65$  °C
  2. When T2080 is off,  $V_{DD\_LP}$  may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches  $V_{DD\_LP}$  to battery when SoC powered down. See T2080 Reference Manual Trust Architecture chapter for more information.

**Table 3-9.** T2080 Rev 1.1 single core/single cluster low-power mode power savings, 1.0 V 105°C<sup>(1)(2)(3)</sup>

| Mode  | Core Frequency = 1.8 GHz | Core Frequency = 1.533 GHz | Core Frequency = 1.2 GHz | Units | Comments  | Notes     |
|-------|--------------------------|----------------------------|--------------------------|-------|---|-----------|
| PH10  | 0.96                     | 0.82                       | 0.64                     | Watts | Savings realized moving from PH00 to PH10 state, single core      | (1)(2)(4) |
| PH15  | 0.27                     | 0.23                       | 0.19                     | Watts | Savings realized moving from PH10 to PH15 state, single core      | (1)(4)(5) |
| PH20  | 0.37                     | 0.35                       | 0.34                     | Watts | Savings realized moving from PH15 to PH20 state, single core      | (1)(4)    |
| PCL10 | 0.95                     | 0.91                       | 0.73                     | Watts | Savings realized moving from PH20 to PCL10 state, single cluster  | (1)       |
| LPM20 | 0.90                     | 0.82                       | 0.72                     | Watts | Savings realized moving from PCL10 to LPM20 state                 | (1)       |
| LPM40 | 0.60                     | 0.49                       | 0.35                     | Watts | Savings realized moving from LPM20 to LPM40 state, single cluster | (1)       |

- Notes:
1. Power for  $V_{DD}$  only.
  2. Typical power assumes Dhrystone running (PH00 state) with 70% activity factor.
  3. Typical power based on nominal process distribution for this device.
  4. PH10, PH15, PH20 power savings with one core. Maximum savings would be  $n$  times, where  $n$  is the number of used cores.
  5. Require both threads of the core to enter the same low-power mode.

## 3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

**Table 3-10.** Power supply ramp rate

| Parameter   | Min | Max | Unit | Notes  |
|---|-----|-----|------|--------|
| Required ramp rate for all voltage supplies (including OV <sub>DD</sub> /DV <sub>DD</sub> /G1V <sub>DD</sub> /SnV <sub>DD</sub> /XnV <sub>DD</sub> /LV <sub>DD</sub> , all core and platform VDD supplies, D1_MVREF, all AV <sub>DD</sub> , and CV <sub>DD</sub> supplies.) | –   | 25  | V/ms | (1)(2) |
| Required ramp rate for PROG_SFP   | –   | 25  | V/ms | (1)(2) |

Notes: 1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.  
2. Over full recommended operating temperature range (see [Table 3-2](#)).

## 3.6 Input clocks

### 3.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

#### 3.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC specifications.

**Table 3-11.** SYSCLK DC electrical characteristics<sup>(3)</sup>

| Parameter   | Symbol          | Min  | Typical | Max | Unit | Notes |
|---|-----------------|------|---------|-----|------|-------|
| Input high voltage  | V <sub>IH</sub> | 1.25 | –       | –   | V    | (1)   |
| Input low voltage   | V <sub>IL</sub> | –    | –       | 0.6 | V    | (1)   |
| Input capacitance   | C <sub>IN</sub> | –    | 7       | 12  | pF   | –     |
| Input current (OV <sub>IN</sub> = 0 V or OV <sub>IN</sub> = OVDD) | I <sub>IN</sub> | –50  | –       | +50 | μA   | (2)   |

Notes: 1. The min V<sub>IL</sub> and max V<sub>IH</sub> values are based on the respective min and max OV<sub>IN</sub> values found in [Table 3-2](#).  
2. The symbol OV<sub>IN</sub>, in this case, represents the OV<sub>IN</sub> symbol referenced in [Recommended operating conditions](#).  
3. At recommended operating conditions with OV<sub>DD</sub> = 1.8 V, see [Table 3-2](#).

### 3.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

**Table 3-12.** SYSCLK AC timing specifications<sup>(5)</sup>

| Parameter/condition                             | Symbol                             | Min                         | Typ | Max                       | Unit | Notes  |
|---|------------------------------------|-----------------------------|-----|---------------------------|------|--------|
| SYSCLK frequency                                | $f_{\text{SYSCLK}}$                | 66                          | —   | 133.3                     | MHz  | (1)(2) |
| SYSCLK cycle time                               | $t_{\text{SYSCLK}}$                | 7.5                         | —   | 15                        | ns   | (1)(2) |
| SYSCLK duty cycle                               | $t_{\text{KHK}}/t_{\text{SYSCLK}}$ | 40                          | —   | 60                        | %    | (2)    |
| SYSCLK slew rate                                | —                                  | 1                           | —   | 4                         | V/ns | (3)    |
| SYSCLK peak period jitter                       | —                                  | —                           | —   | ± 150                     | ps   | —      |
| SYSCLK jitter phase noise at -56 dBc            | —                                  | —                           | —   | 500                       | KHz  | (4)    |
| AC Input Swing Limits at 1.8 V $OV_{\text{DD}}$ | $\Delta V_{\text{AC}}$             | $0.6 \times OV_{\text{DD}}$ | —   | $1 \times OV_{\text{DD}}$ | V    | (6)    |

- Notes:
- Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
  - Measured at the rising edge and/or the falling edge at  $OV_{\text{DD}}/2$ .
  - Slew rate as measured from  $0.35 \times OV_{\text{DD}}$  to  $0.65 \times OV_{\text{DD}}$ .
  - Phase noise is calculated as FFT of TIE jitter.
  - At recommended operating conditions with  $OV_{\text{DD}} = 1.8\text{V}$ , see [Table 3-2](#).
  - AC swing measured relative to half  $OV_{\text{DD}}$  or  $V_{\text{IH}}$  and  $V_{\text{IL}}$  have equal absolute offset from  $OV_{\text{DD}}/2$ , So,  $\text{Swing} = (V_{\text{IH}} - V_{\text{IL}})/OV_{\text{DD}}$  and  $\Delta V_{\text{AC}} = \text{Swing} \times OV_{\text{DD}}$ .

### 3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

**Table 3-13.** Spread-spectrum clock source recommendations<sup>(1)</sup>

| Parameter            | Min | Max | Unit | Notes  |
|----------------------|-----|-----|------|--------|
| Frequency modulation | —   | 60  | kHz  | —      |
| Frequency spread     | —   | 1.0 | %    | (2)(3) |

- Notes:
- At recommended operating conditions with  $OV_{\text{DD}} = 1.8\text{ V}$ , see [Table 3-2](#).
  - SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in [Table 3-12](#).
  - Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

#### CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.



## 3.6.3 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 3.6.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC specifications.

**Table 3-14.** ECn\_GTX\_CLK125 DC electrical characteristics<sup>(1)</sup>

| Parameter  | Symbol   | Min | Typical | Max      | Unit    | Notes |
|--|----------|-----|---------|----------|---------|-------|
| Input high voltage                                       | $V_{IH}$ | 1.7 | –       | –        | V       | (2)   |
| Input low voltage  | $V_{IL}$ | –   | –       | 0.7      | V       | (2)   |
| Input capacitance  | $C_{IN}$ | –   | –       | 6        | pF      | –     |
| Input current ( $LV_{in} = 0$ V or $LV_{in} = LV_{DD}$ ) | $I_{IN}$ | –   | –       | $\pm 50$ | $\mu$ A | (3)   |

- Notes:
1. At recommended operating conditions with  $LV_{DD} = 2.5$  V.
  2. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $LV_{in}$  values found in [Table 3-2](#).
  3. The symbol  $LV_{in}$ , in this case, represents the  $LV_{in}$  symbol referenced in [Recommended operating conditions](#).

This table provides the Ethernet gigabit reference clocks AC timing specifications.

**Table 3-15.** ECn\_GTX\_CLK125 AC timing specifications<sup>(1)</sup>

| Parameter/Condition                                    | Symbol                | Min           | Typical | Max           | Unit | Notes |
|--|-----------------------|---------------|---------|---------------|------|-------|
| ECn_GTX_CLK125 frequency                               | $t_{G125}$            | 125 – 100 ppm | 125     | 125 + 100 ppm | MHz  | –     |
| ECn_GTX_CLK125 cycle time                              | $t_{G125}$            | –             | 8       | –             | ns   | –     |
| ECn_GTX_CLK125 rise and fall time<br>$LV_{DD} = 2.5$ V | $t_{G125R}/t_{G125F}$ | –             | –       | 0.75          | ns   | (2)   |
| ECn_GTX_CLK125 duty cycle<br>1000Base-T for RGMII      | $t_{G125H}/t_{G125}$  | 47            | –       | 53            | %    | (2)   |
| ECn_GTX_CLK125 jitter                                  | –                     | –             | –       | $\pm 150$     | ps   | (2)   |

- Notes:
1. At recommended operating conditions with  $LV_{DD} = 2.5$  V  $\pm$  125 mV.
  2. Rise and fall times for ECn\_GTX\_CLK125 are measured from 0.5 and 2.0 V for  $LV_{DD} = 2.5$  V.
  3. ECn\_GTX\_CLK125 is used to generate the GTX clock for the Ethernet transmitter with 2% degradation. The ECn\_GTX\_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the GTX\_CLK. See [RGMII AC timing specifications](#) for duty cycle for 10Base-T and 100Base-T reference clock.

### 3.6.5 DDR clock timing

This section provides the DDR clock DC and AC timing specifications. DDR3L maximum supported data rate is 1866 MT/s.

#### 3.6.5.1 DDR clock DC timing specifications

This table provides the DDR clock (DDRCLK) DC specifications.

**Table 3-16.** DDRCLK DC electrical characteristics<sup>(3)</sup>

| Parameter  | Symbol   | Min  | Typical | Max  | Unit | Notes |
|--|----------|------|---------|------|------|-------|
| Input high voltage                                       | $V_{IH}$ | 1.25 | —       | —    | V    | (1)   |
| Input low voltage  | $V_{IL}$ | —    | —       | 0.6  | V    | (1)   |
| Input capacitance  | $C_{IN}$ | —    | —       | 12   | pF   | —     |
| Input current ( $OV_{IN} = 0$ V or $OV_{IN} = OV_{DD}$ ) | $I_{IN}$ | −50  | —       | + 50 | μA   | (2)   |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $OV_{IN}$  in this case, represents the  $OV_{IN}$  symbol referenced in [Recommended operating conditions](#).
  3. At recommended operating conditions with  $OV_{DD} = 1.8$  V, see [Table 3-2](#).

#### 3.6.5.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

**Table 3-17.** DDRCLK AC timing specifications<sup>(5)</sup>

| Parameter/Condition                      | Symbol                 | Min                   | Typ | Max                   | Unit | Notes  |
|--|------------------------|-----------------------|-----|-----------------------|------|--------|
| DDRCLK frequency                         | $f_{DDRCLK}$           | 66.7                  | —   | 133.3                 | MHz  | (1)(3) |
| DDRCLK cycle time                        | $t_{DDRCLK}$           | 5                     | —   | 15                    | ns   | (1)(2) |
| DDRCLK duty cycle                        | $t_{KHK} / t_{DDRCLK}$ | 40                    | —   | 60                    | %    | (2)    |
| DDRCLK slew rate                         | —                      | 1                     | —   | 4                     | V/ns | (3)    |
| DDRCLK peak period jitter                | —                      | —                     | —   | ± 150                 | ps   | —      |
| DDRCLK jitter phase noise at −56 dBc     | —                      | —                     | —   | 500                   | KHz  | (4)    |
| AC Input Swing Limits at 1.8 V $OV_{DD}$ | $\Delta V_{AC}$        | $0.35 \times OV_{DD}$ | —   | $0.65 \times OV_{DD}$ | V    | —      |

- Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.
  2. Measured at the rising edge and/or the falling edge at  $OV_{DD}/2$ .
  3. Slew rate as measured from  $0.35 \times OV_{DD}$  to  $0.65 \times OV_{DD}$ .
  4. Phase noise is calculated as FFT of TIE jitter.
  5. At recommended operating conditions with  $OV_{DD} = 1.8$  V, see [Table 3-2](#).

## 3.6.6 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, IFC, see the specific interface section.

## 3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

**Table 3-18.** RESET Initialization timing specifications

| Parameter/Condition  | Min | Max | Unit    | Notes  |
|--|-----|-----|---------|--------|
| Required assertion time of PORESET_B   | 1   | –   | ms      | (1)    |
| Required input assertion time of HRESET_B  | 32  | –   | SYSCLKs | (2)(3) |
| Maximum rise/fall time of HRESET_B   | –   | 10  | SYSCLK  | (4)    |
| Maximum rise/fall time of PORESET_B  | –   | 1   | SYSCLK  | (4)    |
| PLL input setup time with stable SYSCLK before HRESET_B negation   | 100 | –   | μs      | –      |
| Input setup time for POR configs with respect to negation of PORESET_B                                     | 4   | –   | SYSCLKs | (2)    |
| Input hold time for all POR configs with respect to negation of PORESET_B                                  | 2   | –   | SYSCLKs | (2)    |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B | –   | 5   | SYSCLKs | (2)    |

- Notes:
1. PORESET\_B must be driven asserted before the core and platform power supplies are powered up.
  2. SYSCLK is the primary clock input for the chip.
  3. The device asserts HRESET\_B as an output when PORESET\_B is asserted to initiate the power-on reset process. The device releases HRESET\_B sometime after PORESET\_B is deasserted. The exact sequencing of HRESET\_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.
  4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

## 3.8 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required  $GV_{DD}(\text{typ})$  voltage is 1.5 V when interfacing to DDR3 SDRAM and the  $GV_{DD}(\text{typ})$  voltage is 1.35 V when interfacing to DDR3L SDRAM.

### NOTE

When operating at a DDR data rate greater than or equal to 1866 MT/s, only one dual-ranked module per memory controller is supported. DDR3L is not supported at a DDR data rate of 2133 MT/s.

### 3.8.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

**Table 3-19.** DDR3 SDRAM interface DC electrical characteristics ( $GV_{DD} = 1.5\text{ V}$ )<sup>(1)(7)</sup>

| Parameter             | Symbol   | Min                   | Max                   | Unit          | Note      |
|-----------------------|----------|-----------------------|-----------------------|---------------|-----------|
| I/O reference voltage | MVREFn   | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V             | (2)(3)(4) |
| Input high voltage    | $V_{IH}$ | $MVREFn + 0.100$      | $GV_{DD}$             | V             | (5)       |
| Input low voltage     | $V_{IL}$ | GND                   | $MVREFn - 0.100$      | V             | (5)       |
| I/O leakage current   | $I_{OZ}$ | -50                   | 50                    | $\mu\text{A}$ | (6)       |

- Notes:
1.  $GV_{DD}$  is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
  2.  $Dn\_MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$  and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $Dn\_MV_{REF}$  may not exceed the  $Dn\_MV_{REF}$  DC level by more than  $\pm 1\%$  of  $GV_{DD}$  (i.e.  $\pm 15\text{ mV}$ ).
  3.  $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to  $Dn\_MV_{REF}$  with a min value of  $Dn\_MV_{REF} - 0.04$  and a max value of  $Dn\_MV_{REF} + 0.04$ .  $V_{TT}$  should track variations in the DC level of  $Dn\_MV_{REF}$ .
  4. The voltage regulator for  $Dn\_MV_{REF}$  must meet the specifications stated in [Table 3-21](#).
  5. Input capacitance load for DQ, DQS, and DQS\_B are available in the IBIS models.
  6. Output leakage is measured with all outputs disabled,  $0\text{ V} = V_{OUT} = GV_{DD}$ .
  7. For recommended operating conditions, see [Table 3-2](#).

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

**Table 3-20.** DDR3L SDRAM interface DC electrical characteristics ( $GV_{DD} = 1.35\text{ V}$ )<sup>(1)(7)</sup>

| Parameter             | Symbol   | Min                   | Max                   | Unit          | Note      |
|-----------------------|----------|-----------------------|-----------------------|---------------|-----------|
| I/O reference voltage | MVREFn   | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V             | (2)(3)(4) |
| Input high voltage    | $V_{IH}$ | $MVREFn + 0.090$      | $GV_{DD}$             | V             | (5)       |
| Input low voltage     | $V_{IL}$ | GND                   | $MVREFn - 0.090$      | V             | (5)       |
| I/O leakage current   | $I_{OZ}$ | -100                  | 100                   | $\mu\text{A}$ | (6)       |

- Notes:
1.  $GV_{DD}$  is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
  2.  $Dn\_MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$  and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $Dn\_MV_{REF}$  may not exceed the  $Dn\_MV_{REF}$  DC level by more than  $\pm 1\%$  of  $GV_{DD}$  (i.e.  $\pm 13.5\text{ mV}$ ).
  3.  $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to  $Dn\_MV_{REF}$  with a min value of  $Dn\_MV_{REF} - 0.04$  and a max value of  $Dn\_MV_{REF} + 0.04$ .  $V_{TT}$  should track variations in the DC level of  $Dn\_MV_{REF}$ .
  4. The voltage regulator for  $Dn\_MV_{REF}$  must meet the specifications stated in [Table 3-21](#).
  5. Input capacitance load for DQ, DQS, and DQS\_B are available in the IBIS models.
  6. Output leakage is measured with all outputs disabled,  $0\text{ V} = V_{OUT} = GV_{DD}$ .
  7. For recommended operating conditions, see [Table 3-2](#).

This table provides the current draw characteristics for  $Dn\_MV_{REF}$ .

**Table 3-21.** Current draw characteristics for  $Dn\_MV^{(1)}$

| Parameter                                       | Symbol          | Min | Max | Unit    | Notes |
|---|-----------------|-----|-----|---------|-------|
| Current draw for DDR3 SDRAM for $Dn\_MV_{REF}$  | $I_{Dn\_MVREF}$ | —   | 500 | $\mu A$ | —     |
| Current draw for DDR3L SDRAM for $Dn\_MV_{REF}$ | $I_{Dn\_MVREF}$ | —   | 500 | $\mu A$ | —     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

## 3.8.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required  $GV_{DD}(typ)$  voltage is 1.5 V when interfacing to DDR3 SDRAM and the required  $GV_{DD}(typ)$  voltage is 1.35 V when interfacing to DDR3L SDRAM.

### 3.8.2.1 DDR3 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

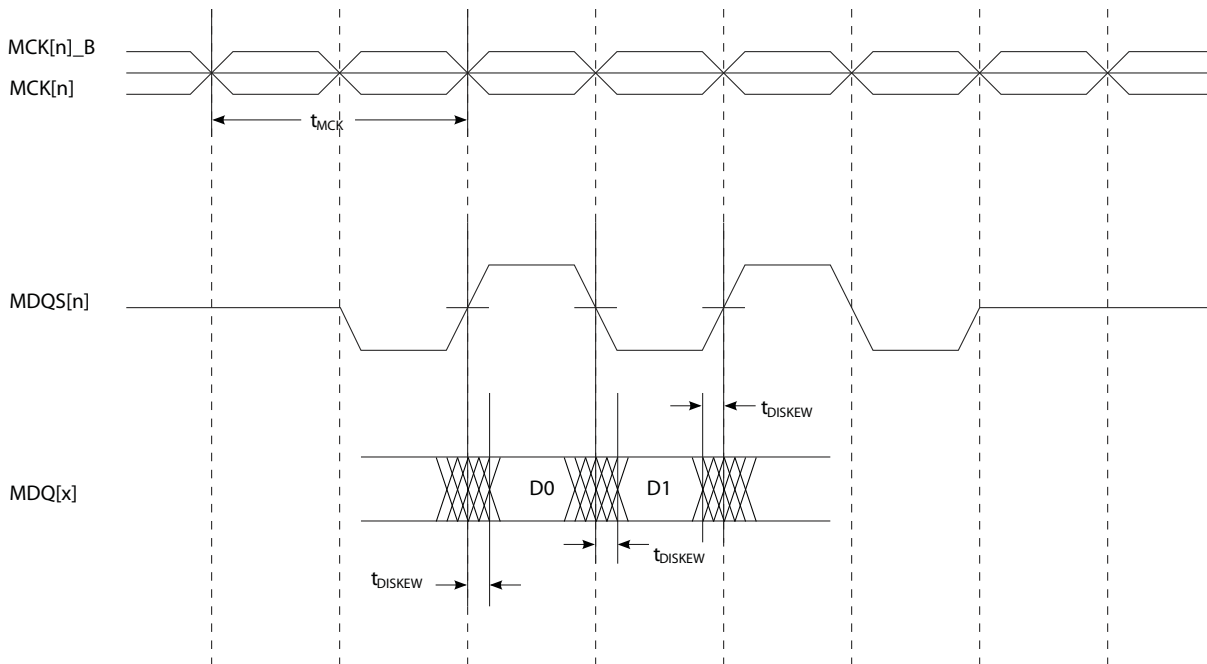
**Table 3-22.** DDR3 and DDR3L SDRAM interface input AC timing specifications<sup>(4)</sup>

| Parameter                         | Symbol       | Min  | Max | Unit | Notes  |
|-----------------------------------|--------------|------|-----|------|--------|
| Controller Skew for MDQS-MDQ/MECC | $t_{CISKEW}$ | —    | —   | ps   | (1)(3) |
| 2133 MT/s data rate               |              | –80  | 80  |      |        |
| 1866 MT/s data rate               |              | –93  | 93  |      |        |
| 1600 MT/s data rate               |              | –112 | 112 |      |        |
| 1333 MT/s data rate               |              | –125 | 125 |      |        |
| 1200 MT/s data rate               |              | –142 | 142 |      |        |
| 1066 MT/s data rate               |              | –170 | 170 |      |        |
| Tolerated Skew for MDQS-MDQ/MECC  | $t_{DISKEW}$ | —    | —   | ps   | (2)(3) |
| 2133 MT/s data rate               |              | –154 | 154 |      |        |
| 1866 MT/s data rate               |              | –175 | 175 |      |        |
| 1600 MT/s data rate               |              | –200 | 200 |      |        |
| 1333 MT/s data rate               |              | –250 | 250 |      |        |
| 1200 MT/s data rate               |              | –275 | 275 |      |        |
| 1066 MT/s data rate               |              | –300 | 300 |      |        |

- Notes:
- $t_{CISKEW}$  represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
  - The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called  $t_{DISKEW}$ . This can be determined by the following equation:  $t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))$  where T is the clock period and  $\text{abs}(t_{CISKEW})$  is the absolute value of  $t_{CISKEW}$ .
  - 2133 MT/s is only supported for DDR3, not DDR3L.
  - For recommended operating conditions, see [Table 3-2](#).

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

**Figure 3-3.** DDR3 and DDR3L SDRAM Interface Input Timing Diagram



### 3.8.2.2 DDR3 and DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

**Table 3-23.** DDR3 and DDR3L SDRAM interface output AC timing specifications<sup>(8)</sup>

| Parameter                                 | Symbol <sup>(1)</sup> | Min   | Max | Unit | Notes  |
|---|-----------------------|-------|-----|------|--------|
| MCK[n] cycle time                         | $t_{MCK}$             | 0.938 | 2   | ns   | (2)    |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$          | —     | —   | ns   | (3)(7) |
| 2133 MT/s data rate                       |                       | 0.350 | —   |      |        |
| 1866 MT/s data rate                       |                       | 0.410 | —   |      |        |
| 1600 MT/s data rate                       |                       | 0.495 | —   |      |        |
| 1333 MT/s data rate                       |                       | 0.606 | —   |      |        |
| 1200 MT/s data rate                       |                       | 0.675 | —   |      |        |
| 1066 MT/s data rate                       |                       | 0.744 | —   |      |        |
| ADDR/CMD output hold with respect to MCK  | $t_{DDKHAX}$          |       |     | ns   | (3)(7) |
| 2133 MT/s data rate                       |                       | 0.350 |     |      |        |
| 1866 MT/s data rate                       |                       | 0.390 | —   |      |        |
| 1600 MT/s data rate                       |                       | 0.495 | —   |      |        |
| 1333 MT/s data rate                       |                       | 0.606 | —   |      |        |
| 1200 MT/s data rate                       |                       | 0.675 | —   |      |        |
| 1066 MT/s data rate                       |                       | 0.744 | —   |      |        |

**Table 3-23.** DDR3 and DDR3L SDRAM interface output AC timing specifications<sup>(8)</sup> (Continued)

| Parameter                                    | Symbol <sup>(1)</sup> | Min                  | Max                  | Unit | Notes  |
|--|-----------------------|----------------------|----------------------|------|--------|
| MCK to MDQS Skew                             | $t_{DDKMHM}$          | –                    | –                    | ns   | (4)(7) |
| > 1600 MT/s data rate                        |                       | –0.150               | 0.150                |      | (4)(6) |
| > 1066 MT/s data rate, = 1600 MT/s data rate |                       | –0.245               | 0.245                |      | (4)(6) |
| MDQ/MECC/MDM output Data eye                 | $t_{DDKXDEYE}$        |                      |                      | ns   | (5)(7) |
| 2133 MT/s data rate                          |                       | 0.320                | –                    |      |        |
| 1866 MT/s data rate                          |                       | 0.350                | –                    |      |        |
| 1600 MT/s data rate                          |                       | 0.400                | –                    |      |        |
| 1333 MT/s data rate                          |                       | 0.500                | –                    |      |        |
| 1200 MT/s data rate                          |                       | 0.550                | –                    |      |        |
| 1066 MT/s data rate                          |                       | 0.600                | –                    |      |        |
| MDQS preamble                                | $t_{DDKHMP}$          | $0.9 \times t_{MCK}$ | –                    | ns   | –      |
| MDQS postamble                               | $t_{DDKHME}$          | $0.4 \times t_{MCK}$ | $0.6 \times t_{MCK}$ | ns   | –      |

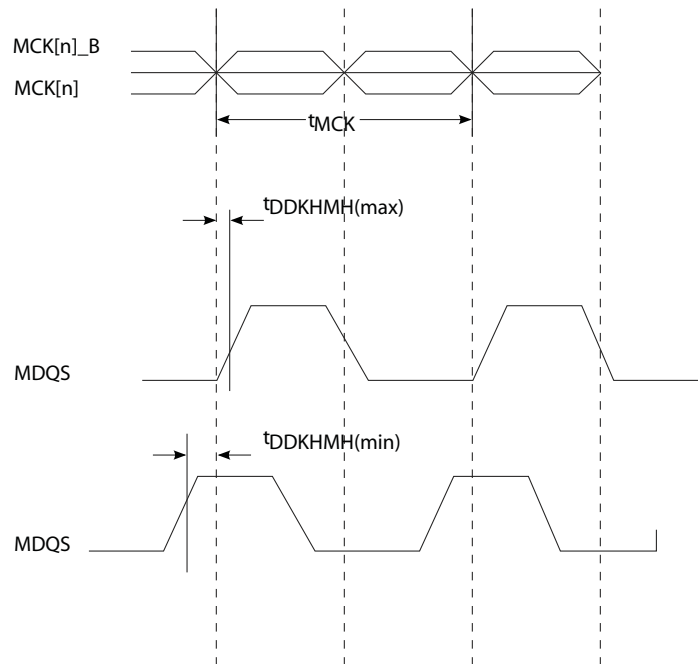
- Notes:
1. The symbols used for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example,  $t_{DDKHAS}$  symbolizes DDR timing (DD) for the time  $t_{MCK}$  memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.
  2. All MCK/MCK\_B and MDQS/MDQS\_B referenced measurements are made from the crossing of the two signals.
  3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK\_B, MCS\_B, and MDQ/MECC/MDM/MDQS.
  4. Note that  $t_{DDKMHM}$  follows the symbol conventions described in note 1. For example,  $t_{DDKMHM}$  describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH).  $t_{DDKMHM}$  can be modified through control of the MDQS override bits (called WR\_DATA\_DELAY) in the TIMING\_CFG\_2 register. This is typically set to the same delay as in DDR\_SDRAM\_CLK\_CNTL[CLK\_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.
  5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
  6. Note that for data rates of 1200 MT/s or higher, it is required to program the start value of the DQS adjust for write leveling.
  7. 2133 MT/s is only supported for DDR3, not DDR3L
  8. For recommended operating conditions, see [Table 3-2](#).

**NOTE**

For the ADDR/CMD setup and hold specifications in [Table 3-23](#), it is assumed that the clock control register is set to adjust the memory clocks by  $\frac{3}{4}$  applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement ( $t_{DDKHMH}$ ).

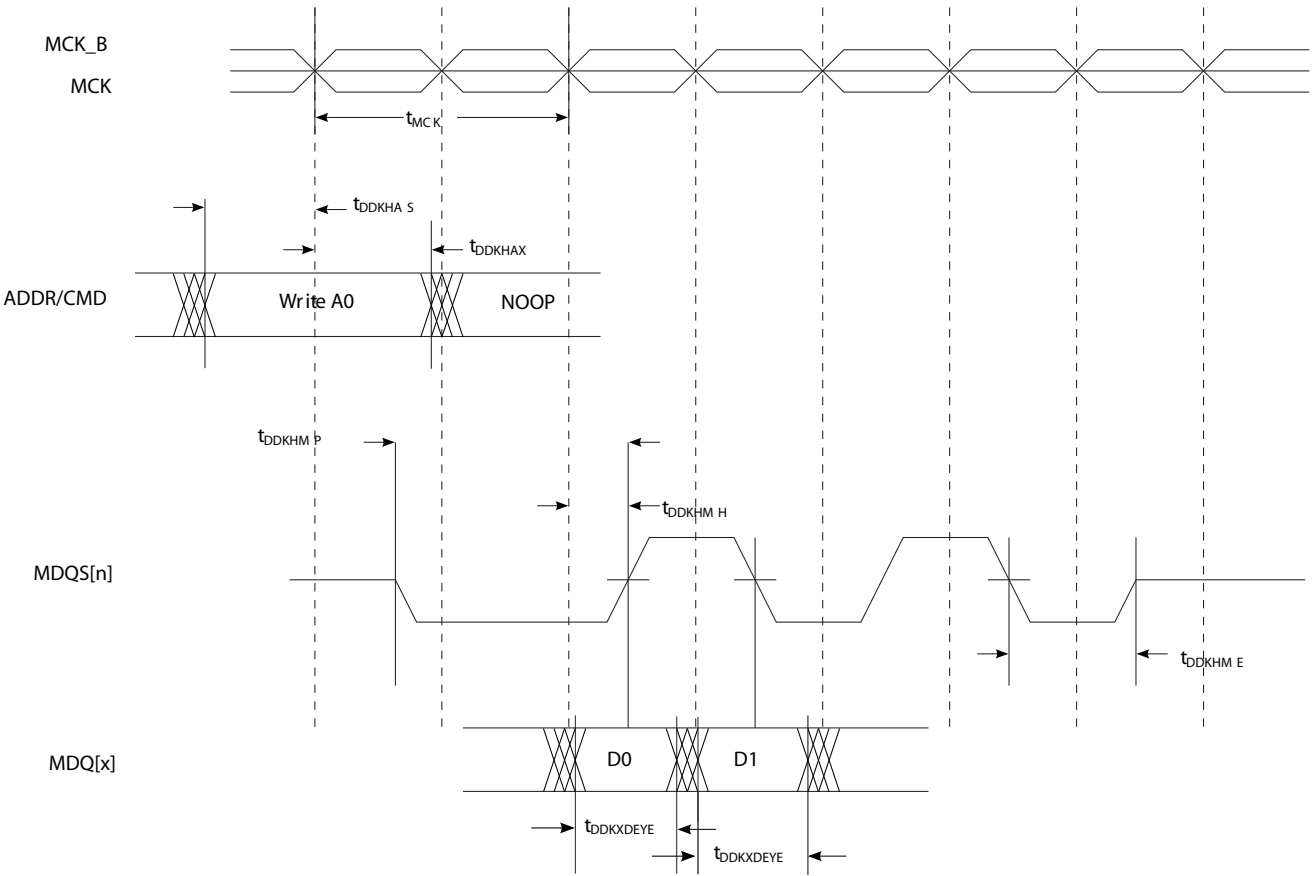
**Figure 3-4.**  $t_{DDKHMH}$  timing diagram





This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

Figure 3-5. DDR3 and DDR3L output timing diagram



3.9 eSPI interface

This section describes the DC and AC electrical specifications for the eSPI interface.

3.9.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at  $OV_{DD} = 2.5\text{ V}$ .

Table 3-24. eSPI DC electrical characteristics (2.5 V)<sup>(3)</sup>

| Parameter  | Symbol   | Min | Max | Unit          | Notes |
|--|----------|-----|-----|---------------|-------|
| Input high voltage   | $V_{IH}$ | 1.7 | –   | V             | (1)   |
| Input low voltage  | $V_{IL}$ | –   | 0.7 | V             | (1)   |
| Input current ( $OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$ )          | $I_{IN}$ | –50 | +50 | $\mu\text{A}$ | (2)   |
| Output high voltage ( $OV_{DD} = \text{min}$ , $I_{OH} = -1\text{ mA}$ ) | $V_{OH}$ | 2.0 | –   | V             | –     |
| Output low voltage ( $OV_{DD} = \text{min}$ , $I_{OL} = 1\text{ mA}$ )   | $V_{OL}$ | –   | 0.4 | V             | –     |

- Notes:
- 1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the min and max  $OV_{IN}$  respective values found in [Table 3-2](#).
  - 2. The symbol  $OV_{IN}$  represents the input voltage of the supply. It is referenced in [Recommended operating conditions](#).
  - 3. For recommended operating conditions, see [Table 3-2](#).

This table provides the DC electrical characteristics for the eSPI interface operating at  $OV_{DD} = 1.8\text{ V}$ .

**Table 3-25.** eSPI DC electrical characteristics (1.8 V)<sup>(3)</sup>

| Parameter   | Symbol   | Min  | Max      | Unit          | Notes |
|---|----------|------|----------|---------------|-------|
| Input high voltage  | $V_{IH}$ | 1.25 | —        | V             | (1)   |
| Input low voltage   | $V_{IL}$ | —    | 0.6      | V             | (1)   |
| Input current ( $V_{IN} = 0\text{ V}$ or $V_{IN} = OV_{DD}$ )                 | $I_{IN}$ | —    | $\pm 50$ | $\mu\text{A}$ | (2)   |
| Output high voltage<br>( $OV_{DD} = \text{min}$ , $I_{OH} = -0.5\text{ mA}$ ) | $V_{OH}$ | 1.35 | —        | V             | —     |
| Output low voltage<br>( $OV_{DD} = \text{min}$ , $I_{OL} = 0.5\text{ mA}$ )   | $V_{OL}$ | —    | 0.4      | V             | —     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}$  values found in Table 3-2.
  2. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Recommended operating conditions.
  3. For recommended operating conditions, see Table 3-2.

### 3.9.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

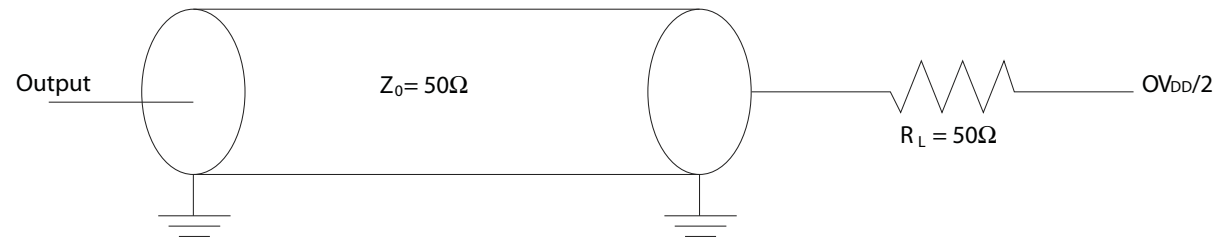
**Table 3-26.** eSPI AC timing specifications<sup>(3)</sup>

| Characteristic   | Symbol <sup>(2)</sup> | Min  | Max  | Unit | Notes     |
|--|-----------------------|--|--|------|-----------|
| SPI_MOSI output-Master data (internal clock) hold time   | $t_{NIKHOX}$          | $n1 + (t_{PLATFORM\_CLK} * SPMODE[HO\_ADJ])$ | —  | ns   | (1)(2)(4) |
| SPI_MOSI output-Master data (internal clock) delay       | $t_{NIKHOV}$          | —  | $n2 + (t_{PLATFORM\_CLK} * SPMODE[HO\_ADJ])$ | ns   | (1)(2)(4) |
| SPI_CS outputs-Master data (internal clock) hold time    | $t_{NIKHOX2}$         | 0  | —  | ns   | (1)       |
| SPI_CS outputs-Master data (internal clock) delay        | $t_{NIKHOV2}$         | —  | 6.0  | ns   | (1)       |
| SPI inputs-Master data (internal clock) input setup time | $t_{NIIVKH}$          | 3.6  | —  | ns   | —         |
| SPI inputs-Master data (internal clock) input hold time  | $t_{NIIXKH}$          | 0  | —  | ns   | —         |
| Clock-high time  | $t_{NIKCKH}$          | 4  | —  | ns   | —         |
| Clock-low time   | $t_{NIKCKL}$          | 4  | —  | ns   | —         |

- Notes:
1. See the chip reference manual for details about the SPMODE register.
  2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
  3. The symbols used for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{NIKHOV}$  symbolizes the NMSI outputs internal timing (NI) for the time  $t_{SPI}$  memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
  4. n1 and n2 values are  $-1.0$  and  $1.0$  respectively.

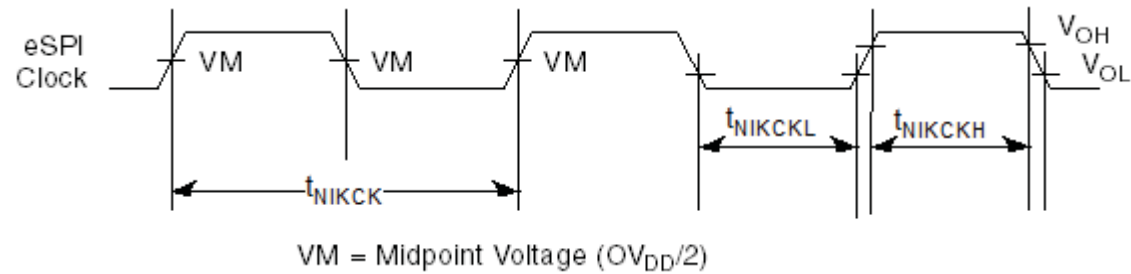
This figure provides the AC test load for the eSPI.

Figure 3-6. eSPI AC test load



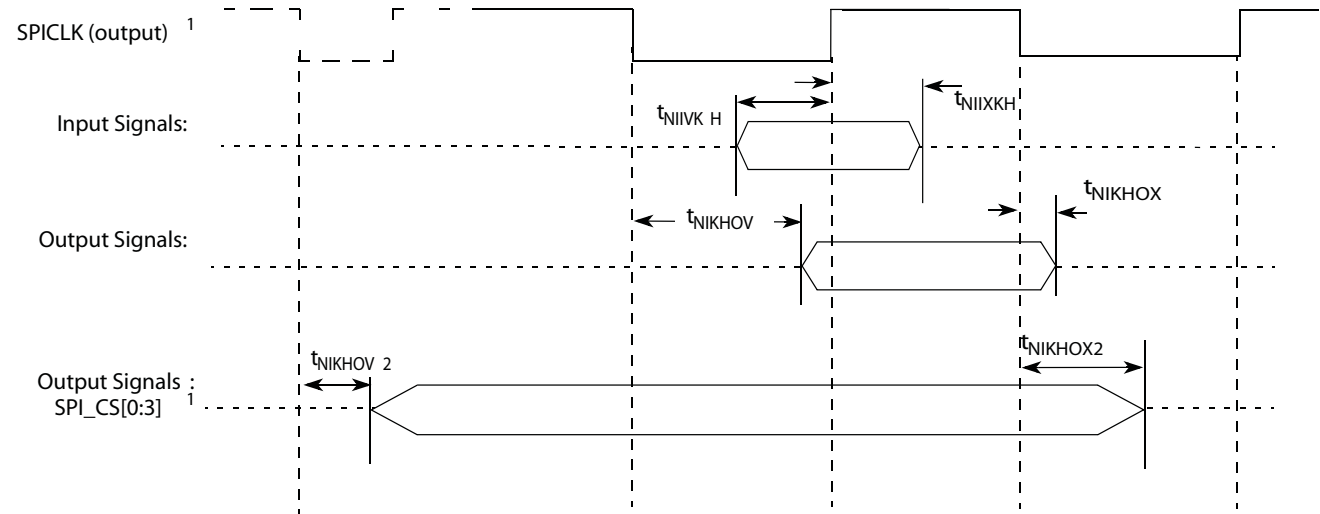
This figure provides the eSPI clock output timing diagram.

Figure 3-7. eSPI clock output timing diagram



This figure represents the AC timing from Table 3-26 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

Figure 3-8. eSPI AC timing in master mode (internal clock) diagram



3.10 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

### 3.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at  $DV_{DD} = 2.5\text{ V}$ .

**Table 3-27.** DUART DC electrical characteristics(2.5 V)<sup>(3)</sup>

| Parameter  | Symbol   | Min | Max | Unit          | Notes |
|--|----------|-----|-----|---------------|-------|
| Input high voltage   | $V_{IH}$ | 1.7 | –   | V             | (1)   |
| Input low voltage  | $V_{IL}$ | –   | 0.7 | V             | (1)   |
| Input current ( $DV_{IN} = 0\text{ V}$ or $DV_{IN} = DV_{DD}$ )          | $I_{IN}$ | –50 | +50 | $\mu\text{A}$ | (2)   |
| Output high voltage ( $DV_{DD} = \text{min}$ , $I_{OH} = -1\text{ mA}$ ) | $V_{OH}$ | 2.0 | –   | V             | –     |
| Output low voltage ( $DV_{DD} = \text{min}$ , $I_{OL} = 1\text{ mA}$ )   | $V_{OL}$ | –   | 0.4 | V             | –     |

- Notes: 1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the min and max  $DV_{IN}$  respective values found in [Table 3-2](#).  
 2. The symbol  $DV_{IN}$  represents the input voltage of the supply. It is referenced in [Recommended operating conditions](#).  
 3. For recommended operating conditions, see [Table 3-2](#).

This table provides the DC electrical characteristics for the DUART interface at  $DV_{DD} = 1.8\text{ V}$ .

**Table 3-28.** DUART DC electrical characteristics(1.8 V)<sup>(3)</sup>

| Parameter  | Symbol   | Min  | Max | Unit          | Notes |
|--|----------|------|-----|---------------|-------|
| Input high voltage   | $V_{IH}$ | 1.25 | –   | V             | (1)   |
| Input low voltage  | $V_{IL}$ | –    | 0.6 | V             | (1)   |
| Input current ( $DV_{IN} = 0\text{ V}$ or $DV_{IN} = DV_{DD}$ )            | $I_{IN}$ | –50  | +50 | $\mu\text{A}$ | (2)   |
| Output high voltage ( $DV_{DD} = \text{min}$ , $I_{OH} = -0.5\text{ mA}$ ) | $V_{OH}$ | 1.35 | –   | V             | –     |
| Output low voltage ( $DV_{DD} = \text{min}$ , $I_{OL} = 0.5\text{ mA}$ )   | $V_{OL}$ | –    | 0.4 | V             | –     |

- Notes: 1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the min and max  $DV_{IN}$  respective values found in [Table 3-2](#).  
 2. The symbol  $DV_{IN}$  represents the input voltage of the supply. It is referenced in [Recommended operating conditions](#).  
 3. For recommended operating conditions, see [Table 3-2](#).

### 3.10.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

**Table 3-29.** DUART AC timing specifications

| Parameter         | Value                           | Unit | Notes  |
|-------------------|---------------------------------|------|--------|
| Minimum baud rate | $f_{PLAT}/(2 \times 1,048,576)$ | baud | (1)(3) |
| Maximum baud rate | $f_{PLAT}/(2 \times 16)$        | baud | (1)(2) |

- Notes: 1.  $f_{PLAT}$  refers to the internal platform clock.  
 2. The actual attainable baud rate is limited by the latency of interrupt processing.  
 3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.

## 3.11 Ethernet interface, Ethernet management interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interfaces.

## 3.11.1 SGMII electrical specifications

See SGMII interface.

## 3.11.2 RGMII electrical specifications

This section discusses the electrical characteristics for the RGMII interface.

### 3.11.2.1 RGMII DC electrical characteristics

This table shows the DC electrical characteristics for the RGMII interface.

**Table 3-30.** RGMII DC electrical characteristics (LVDD = 2.5 V)<sup>(3)</sup>

| Parameters   | Symbol   | Min       | Max             | Unit | Notes |
|--|----------|-----------|-----------------|------|-------|
| Input high voltage   | $V_{IH}$ | 1.70      | —               | V    | (1)   |
| Input low voltage  | $V_{IL}$ | —         | 0.70            | V    | (1)   |
| Input current ( $V_{IN} = 0$ V or $V_{IN} = LV_{DD}$ )             | $I_{IH}$ | −50       | +50             | μA   | (2)   |
| Output high voltage ( $LV_{DD} = \text{min}$ , $I_{OH} = -1.0$ mA) | $V_{OH}$ | 2.00      | $LV_{DD} + 0.3$ | V    | —     |
| Output low voltage ( $LV_{DD} = \text{min}$ , $I_{OL} = 1.0$ mA)   | $V_{OL}$ | GND − 0.3 | 0.40            | V    | —     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $LV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $LV_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in [Recommended operating conditions](#).
  3. For recommended operating conditions, see [Table 3-2](#).

### 3.11.2.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

**Table 3-31.** RGMII AC timing specifications (LVDD = 2.5 V)<sup>(8)</sup>

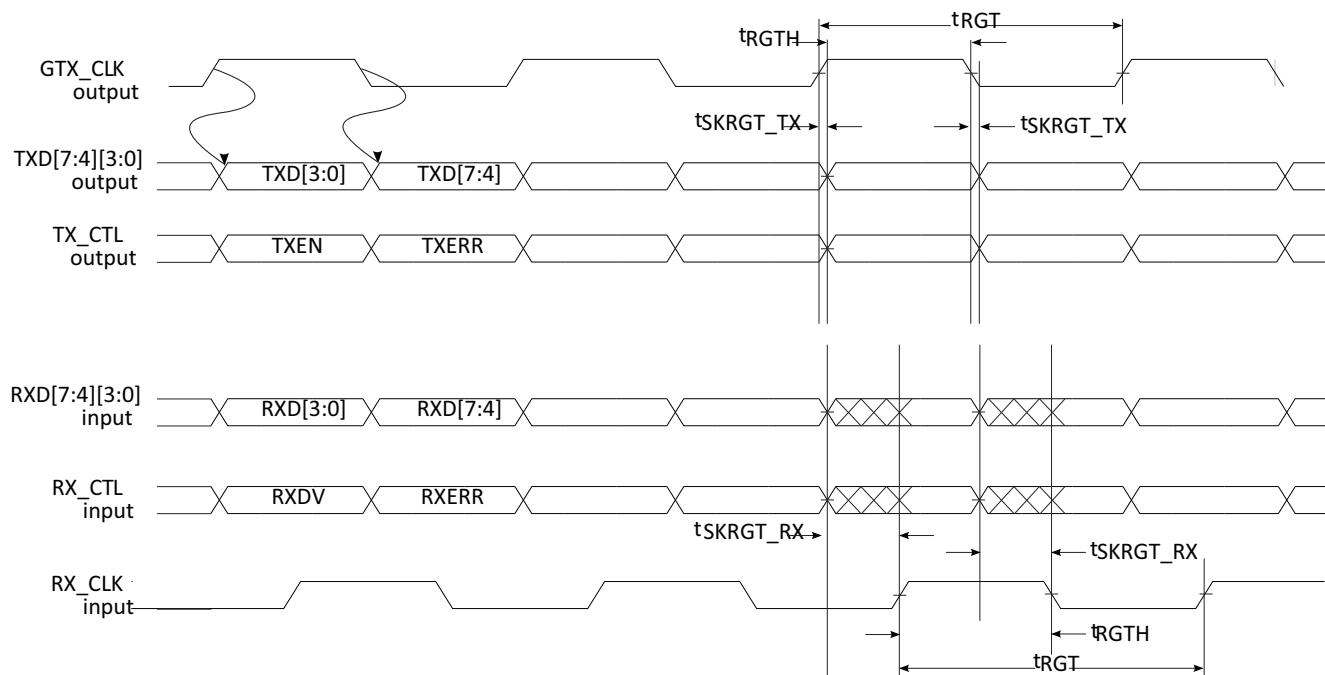
| Parameter/Condition                        | Symbol <sup>(1)</sup> | Min  | Typ | Max  | Unit | Notes  |
|--|-----------------------|------|-----|------|------|--------|
| Data to clock output skew (at transmitter) | $t_{SKRGT\_TX}$       | −750 | 0   | 1000 | ps   | (7)(9) |
| Data to clock input skew (at receiver)     | $t_{SKRGT\_RX}$       | 1.0  | —   | 2.6  | ns   | (2)    |
| Clock period duration                      | $t_{RGT}$             | 7.2  | 8.0 | 8.8  | ns   | (3)    |
| Duty cycle for 10BASE-T and 100BASE-TX     | $t_{RGTH}/t_{RGT}$    | 40   | 50  | 60   | %    | (3)(4) |
| Duty cycle for Gigabit                     | $t_{RGTH}/t_{RGT}$    | 45   | 50  | 55   | %    | —      |
| Rise time (20%-80%)                        | $t_{RGTR}$            | —    | —   | 0.75 | ns   | (5)(6) |
| Fall time (20%-80%)                        | $t_{RGTF}$            | —    | —   | 0.75 | ns   | (5)(6) |

- Notes:
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
  2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
  3. For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
  4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{RGT}$  of the lowest speed transitioned between.
  5. Applies to inputs and outputs.

6. System/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
  7. The frequency of ECn\_RX\_CLK (input) should not exceed the frequency of ECn\_GTX\_CLK (output) by more than 300 ppm.
  8. For recommended operating conditions, see [Table 3-2](#).
  9. IEEE specification mandates  $t_{SKRG\overline{T}_{TX}} = \pm 0.5$  ns. Per erratum A-005177, we see  $t_{SKRG\overline{T}_{TX}}$  has a wider output skew range from  $-0.75$  ns to  $1.00$  ns, which is larger than the specification asks for. If the device cannot cope with this wide skew, use RGMII at 100 Mbps or 10 Mbps, which allows larger maximum RX skews, or terminate 1000 Mbps RGMII links with PHYs that accommodate larger RX skews.
- NOTE: MAC10 is not impacted by erratum A-005177, and it meets industry specifications.

This figure shows the RGMII AC timing and multiplexing diagrams.

**Figure 3-9.** RGMII AC timing and multiplexing diagrams



**Warning**

TELEDYNE e2v guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

### 3.11.3 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces. Frame Manager's external GE MDIO configures external GE PHYs connected to EMI1 pins.

Frame Manager's external 10GE MDIO configures external XFI, XAUI, and HiGig/HiGig2 PHY connected to EMI2 pins.

The EMI1 interface timing is compatible with IEEE Std 802.3 clause 22 and EMI2 interface timing is compatible with IEEE Std 802.3 clause 45.

## 3.11.3.1 Ethernet management interface 1 DC electrical characteristics

The DC electrical characteristics for EMI1\_MDIO and EMI1\_MDC are provided in this section.

**Table 3-32.** Ethernet management interface 1 DC electrical characteristics (LVDD = 2.5 V)<sup>(3)</sup>

| Parameters   | Symbol   | Min         | Max             | Unit    | Notes |
|--|----------|-------------|-----------------|---------|-------|
| Input high voltage   | $V_{IH}$ | 1.70        | –               | V       | (1)   |
| Input low voltage  | $V_{IL}$ | –           | 0.70            | V       | (1)   |
| Input high current ( $V_{IN} = LVDD$ )                       | $I_{IH}$ | –           | 50              | $\mu A$ | (2)   |
| Input low current ( $V_{IN} = GND$ )                         | $I_{IL}$ | –50         | –               | $\mu A$ | –     |
| Output high voltage ( $LV_{DD} = \min$ , $I_{OH} = -1.0$ mA) | $V_{OH}$ | 2.00        | $LV_{DD} + 0.3$ | V       | –     |
| Output low voltage ( $LV_{DD} = \min$ , $I_{OL} = 1.0$ mA)   | $V_{OL}$ | $GND - 0.3$ | 0.40            | V       | –     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $LV_{IN}$  values found in Table 3-2.
  2. The symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in Recommended operating conditions.
  3. For recommended operating conditions, see Table 3-2.

**Table 3-33.** Ethernet management interface 1 DC electrical characteristics (LVDD = 1.8 V)<sup>(3)</sup>

| Parameter  | Symbol   | Min  | Max  | Unit    | Notes |
|--|----------|------|------|---------|-------|
| Input high voltage   | $V_{IH}$ | 1.25 | –    | V       | (1)   |
| Input low voltage  | $V_{IL}$ | –    | 0.60 | V       | (1)   |
| Input current ( $LV_{IN} = 0V$ or $LV_{IN} = LV_{DD}$ )      | $I_{IN}$ | –50  | 50   | $\mu A$ | (2)   |
| Output high voltage ( $LV_{DD} = \min$ , $I_{OH} = -0.5$ mA) | $V_{OH}$ | 1.35 | –    | V       | –     |
| Output low voltage ( $LV_{DD} = \min$ , $I_{OL} = 0.5$ mA)   | $V_{OL}$ | –    | 0.40 | V       | –     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}/QV_{IN}$  values found in Table 3.
  2. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 3-2.

## 3.11.3.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. The DC electrical characteristics for EMI2\_MDIO and EMI2\_MDC are provided in this section.

**Table 3-34.** Ethernet management interface 2 DC electrical characteristics (1.2 V)<sup>(1)</sup>

| Parameter          | Symbol   | Min  | Max  | Unit | Notes |
|--------------------|----------|------|------|------|-------|
| Input high voltage | $V_{IH}$ | 0.84 | –    | V    | –     |
| Input low voltage  | $V_{IL}$ | –    | 0.36 | V    | –     |

**Table 3-34.** Ethernet management interface 2 DC electrical characteristics (1.2 V)<sup>(1)</sup>

|   |          |   |     |    |   |
|---|----------|---|-----|----|---|
| Output low voltage ( $I_{OL} = 100 \mu A$ ) | $V_{OL}$ | – | 0.2 | V  | – |
| Output low current ( $V_{OL} = 0.2 V$ )     | $I_{OL}$ | 4 | –   | mA | – |
| Input capacitance                           | $C_{IN}$ | – | 10  | pF | – |

Note: 1. For recommended operating conditions, see [Table 3-2](#)

### 3.11.3.3 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC timing specifications.

**Table 3-35.** Ethernet management interface 1 AC timing specifications<sup>(5)</sup>

| Parameter/Condition        | Symbol <sup>1</sup> | Min                            | Typ | Max                            | Unit | Notes  |
|----------------------------|---------------------|--------------------------------|-----|--------------------------------|------|--------|
| MDC frequency              | $f_{MDC}$           | –                              | –   | 2.5                            | MHz  | (2)    |
| MDC clock pulse width high | $t_{MDCH}$          | 160                            | –   | –                              | ns   | –      |
| MDC to MDIO delay          | $t_{MDKHDX}$        | $(5 \times t_{enet\_clk}) - 3$ | –   | $(5 \times t_{enet\_clk}) + 3$ | ns   | (3)(4) |
| MDIO to MDC setup time     | $t_{MDDVKH}$        | 8                              | –   | –                              | ns   | –      |
| MDIO to MDC hold time      | $t_{MDDXKH}$        | 0                              | –   | –                              | ns   | –      |

- Notes: 1. The symbols used for timing specifications follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{MDKHDX}$  symbolizes management data timing (MD) for the time  $t_{MDC}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{MDDVKH}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{MDC}$  clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency (MDIO\_CFG [MDIO\_CLK\_DIV] field determines the clock frequency of the MgmtClk Clock EC\_MDC).
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods  $\pm 3$  ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns  $\pm 3$  ns.
4.  $t_{enet\_clk}$  is the Ethernet clock period (Frame Manager clock period).
5. For recommended operating conditions, see [Table 3-2](#).

### 3.11.3.4 Ethernet management interface 2 AC electrical characteristics

This table provides the Ethernet management interface 2 AC timing specifications.

**Table 3-36.** Ethernet management interface 2 AC timing specifications<sup>(5)</sup>

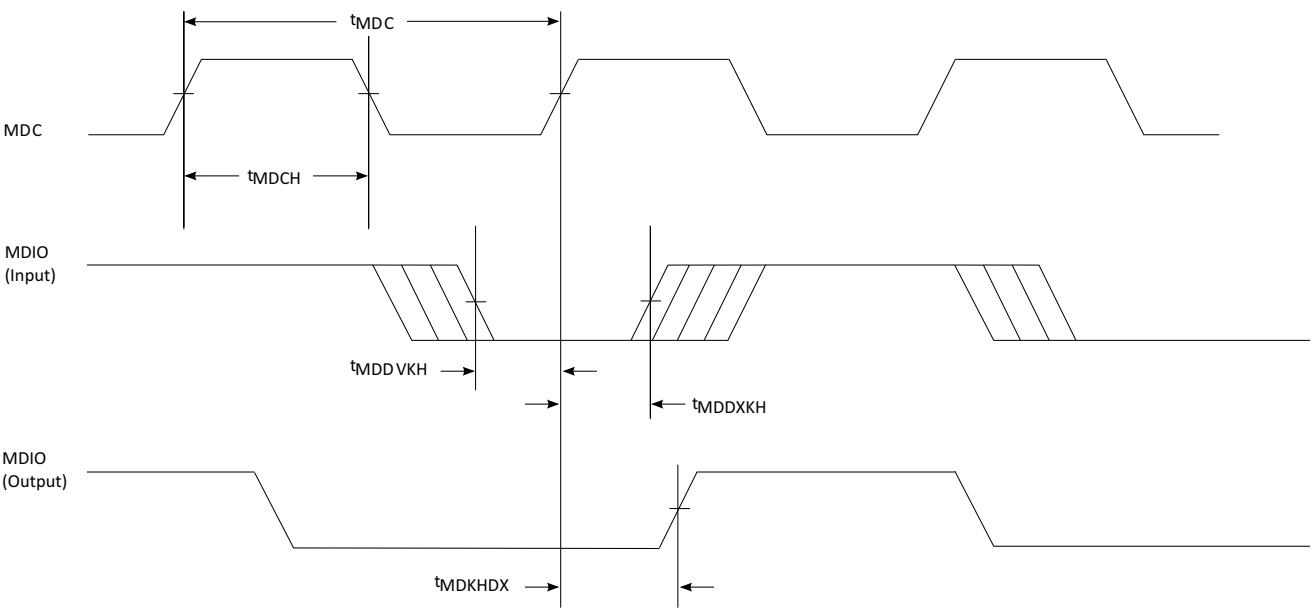
| Parameter/Condition        | Symbol <sup>(1)</sup> | Min                            | Typ | Max                            | Unit | Notes |
|----------------------------|-----------------------|--------------------------------|-----|--------------------------------|------|-------|
| MDC frequency              | $f_{MDC}$             | 2.5                            | –   | –                              | MHz  | 2     |
| MDC clock pulse width high | $t_{MDCH}$            | 160                            | –   | –                              | ns   | –     |
| MDC to MDIO delay          | $t_{MDKHDX}$          | $(5 \times t_{enet\_clk}) - 3$ | –   | $(5 \times t_{enet\_clk}) + 3$ | ns   | 3, 4  |
| MDIO to MDC setup time     | $t_{MDDVKH}$          | 8                              | –   | –                              | ns   | –     |
| MDIO to MDC hold time      | $t_{MDDXKH}$          | 0                              | –   | –                              | ns   | –     |



- Notes:
- 1. The symbols used for timing specifications follow the pattern of  $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$  for inputs and  $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$  for outputs. For example,  $t_{\text{MDKHDX}}$  symbolizes management data timing (MD) for the time  $t_{\text{MDC}}$  from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also,  $t_{\text{MDDVKH}}$  symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the  $t_{\text{MDC}}$  clock reference (K) going to the high (H) state or setup time.
  - 2. This parameter is dependent on the Ethernet clock frequency (MDIO\_CFG [MDIO\_CLK\_DIV] field determines the clock frequency of the MgmtClk Clock EC\_MDC).
  - 3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods  $\pm$  3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns  $\pm$  3 ns.
  - 4.  $t_{\text{enet\_clk}}$  is the Ethernet clock period (Frame Manager clock period).
  - 5. For recommended operating conditions, see [Table 3-2](#).

This figure shows the Ethernet management interface timing diagram

Figure 3-10. Ethernet management interface timing diagram



3.11.4 IEEE 1588 electrical specifications

3.11.4.1 IEEE 1588 DC

This table shows IEEE 1588 DC electrical characteristics when operating at  $V_{\text{DD}} = 2.5$  V supply.

Table 3-37. IEEE 1588 DC electrical characteristics ( $V_{\text{DD}} = 2.5$  V)<sup>3</sup>

| Parameters  | Symbol          | Min                | Max                   | Unit          | Notes |
|---|-----------------|--------------------|-----------------------|---------------|-------|
| Input high voltage  | $V_{\text{IH}}$ | 1.70               | –                     | V             | (1)   |
| Input low voltage   | $V_{\text{IL}}$ | –                  | 0.70                  | V             | (1)   |
| Input current ( $V_{\text{IN}} = 0$ V or $V_{\text{IN}} = V_{\text{DD}}$ )      | $I_{\text{IH}}$ | –50                | +50                   | $\mu\text{A}$ | 2     |
| Output high voltage ( $V_{\text{DD}} = \text{min}$ , $I_{\text{OH}} = -1.0$ mA) | $V_{\text{OH}}$ | 2.00               | $V_{\text{DD}} + 0.3$ | V             | –     |
| Output low voltage ( $V_{\text{DD}} = \text{min}$ , $I_{\text{OL}} = 1.0$ mA)   | $V_{\text{OL}}$ | $\text{GND} - 0.3$ | 0.40                  | V             | –     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $LV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $LV_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in Recommended operating conditions.
  3. For recommended operating conditions, see [Table 3-2](#).

This table shows IEEE 1588 DC electrical characteristics when operating at  $LVDD = 1.8$  V supply.

**Table 3-38.** IEEE 1588 DC electrical characteristics ( $LVDD = 1.8$  V)<sup>(3)</sup>

| Parameters   | Symbol   | Min       | Max             | Unit    | Notes |
|--|----------|-----------|-----------------|---------|-------|
| Input high voltage   | $V_{IH}$ | 1.25      | –               | V       | (1)   |
| Input low voltage  | $V_{IL}$ | –         | 0.6             | V       | (1)   |
| Input current ( $LV_{IN} = 0$ V or $LV_{IN} = LV_{DD}$ )           | $I_{IH}$ | –50       | +50             | $\mu$ A | 2     |
| Output high voltage ( $LV_{DD} = \text{min}$ , $I_{OH} = -0.5$ mA) | $V_{OH}$ | 1.35      | $LV_{DD} + 0.3$ | V       | –     |
| Output low voltage ( $LV_{DD} = \text{min}$ , $I_{OL} = 0.5$ mA)   | $V_{OL}$ | GND – 0.3 | 0.40            | V       | –     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $LV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $LV_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in Recommended operating conditions.
  3. For recommended operating conditions, see [Table 3-2](#).

#### 3.11.4.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

**Table 3-39.** IEEE 1588 AC timing specifications<sup>(5)</sup>

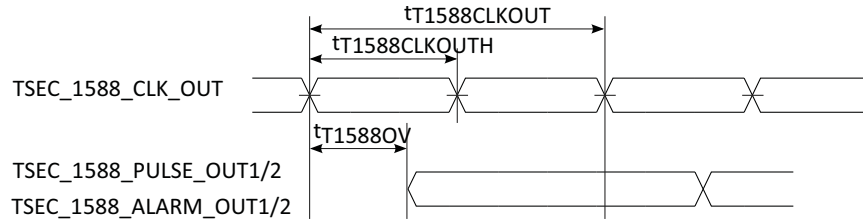
| Parameter/Condition                               | Symbol                              | Min                          | Typ | Max                    | Unit | Notes |
|---|-------------------------------------|------------------------------|-----|------------------------|------|-------|
| TSEC_1588_CLK_IN clock period                     | $t_{T1588CLK}$                      | 3.3                          | –   | $T_{RX\_CLK} \times 7$ | ns   | 1, 3  |
| TSEC_1588_CLK_IN duty cycle                       | $t_{T1588CLKH} / t_{T1588CLK}$      | 40                           | 50  | 60                     | %    | 2     |
| TSEC_1588_CLK_IN peak-to-peak jitter              | $t_{T1588CLKINJ}$                   | –                            | –   | 250                    | ps   | –     |
| Rise time TSEC_1588_CLK_IN (20% -80%)             | $t_{T1588CLKINR}$                   | 1.0                          | –   | 2.0                    | ns   | –     |
| Fall time TSEC_1588_CLK_IN (80% –20%)             | $t_{T1588CLKINF}$                   | 1.0                          | –   | 2.0                    | ns   | –     |
| TSEC_1588_CLK_OUT clock period                    | $t_{T1588CLKOUT}$                   | 5.0                          | –   | –                      | ns   | 4     |
| TSEC_1588_CLK_OUT duty cycle                      | $t_{T1588CLKOTH} / t_{T1588CLKOUT}$ | 30                           | 50  | 70                     | %    | –     |
| TSEC_1588_PULSE_OUT1/2,<br>TSEC_1588_ALARM_OUT1/2 | $t_{T1588OV}$                       | 0.5                          | –   | 3.0                    | ns   | –     |
| TSEC_1588_TRIG_IN1/2 pulse width                  | $t_{T1588TRIGH}$                    | $2 \times t_{T1588CLK\_MAX}$ | –   | –                      | ns   | 3     |

- Notes:
1.  $TRX\_CLK$  is the maximum clock period of ethernet receiving clock selected by  $TMR\_CTRL[CKSEL]$ . See the chip reference manual for a description of  $TMR\_CTRL$  registers.

2. It needs to be at least two times the clock period of the clock selected by TMR\_CTRL[CKSEL]. See the chip reference manual for a description of TMR\_CTRL registers.
3. The maximum value of tT1588CLK is not only defined by the value of TRX\_CLK, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of tT1588CLK will be 2800, 280, and 56 ns, respectively.
4. There are 3 input clock sources for 1588 i.e. TSEC\_1588\_CLK\_IN, RTC and MAC clock / 2. When using TSEC\_1588\_CLK\_IN, the minimum clock period is  $2 \times tT1588CLK$ .
5. For recommended operating conditions, see [Table 3-2](#).

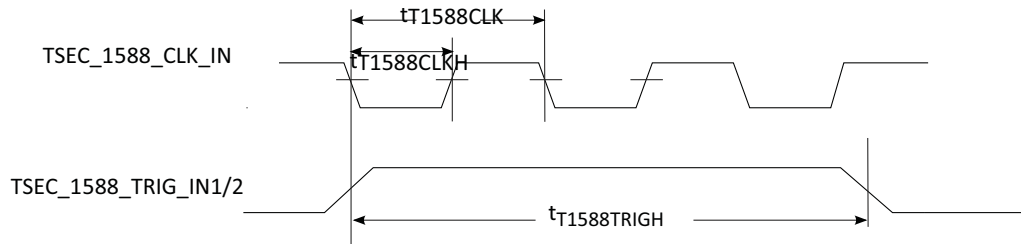
This figure shows the data and command output AC timing diagram.

**Figure 3-11.** IEEE 1588 output AC timing



This figure shows the data and command input AC timing diagram.

**Figure 3-12.** IEEE 1588 input AC timing



## 3.12 USB interface

This section provides the AC and DC electrical specifications for the USB interface.

### 3.12.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB\_HVDD = 3.3 V.

**Table 3-40.** USB DC electrical characteristics (USB\_HVDD = 3.3 V)<sup>(3)</sup>

| Parameter   | Symbol   | Min  | Max  | Unit    | Notes  |
|---|----------|------|------|---------|--------|
| Input high voltage                                    | $V_{IH}$ | 2.0  | –    | V       | (1)(4) |
| Input low voltage                                     | $V_{IL}$ | –    | 0.8  | V       | (1)(4) |
| Input current (USB_HVIN = 0 V or USB_HVIN = USB_HVDD) | $I_{IN}$ | –100 | +100 | $\mu A$ | (2)(4) |
| Output high voltage (USB_HVDD = min, IOH = –2 mA)     | $V_{OH}$ | 2.8  | –    | V       | (5)    |
| Output low voltage (USB_HVDD = min, IOL = 2 mA)       | $V_{OL}$ | –    | 0.3  | V       | (5)    |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max USB\_HVIN values found in [Table 3-2](#).
  2. The symbol USB\_HVIN, in this case, represents the USB\_HVIN symbol referenced in Recommended operating conditions

3. For recommended operating conditions, see [Table 3-2](#)
4. These specifications only apply to the following pins: USB1\_PWRFAULT, USB2\_PWRFAULT, USB1\_UDM (full-speed mode), USB2\_UDM (full-speed mode), USB1\_UDP (full-speed mode), and USB2\_UDP (full-speed mode).
5. This specification only applies to USB1\_DRVVBUS and USB2\_DRVVBUS pins.

This table provides the DC electrical characteristics for the USBCLK at  $OV_{DD} = 1.8\text{ V}$ .

**Table 3-41.** USBCLK DC electrical characteristics (1.8 V)<sup>(3)</sup>

| Parameter   | Symbol   | Min  | Max  | Unit | Notes |
|---|----------|------|------|------|-------|
| Input high voltage  | $V_{IH}$ | 1.25 | –    | V    | (1)   |
| Input low voltage   | $V_{IL}$ | –    | 0.6  | V    | (1)   |
| Input current ( $V_{IN} = 0\text{ V}$ or $V_{IN} = OV_{DD}$ ) | $I_{IN}$ | –    | ±100 | μA   | (2)   |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Recommended operating conditions.
  3. For recommended operating conditions, see [Table 3-2](#).

### 3.12.2 USB AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

This table provides the USB clock input (USBCLK) AC timing specifications.

**Table 3-42.** USBCLK AC timing specifications<sup>1</sup>

| Parameter                              | Condition  | Symbol             | Min   | Typ | Max  | Unit | Notes |
|--|--|--------------------|-------|-----|------|------|-------|
| Frequency range                        | –  | $f_{USB\_CLK\_IN}$ | –     | 24  | –    | MHz  | –     |
| Rise/Fall time                         | Measured between 10% and 90%   | $t_{USRF}$         | –     | –   | 6    | ns   | 2     |
| Clock frequency tolerance              | –  | $t_{CLK\_TOL}$     | –0.01 | 0   | 0.01 | %    | –     |
| Reference clock duty cycle             | Measured at rising edge and/or failing edge at $OV_{DD}/2$   | $t_{CLK\_DUTY}$    | 40    | 50  | 60   | %    | –     |
| Total input jitter/time interval error | RMS value measured with a second-order, band-pass filter of 500 kHz to 4 MHz bandwidth at $10^{-12}$ BER | $t_{CLK\_PJ}$      | –     | –   | 5    | ps   | –     |

- Notes:
1. For recommended operating conditions, see [Table 3-2](#)
  2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.13 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.13.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at  $OV_{DD}=1.8\text{ V}$ .

Table 3-43. Integrated flash controller DC electrical characteristics (1.8 V)<sup>(3)</sup>

| Parameter   | Symbol   | Min  | Max | Unit          | Note |
|---|----------|------|-----|---------------|------|
| Input high voltage  | $V_{IH}$ | 1.25 | –   | V             | (1)  |
| Input low voltage   | $V_{IL}$ | –    | 0.6 | V             | (1)  |
| Input current<br>( $V_{IN}=0\text{ V}$ or $V_{IN}=OV_{DD}$ )              | $I_{IN}$ | –50  | +50 | $\mu\text{A}$ | 2    |
| Output high voltage<br>( $OV_{DD}=\text{min}$ , $I_{OH}=-0.5\text{ mA}$ ) | $V_{OH}$ | 1.35 | –   | V             | –    |
| Output low voltage<br>( $OV_{DD}=\text{min}$ , $I_{OL}=0.5\text{ mA}$ )   | $V_{OL}$ | –    | 0.4 | V             | –    |

- Notes:
- 1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}$  values found in [Table 3-2](#).
  - 2. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in [Recommended operating conditions](#).
  - 3. For recommended operating conditions, see [Table 3-2](#).

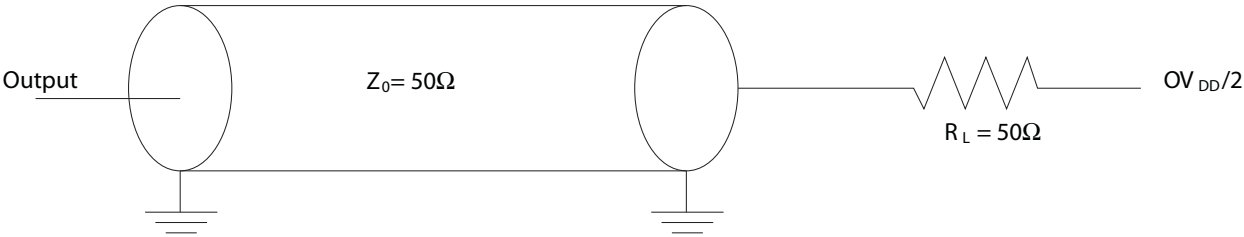
3.13.2 Integrated flash controller AC timing

This section describes the AC timing specifications for the integrated flash controller.

3.13.2.1 Test condition

This figure provides the AC test load for the integrated flash controller.

Figure 3-13. Integrated flash controller AC test load



3.13.2.2 Integrated flash controller AC timing specifications

All output signal timings are relative to the falling edge of any IFC\_CLK. The external circuit must use the rising edge of the IFC\_CLKs to latch the data.

All input timings are relative to the rising edge of IFC\_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

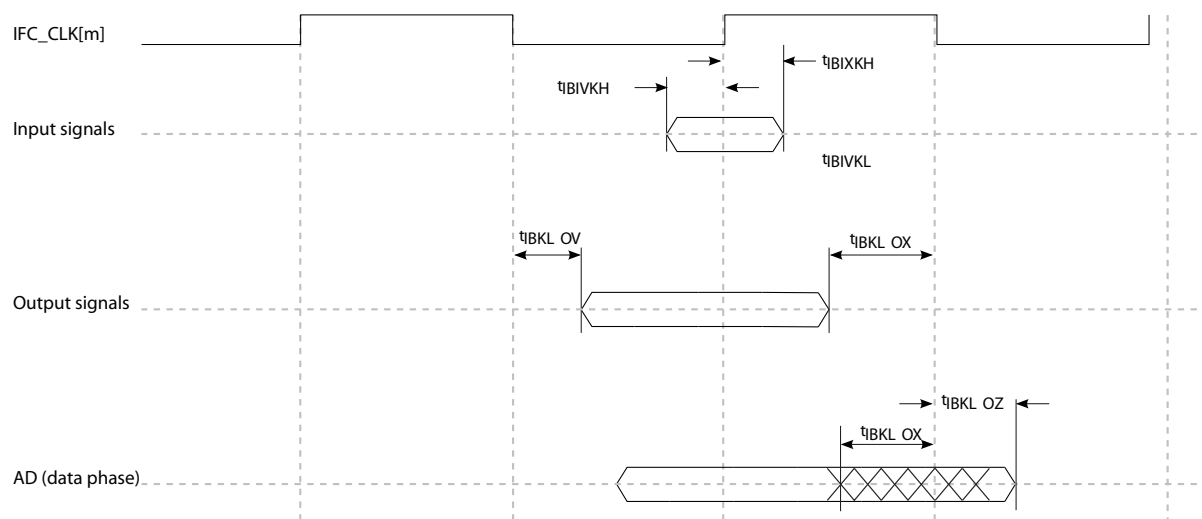
**Table 3-44.** Integrated flash controller timing specifications (OVDD = 1.8 V)<sup>(5)</sup>

| Parameter                               | Symbol <sup>(1)</sup> | Min | Max | Unit | Notes |
|---|-----------------------|-----|-----|------|-------|
| IFC_CLK cycle time                      | $t_{IBK}$             | 10  | —   | ns   | —     |
| IFC_CLK duty cycle                      | $t_{IBKH}/t_{IBK}$    | 45  | 55  | %    | —     |
| IFC_CLK[n] skew to IFC_CLK[m]           | $t_{IBKSKEW}$         | —   | 150 | ps   | (2)   |
| Input setup                             | $t_{IBIVKH}$          | 4   | —   | ns   | —     |
| Input hold                              | $t_{IBIXKH}$          | 1   | —   | ns   | —     |
| Output delay                            | $t_{IBKLOV}$          | —   | 2.5 | ns   | —     |
| Output hold                             | $t_{IBKLOX}$          | –2  | —   | ns   | (4)   |
| IFC_CLK to output high impedance for AD | $t_{IBKLOZ}$          | —   | 2   | ns   | (3)   |

- Notes:
1. All signals are measured from  $OV_{DD}/2$  of rising/falling edge of IFC\_CLK to  $OV_{DD}/2$  of the signal in question.
  2. Skew measured between different IFC\_CLK signals at  $OV_{DD}/2$ .
  3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
  4. Here the negative sign means output transit happens earlier than the falling edge of IFC\_CLK.
  5. For recommended operating conditions, see [Table 3-2](#).

This figure shows the AC timing diagram.

**Figure 3-14.** Integrated flash controller signals



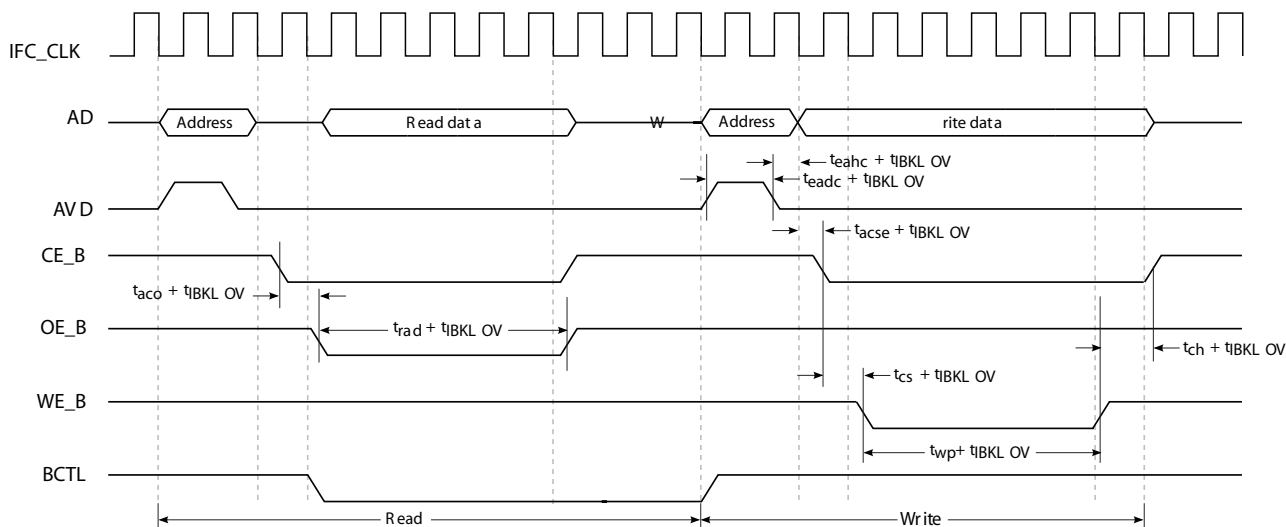
The figure above applies to all the controllers that IFC supports.

- For input signals, the AC timing data is used directly for all controllers.
- For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.

Notes for figure:

**Figure 3-15.** GPCM output timing diagram<sup>1,2</sup>



1.  $t_{aco}$ ,  $t_{rad}$ ,  $t_{eahc}$ ,  $t_{eadc}$ ,  $t_{acse}$ ,  $t_{cs}$ ,  $t_{ch}$ ,  $t_{wp}$  are programmable. See the chip reference manual.
2. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

## 3.14 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

### 3.14.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

**Table 3-45.** eSDHC interface DC electrical characteristics (dual-voltage cards)<sup>(3)</sup>

| Characteristic               | Symbol          | Condition                             | Min                 | Max                 | Unit    | Notes |
|------------------------------|-----------------|---------------------------------------|---------------------|---------------------|---------|-------|
| Input high voltage           | $V_{IH}$        | —                                     | $0.7 \times V_{DD}$ | —                   | V       | (1)   |
| Input low voltage            | $V_{IL}$        | —                                     | —                   | $0.2 \times V_{DD}$ | V       | (1)   |
| Input/Output leakage current | $I_{IN}/I_{OZ}$ | —                                     | –50                 | 50                  | $\mu A$ | —     |
| Output high voltage          | $V_{OH}$        | $I_{OH} = -100 \mu A$ at $V_{DD}$ min | $V_{DD} - 0.2$      | —                   | V       | —     |
| Output low voltage           | $V_{OL}$        | $I_{OL} = 100 \mu A$ at $V_{DD}$ min  | —                   | 0.2                 | V       | —     |
| Output high voltage          | $V_{OH}$        | $I_{OH} = -100 \mu A$                 | $V_{DD} - 0.2$      | —                   | V       | (2)   |
| Output low voltage           | $V_{OL}$        | $I_{OL} = 2$ mA                       | —                   | 0.3                 | V       | (2)   |

Notes: 1. The min  $V_{IL}$  and  $V_{IH}$  values are based on the respective min and max  $V_{IN}$  values found in [Table 3-2](#).

2. Open-drain mode is for MMC cards only.

3. For recommended operating conditions, see [Table 3-2](#).

4. SDHC interface is powered by  $OV_{DD}$  and  $CV_{DD}$ . The  $V_{DD}$  and  $V_{IN}$  in the table above should be replaced by the respective I/O power supply.

### 3.14.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in [Figure 3-16](#) and [Figure 3-17](#) ( $OV_{DD}/CV_{DD} = 1.8V$  or  $3.3V$ ).

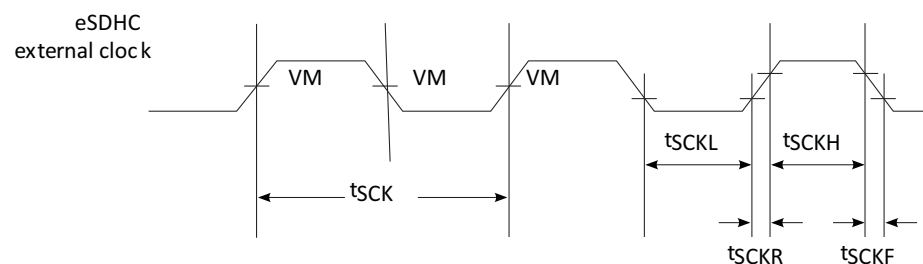
**Table 3-46.** eSDHC AC timing specifications (High Speed/Full Speed)<sup>(6)</sup>

| Parameter  |                                      | Symbol <sup>1</sup> | Min  | Max   | Unit | Notes   |
|--|--------------------------------------|---------------------|------|-------|------|---------|
| SDHC_CLK clock frequency                                 | SD/SDIO (full-speed/high-speed mode) | $f_{SCK}$           | 0    | 25/50 | MHz  | 2, 4    |
|  | MMC full-speed/high-speed mode       |                     |      | 20/52 |      |         |
| SDHC_CLK clock low time (full-speed/high-speed mode)     |                                      | $t_{SCKL}$          | 10/7 | —     | ns   | 4       |
| SDHC_CLK clock high time (full-speed/high-speed mode)    |                                      | $t_{SCKH}$          | 10/7 | —     | ns   | 4       |
| SDHC_CLK clock rise and fall times                       |                                      | $t_{SCKR}/t_{SCKF}$ | —    | 3     | ns   | 4       |
| Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK       |                                      | $t_{NIIVKH}$        | 2.5  | —     | ns   | 3, 4, 5 |
| Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK        |                                      | $t_{NIIXKH}$        | 2.5  | —     | ns   | 4, 5    |
| Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid  |                                      | $t_{NIKHGX}$        | —3   | —     | ns   | 4, 5    |
| Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid |                                      | $t_{NIKHGX}$        | —    | 3     | ns   | 4, 5    |

- Notes:
- The symbols used for timing specifications herein follow the pattern of  $t_{(first\ three\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and (first three letters of functional block)(reference)(state)(signal)(state) for outputs. For example,  $t_{FHSKHGX}$  symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
  - In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card.
  - To satisfy setup timing, one-way board-routing delay between Host and Card, on SDHC\_CLK, SDHC\_CMD, and SDHC\_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SDHC\_CLK, SDHC\_CMD, and SDHC\_DATx should not exceed 1.5ns.
  - $C_{CARD} = 10\text{ pF}$ , (1 card), and  $C_L = C_{BUS} + C_{HOST} + C_{CARD} = 40\text{ pF}$ .
  - The parameter values apply to both full-speed and high-speed modes.
  - For recommended operating conditions, see [Table 3-2](#).

This figure provides the eSDHC clock input timing diagram.

**Figure 3-16.** eSDHC clock input timing diagram



This figure provides the data and command input/output timing diagram.



Figure 3-17. eSDHC data and command input/output timing diagram referenced to clock

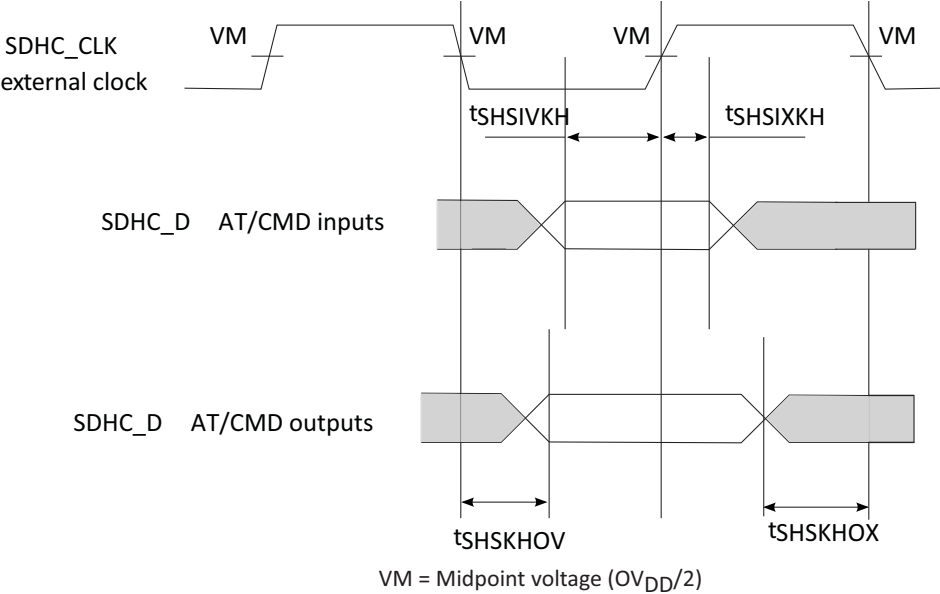
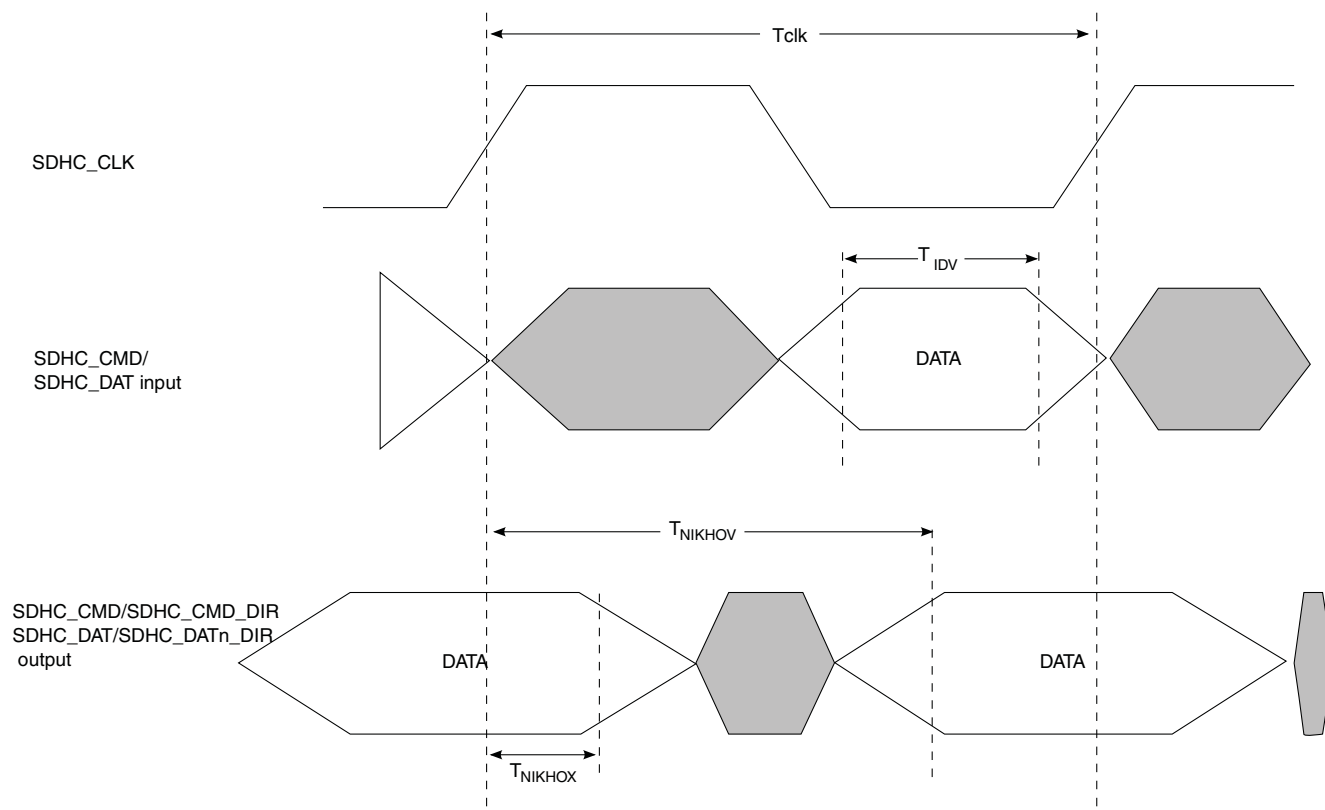


Table 3-47. eSDHC AC timing (eMMC HS200)

| Parameter   |                 | Symbol              | Min   | Max | Unit          | Notes |
|---|-----------------|---------------------|-------|-----|---------------|-------|
| SDHC_CLK clock frequency  | eMMC HS200 mode | $f_{SCK}$           | —     | 175 | MHz           | —     |
| SDHC_CLK duty cycle   |                 | —                   | 47    | 53  | %             | —     |
| SDHC_CLK clock rise and fall times  |                 | $t_{SCKR}/t_{SCKF}$ | —     | 1   | ns            | (1)   |
| Output hold time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR  | eMMC HS200 mode | $t_{NIKHOX}$        | 1.6   | —   | ns            | —     |
| Output delay time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR | eMMC HS200 mode | $t_{NIKHOV}$        | —     | 3.9 | ns            | —     |
| Input data window (UI)  | eMMC HS200 mode | $t_{IDV}$           | 0.475 | —   | Unit interval | —     |

- Notes:
- 1.  $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 10$  pF.
  - 2. For recommended operating conditions, see Table 3.

This figure provides the HS200 mode timing diagram.

**Figure 3-18.** eMMC HS200 mode timing diagram

### 3.15 Multicore programmable interrupt controller (MPIC)

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

#### 3.15.1 MPIC DC specifications

This figure provides the DC electrical characteristics for the MPIC interface.

**Table 3-48.** MPIC DC electrical characteristics ( $OV_{DD} = 1.8\text{ V}$ )<sup>(3)</sup>

| Parameter  | Symbol   | Min  | Max | Unit          | Notes |
|--|----------|------|-----|---------------|-------|
| Input high voltage   | $V_{IH}$ | 1.25 | –   | V             | 1     |
| Input low voltage  | $V_{IL}$ | –    | 0.6 | V             | 1     |
| Input current ( $OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$ )            | $I_{IN}$ | –50  | +50 | $\mu\text{A}$ | 2     |
| Output high voltage ( $OV_{DD} = \text{min}$ , $I_{OH} = -0.5\text{ mA}$ ) | $V_{OH}$ | 1.35 | –   | V             | –     |
| Output low voltage ( $OV_{DD} = \text{min}$ , $I_{OL} = 0.5\text{ mA}$ )   | $V_{OL}$ | –    | 0.4 | V             | –     |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the min and max  $OV_{IN}$  respective values found in [Table 3-2](#).
  2. The symbol  $OV_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in [Table 3-2](#).
  3. For recommended operating conditions, see [Table 3-2](#).

## 3.15.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

**Table 3-49.** MPIC Input AC timing specifications<sup>(2)</sup>

| Characteristic                  | Symbol      | Min | Max | Unit    | Notes |
|---------------------------------|-------------|-----|-----|---------|-------|
| MPIC inputs-minimum pulse width | $t_{PIWID}$ | 3   | —   | SYSCLKs | 1     |

- Notes:
1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least  $t_{PIWID}$  ns to ensure proper operation when working in edge triggered mode.
  2. For recommended operating conditions, see [Table 3-2](#).

## 3.16 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

### 3.16.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

**Table 3-50.** JTAG DC electrical characteristics ( $OV_{DD} = 1.8V$ )<sup>(3)</sup>

| Parameter  | Symbol   | Min  | Max      | Unit | Notes  |
|--|----------|------|----------|------|--------|
| Input high voltage   | $V_{IH}$ | 1.25 | —        | V    | (1)    |
| Input low voltage  | $V_{IL}$ | —    | 0.6      | V    | (1)    |
| Input current ( $OV_{IN} = 0V$ or $OV_{IN} = OV_{DD}$ )      | $I_{IN}$ | —    | −100/+50 | μA   | (2)(4) |
| Output high voltage ( $OV_{DD} = \min$ , $I_{OH} = -0.5$ mA) | $V_{OH}$ | 1.35 | —        | V    | —      |
| Output low voltage ( $OV_{DD} = \min$ , $I_{OL} = 0.5$ mA)   | $V_{OL}$ | —    | 0.4      | V    | —      |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $OV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $V_{IN'}$  in this case, represents the  $OV_{in}$  symbol found in [Table 3-2](#).
  3. For recommended operating conditions, see [Table 3-2](#).
  4. TDI, TMS, and TRST\_B have internal pull-ups per the IEEE Std. 1149.1 specification.

### 3.16.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in [Figure 3-19](#) through [Figure 3-22](#).

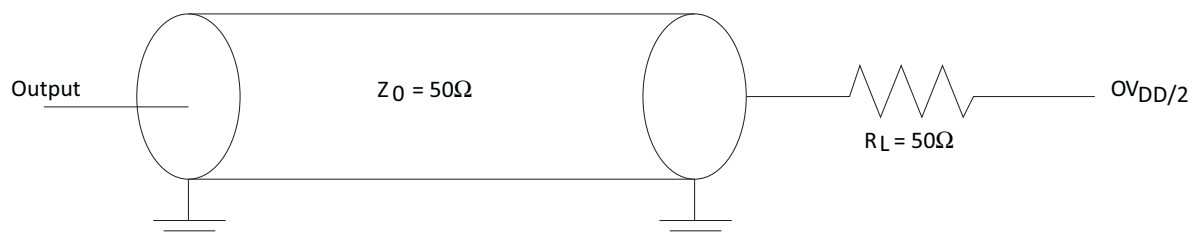
**Table 3-51.** JTAG AC timing specifications<sup>(4)</sup>

| Parameter   | Symbol <sup>(1)</sup> | Min | Max  | Unit | Notes |
|---|-----------------------|-----|------|------|-------|
| JTAG external clock frequency of operation        | $f_{JTG}$             | 0   | 33.3 | MHz  | —     |
| JTAG external clock cycle time                    | $t_{JTG}$             | 30  | —    | ns   | —     |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$          | 15  | —    | ns   | —     |
| JTAG external clock rise and fall times           | $t_{JTGR}/t_{JTGF}$   | 0   | 2    | ns   | —     |
| TRST_B assert time                                | $t_{TRST}$            | 25  | —    | ns   | (2)   |
| Input setup times                                 | $t_{JTDVKH}$          | 4   | —    | ns   | (5)   |
| Input hold times                                  | $t_{JTDXKH}$          | 10  | —    | ns   | —     |
| Output valid times                                | $t_{JTKLDV}$          |     |      | ns   | (3)   |
| Boundary—scan data                                |                       | —   | 15   |      |       |
| TDO   |                       | —   | 10   |      |       |
| Output hold times                                 | $t_{JTKLDX}$          | 0   | —    | ns   | (3)   |

- Notes:
1. The symbols used for timing specifications follow the pattern  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{JTDVKH}$  symbolizes JTAG device timing ( $J_T$ ) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTDXKH}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
  2. TRST\_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
  3. All outputs are measured from the midpoint voltage of the falling edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive  $50\Omega$  load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
  4. For recommended operating conditions, see [Table 3-2](#).
  5. LP\_TMP\_DETECT pin requires 9.5ns input setup time for the board JTAG test to go through runTESTIdle.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

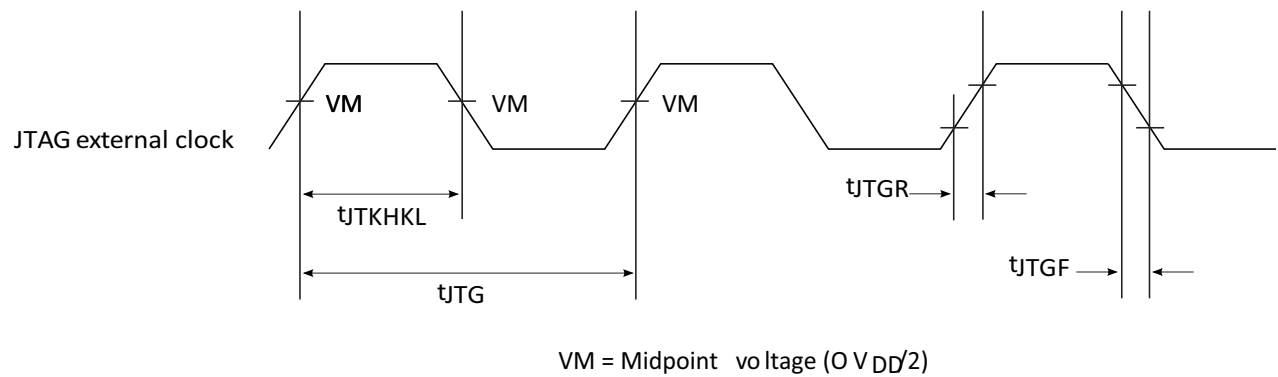
**Figure 3-19.** AC test load for the JTAG interface



VM = Midpoint voltage ( $OV_{DD}/2$ )

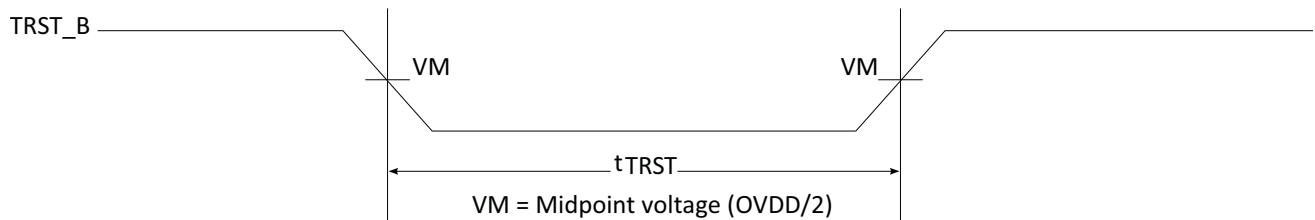
This figure provides the JTAG clock input timing diagram.

**Figure 3-20.** JTAG clock input timing diagram



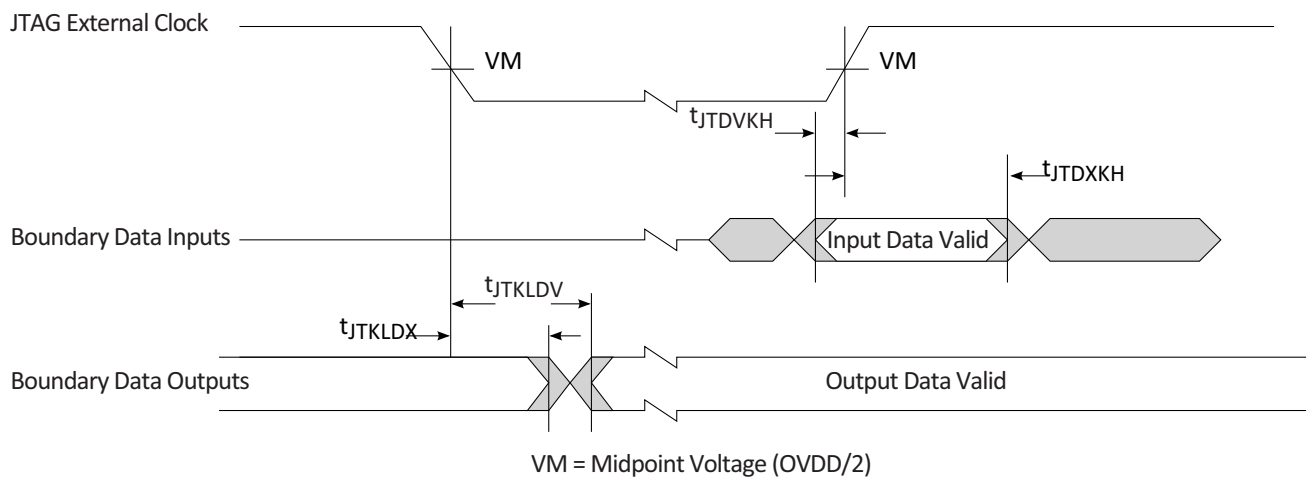
This figure provides the TRST\_B timing diagram.

**Figure 3-21.** TRST\_B timing diagram



This figure provides the boundary-scan timing diagram.

**Figure 3-22.** Boundary-scan timing diagram



## 3.17 I<sup>2</sup>C interface

This section describes the DC and AC electrical characteristics for the I<sup>2</sup>C interface.

### 3.17.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I<sup>2</sup>C interfaces operating at 2.5V.

**Table 3-52.** I2C DC electrical characteristics (DV<sub>DD</sub> = 2.5V)<sup>(5)</sup>

| Parameter   | Symbol              | Min | Max | Unit | Notes |
|---|---------------------|-----|-----|------|-------|
| Input high voltage  | V <sub>IH</sub>     | 1.7 | –   | V    | (1)   |
| Input low voltage   | V <sub>IL</sub>     | –   | 0.7 | V    | (1)   |
| Output low voltage (OV <sub>DD</sub> = min, I <sub>OL</sub> = 3 mA)   | V <sub>OL</sub>     | 0   | 0.4 | V    | (2)   |
| Pulse width of spikes which must be suppressed by the input filter  | t <sub>I2CHKL</sub> | 0   | 50  | ns   | (3)   |
| Input current each I/O pin (input voltage is between 0.1 x OV <sub>DD</sub> and 0.9 x OV <sub>DD</sub> (max)) | I <sub>I</sub>      | –50 | 50  | μA   | (4)   |
| Capacitance for each I/O pin  | C <sub>I</sub>      | –   | 10  | pF   | –     |

- Notes:
1. The min V<sub>IL</sub> and max V<sub>IH</sub> values are based on the respective min and max OV<sub>IN</sub> values found in [Table 3-2](#).
  2. The output voltage (open drain or open collector) condition = 3 mA sink current.
  3. See the chip reference manual for information about the digital filter used.
  4. I/O pins obstruct the SDA and SCL lines if OV<sub>DD</sub> is switched off.
  5. For recommended operating conditions, see [Table 3-2](#).

This table provides the DC electrical characteristics for the I<sup>2</sup>C interfaces operating at 1.8V.

**Table 3-53.** I2C DC electrical characteristics (DV<sub>DD</sub> = 1.8V)<sup>(4)</sup>

| Parameter   | Symbol              | Min  | Max  | Unit | Notes |
|---|---------------------|------|------|------|-------|
| Input high voltage  | V <sub>IH</sub>     | 1.25 | –    | V    | (1)   |
| Input low voltage   | V <sub>IL</sub>     | –    | 0.6  | V    | (1)   |
| Output low voltage (OV <sub>DD</sub> = min, I <sub>OL</sub> = 2 mA)   | V <sub>OL</sub>     | 0    | 0.36 | V    |       |
| Pulse width of spikes which must be suppressed by the input filter  | t <sub>I2CHKL</sub> | 0    | 50   | ns   | (2)   |
| Input current each I/O pin (input voltage is between 0.1 x OV <sub>DD</sub> and 0.9 x OV <sub>DD</sub> (max)) | I <sub>I</sub>      | –50  | 50   | μA   | (3)   |
| Capacitance for each I/O pin  | C <sub>I</sub>      | –    | 10   | pF   | –     |

- Notes:
1. The min V<sub>IL</sub> and max V<sub>IH</sub> values are based on the respective min and max OV<sub>IN</sub> values found in [Table 3-2](#).
  2. See the chip reference manual for information about the digital filter used.
  3. I/O pins obstruct the SDA and SCL lines if OV<sub>DD</sub> is switched off.
  4. For recommended operating conditions, see [Table 3-2](#).

### 3.17.2 I2C AC timing specifications

This table provides the AC timing parameters for the I<sup>2</sup>C interfaces.

**Table 3-54.** I2C AC timing specifications<sup>(5)</sup>

| Parameter                    | Symbol <sup>(1)</sup> | Min | Max | Unit | Notes |
|------------------------------|-----------------------|-----|-----|------|-------|
| SCL clock frequency          | f <sub>I2C</sub>      | 0   | 400 | kHz  | (2)   |
| Low period of the SCL clock  | t <sub>I2CL</sub>     | 1.3 | –   | μs   | –     |
| High period of the SCL clock | t <sub>I2CH</sub>     | 0.6 | –   | μs   | –     |

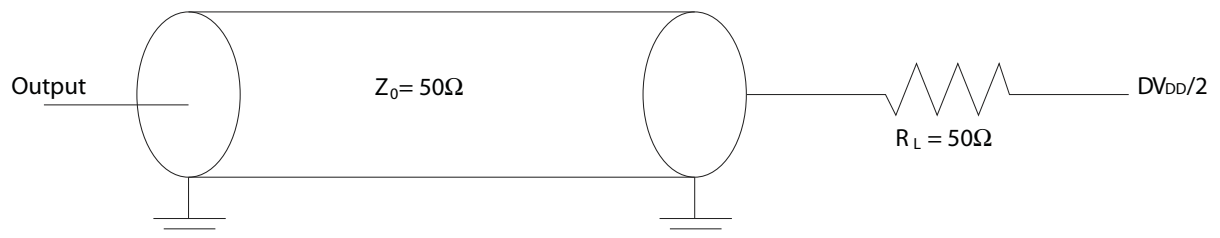
**Table 3-54.** I2C AC timing specifications<sup>(5)</sup>

|  |              |                      |     |         |     |
|--|--------------|----------------------|-----|---------|-----|
| Setup time for a repeated START condition  | $t_{I2SVKH}$ | 0.6                  | —   | $\mu s$ | —   |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6                  | —   | $\mu s$ | —   |
| Data setup time  | $t_{I2DVKH}$ | 100                  | —   | ns      | —   |
| Data input hold time:  | $t_{I2DXKL}$ |                      |     | $\mu s$ | (3) |
| CBUS compatible masters  |              | —                    | —   |         |     |
| I <sup>2</sup> C bus devices   |              | 0                    | —   |         |     |
| Data output delay time   | $t_{I2OVKL}$ | —                    | 0.9 | $\mu s$ | (4) |
| Setup time for STOP condition  | $t_{I2PVKH}$ | 0.6                  | —   | $\mu s$ | —   |
| Bus free time between a STOP and START condition   | $t_{I2KHDx}$ | 1.3                  | —   | $\mu s$ | —   |
| Noise margin at the LOW level for each connected device (including hysteresis)               | $V_{NL}$     | $0.1 \times OV_{DD}$ | —   | V       | —   |
| Noise margin at the HIGH level for each connected device (including hysteresis)              | $V_{NH}$     | $0.2 \times OV_{DD}$ | —   | V       | —   |
| Capacitive load for each bus line  | $C_b$        | —                    | 400 | pF      | —   |

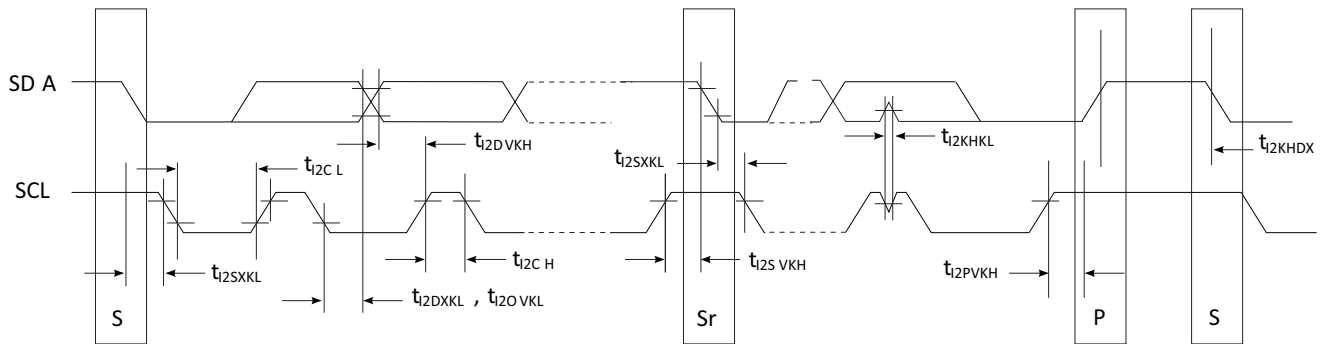
- Notes:
1. The symbols used for timing specifications herein follow the pattern  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{I2DVKH}$  symbolizes I2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time. Also,  $t_{I2SXKL}$  symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the tI2C clock reference (K) going to the low (L) state or hold time. Also,  $t_{I2PVKH}$  symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time.
  2. The requirements for I2C frequency calculation must be followed. See Determining the I2C Frequency Divider Ratio for SCL (AN2919).
  3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see Determining the I2C Frequency Divider Ratio for SCL (AN2919).
  4. The maximum  $t_{I2OVKL}$  has to be met only if the device does not stretch the LOW period ( $t_{I2CL}$ ) of the SCL signal.
  5. For recommended operating conditions, see Table 3-2.

This figure provides the AC test load for the I<sup>2</sup>C.

**Figure 3-23.** I<sup>2</sup>C AC test load



This figure shows the AC timing diagram for the I<sup>2</sup>C bus.

**Figure 3-24.** I<sup>2</sup>C Bus AC timing diagram

### 3.18 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

#### 3.18.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at  $V_{DD} = 2.5$  V.

**Table 3-55.** GPIO DC electrical characteristics (2.5 V)<sup>(3)</sup>

| Parameter  | Symbol   | Min | Max | Unit    | Notes |
|--|----------|-----|-----|---------|-------|
| Input high voltage   | $V_{IH}$ | 1.7 | –   | V       | (1)   |
| Input low voltage  | $V_{IL}$ | –   | 0.7 | V       | (1)   |
| Input current ( $V_{IN} = 0$ V or $V_{IN} = V_{DD}$ )              | $I_{IN}$ | –50 | +50 | $\mu$ A | (2)   |
| Output high voltage<br>( $V_{DD} = \text{min}$ , $I_{OH} = -1$ mA) | $V_{OH}$ | 2.0 | –   | V       | –     |
| Output low voltage<br>( $V_{DD} = \text{min}$ , $I_{OL} = 1$ mA)   | $V_{OL}$ | –   | 0.4 | V       | –     |

- Notes: 1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $V_{IN}$  values found in [Table 3-2](#).  
 2. The symbol  $V_{IN}$ , in this case, represents the  $V_{IN}$  symbol referenced in Recommended operating conditions.  
 3. For recommended operating conditions, see [Table 3-2](#).

This table provides the DC electrical characteristics for GPIO pins operating at  $V_{DD}$  or  $OV_{DD} = 1.8$  V.

**Table 3-56.** GPIO DC electrical characteristics (1.8 V)<sup>(3)</sup>

| Parameter          | Symbol   | Min  | Max | Unit | Notes |
|--------------------|----------|------|-----|------|-------|
| Input high voltage | $V_{IH}$ | 1.25 | –   | V    | (1)   |
| Input low voltage  | $V_{IL}$ | –    | 0.6 | V    | (1)   |



**Table 3-56.** GPIO DC electrical characteristics (1.8 V)<sup>(3)</sup>

|   |          |      |          |               |     |
|---|----------|------|----------|---------------|-----|
| Input current ( $V_{IN} = 0\text{ V}$ or $V_{IN} = L/OV_{DD}$ )                 | $I_{IN}$ | —    | $\pm 50$ | $\mu\text{A}$ | (2) |
| Output high voltage<br>( $L/OV_{DD} = \text{min}$ , $I_{OH} = -0.5\text{ mA}$ ) | $V_{OH}$ | 1.35 | —        | V             | —   |
| Output low voltage<br>( $L/OV_{DD} = \text{min}$ , $I_{OL} = 0.5\text{ mA}$ )   | $V_{OL}$ | —    | 0.4      | V             | —   |

- Notes:
1. The min  $V_{IL}$  and max  $V_{IH}$  values are based on the respective min and max  $L/OV_{IN}$  values found in [Table 3-2](#).
  2. The symbol  $V_{IN}$ , in this case, represents the  $L/OV_{IN}$  symbol referenced in [Recommended operating conditions](#).
  3. For recommended operating conditions, see [Table 3-2](#).

## 3.18.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

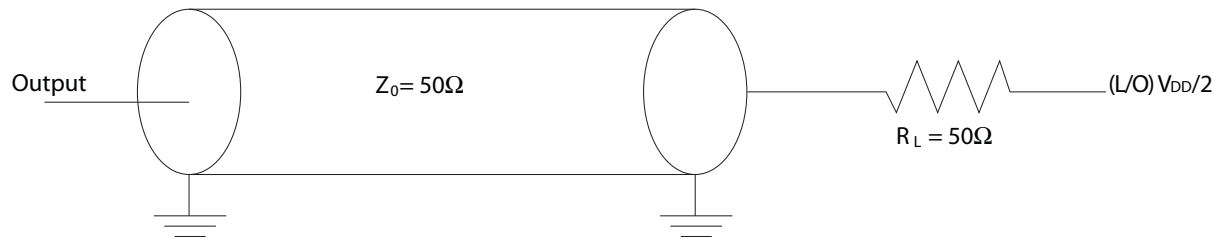
**Table 3-57.** GPIO input AC timing specifications<sup>(2)</sup>

| Parameter                       | Symbol      | Min | Unit | Notes |
|---------------------------------|-------------|-----|------|-------|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20  | ns   | (1)   |

- Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least  $t_{PIWID}$  to ensure proper operation.
  2. For recommended operating conditions, see [Table 3-2](#).

This figure provides the AC test load for the GPIO.

**Figure 3-25.** GPIO AC test load



## 3.19 High-speed serial interfaces (HSSI)

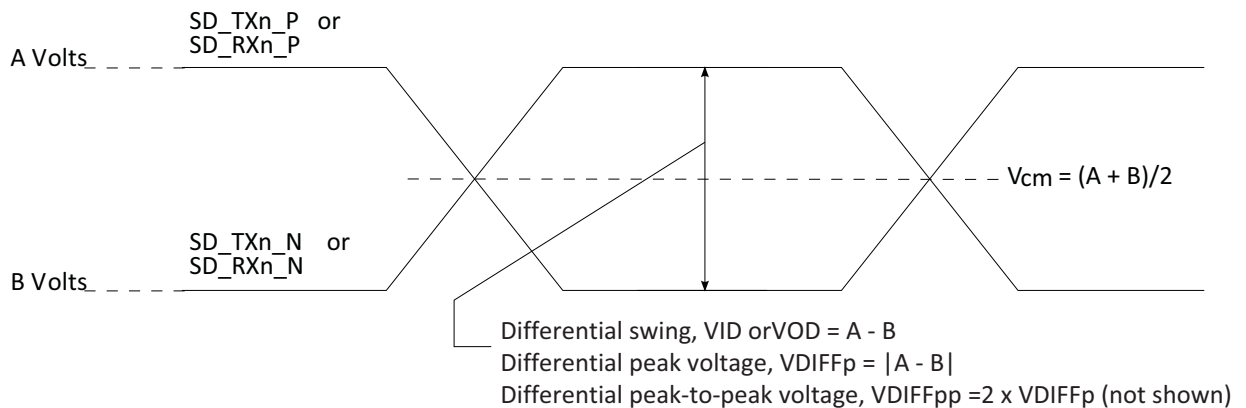
The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SATA, Serial RapidIO, XAUI, XFI, Aurora, HiGig, SGMII and QSGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

### 3.19.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output ( $SD\_TXn\_P$  and  $SD\_TXn\_N$ ) or a receiver input ( $SD\_RXn\_P$  and  $SD\_RXn\_N$ ). Each signal swings between A volts and B volts where  $A > B$ .

**Figure 3-26.** Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

#### Single-Ended Swing

The transmitter output signals and the receiver input signals SD\_TXn\_P, SD\_TXn\_N, SD\_RXn\_P and SD\_RXn\_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

#### Differential Output Voltage, V<sub>OD</sub> (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V<sub>OD</sub>, is defined as the difference of the two complementary output voltages: V<sub>SD\_TXn\_P</sub> - V<sub>SD\_TXn\_N</sub>. The V<sub>OD</sub> value can be either positive or negative.

#### Differential Input Voltage, V<sub>ID</sub> (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V<sub>ID</sub>, is defined as the difference of the two complementary input voltages: V<sub>SD\_RXn\_P</sub> - V<sub>SD\_RXn\_N</sub>. The V<sub>ID</sub> value can be either positive or negative.

#### Differential Peak Voltage, V<sub>DIFFp</sub>

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V<sub>DIFFp</sub> = |A - B| volts.

#### Differential Peak-to-Peak, V<sub>DIFFp-p</sub>

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, V<sub>DIFFp-p</sub> = 2 × V<sub>DIFFp</sub> = 2 × |A - B| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as V<sub>TX-DIFFp-p</sub> = 2 × |V<sub>OD</sub>|.

#### Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD\_TXn\_N, for example) from the non-inverting signal (SD\_TXn\_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See [Figure 3-31](#) as an example for differential waveform.

## Common Mode Voltage, $V_{cm}$

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output,  $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \sim 2 = (A + B) \sim 2$ , which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD\_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD\_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing ( $V_{OD}$ ) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words,  $V_{OD}$  is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ( $V_{DIFFp}$ ) is 500 mV. The peak-to-peak differential voltage ( $V_{DIFFp-p}$ ) is 1000 mV p-p.

### 3.19.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1\_REF\_CLK[1:2]\_P and SD1\_REF\_CLK[1:2]\_N for SerDes 1, SD2\_REF\_CLK[1:2]\_P and SD2\_REF\_CLK[1:2]\_N for SerDes 2.

SerDes 1-2 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS\_PRTCLn:

- SerDes 1: SGMII (1.25 and 3.125 GBaud), PEX3 (2.5, 5 and 8 GT/s), PEX4 (2.5 and 5 GT/s), HiGig/HiGig2 (3.125GBaud), HiGig/HiGig2 (3.75GBaud) or XAUI (3.125GBaud)XFI (10.3125 GBaud only), 1000Base-KX (3.125GBaud), 10GBase-KR (10.3125 GBaud only)
- SerDes 2: PEX1 (2.5, 5 and 8 GT/s), PEX2 (2.5 and 5 GT/s), Aurora (2.5 and 5 GBaud), SATA1/2 (1.5 and 3.0 Gbps) and SRIO1/2 (2.5, 3.125 and 5 GBaud)

The following sections describe the SerDes reference clock requirements and provide application information.

#### 3.19.2.1 SerDes spread-spectrum clock source recommendations

SDn\_REF\_CLKn\_P/SDn\_REF\_CLKn\_N are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in [Table 3-58](#). When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

For SATA protocol, the SerDes transmitter does not support spread-spectrum clocking. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread-spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as

SATA/SGMII/QSGMII/SRIO/ XAUI due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

**Table 3-58.** SerDes spread-spectrum clock source recommendations<sup>(1)</sup>

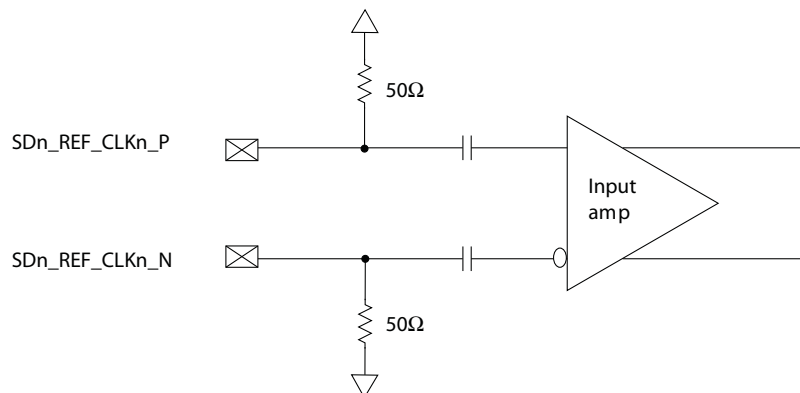
| Parameter            | Min | Max  | Unit | Notes |
|----------------------|-----|------|------|-------|
| Frequency modulation | 30  | 33   | kHz  | –     |
| Frequency spread     | +0  | –0.5 | %    | (2)   |

Notes: 1. At recommended operating conditions. See [Table 3-2](#).  
2. Only down-spreading is allowed.

### 3.19.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

**Figure 3-27.** Receiver of SerDes reference clocks



The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements ( $SV_{DDn}$ ) are as specified in [Recommended operating conditions](#).
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The  $SDn\_REF\_CLKn\_P$  and  $SDn\_REF\_CLKn\_N$  are internally AC-coupled differential inputs as shown in [Figure 3-27](#). Each differential clock input ( $SDn\_REF\_CLKn\_P$  or  $SDn\_REF\_CLKn\_N$ ) has on-chip  $50\Omega$  termination to  $SGNDn$  followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

- The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ( $0.4\text{ V} \sim 50 = 8\text{ mA}$ ) while the minimum common mode input level is 0.1 V above SGND<sub>n</sub>. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD<sub>n</sub>\_REF\_CLK<sub>n</sub>\_P and SD<sub>n</sub>\_REF\_CLK<sub>n</sub>\_N inputs cannot drive 50Ω to SGND<sub>n</sub> DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

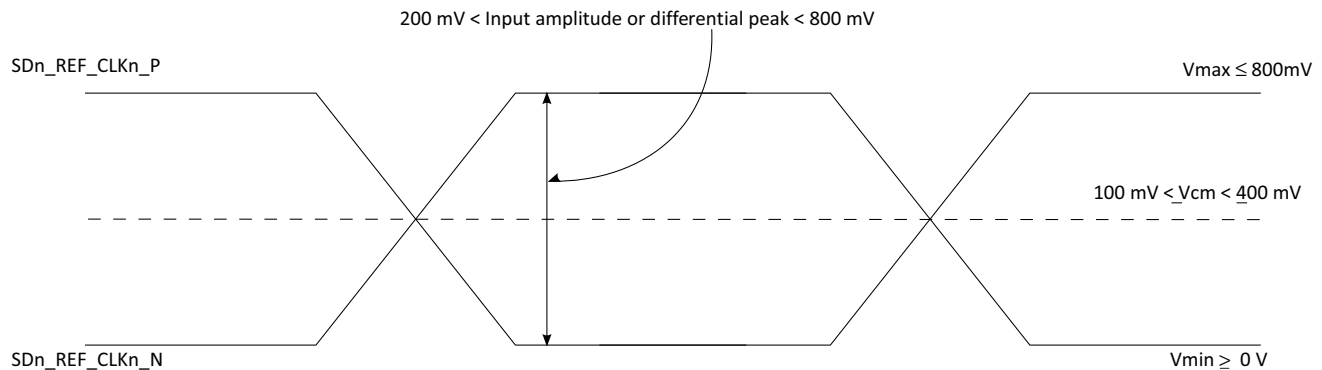
## 3.19.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in [SerDes reference clock receiver characteristics](#), the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. [Figure 3-28](#) shows the SerDes reference clock input requirement for DC-coupled connection scheme.

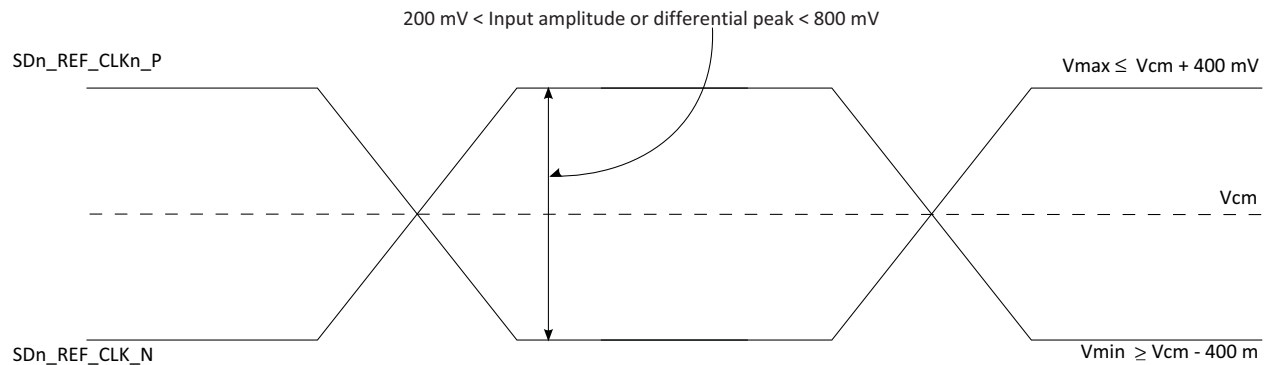
**Figure 3-28.** Differential reference clock input DC requirements (external DC-coupled)



- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this

connection scheme has its common mode voltage set to SGNDn. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGNDn). Figure 3-29 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

**Figure 3-29.** Differential reference clock input DC requirements (external AC-coupled)

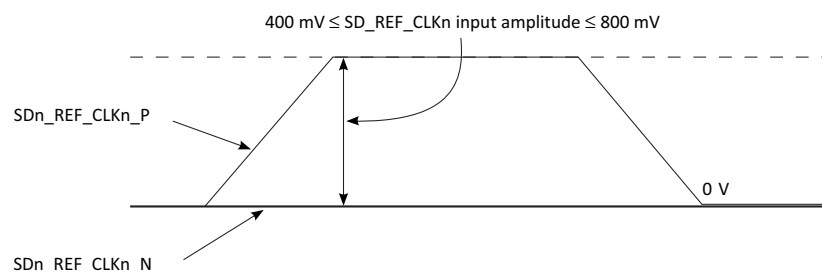


Single-ended mode:

The reference clock can also be single-ended. The SDn\_REF\_CLKn\_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from  $V_{MIN}$  to  $V_{MAX}$ ) with SDn\_REF\_CLKn\_N either left unconnected or tied to ground.

- The SDn\_REF\_CLKn\_P input average voltage must be between 200 and 400 mV. Figure 3-30 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SDn\_REF\_CLKn\_N) through the same source impedance as the clock input (SDn\_REF\_CLKn\_P) in use.

**Figure 3-30.** Single-ended reference clock input DC requirements



### 3.19.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 8 GBaud.

This includes PCI Express (2.5, 5 and 8 GT/s), SGMII (1.25GBaud), 2.5x SGMII (3.125 GBaud), Serial RapidIO (2.5, 3.125 and 5 GBaud), Aurora (2.5 and 5 GBaud), HiGig/

HiGig2 (3.125 GBaud), HiGig/HiGig2 (3.75 GBaud), XAUI (3.125 GBaud), SATA (1.5 and 3 Gbps), 1000Base-KX (3.125 GBaud) and SerDes reference clocks to be guaranteed by the customer's application design.

**Table 3-59.** SDn\_REF\_CLKn\_P/SDn\_REF\_CLKn\_N input clock requirements (SV<sub>DDn</sub> = 1.0 V)<sup>(1)</sup>

| Parameter  | Symbol                | Min  | Typ            | Max  | Unit   | Notes    |
|--|-----------------------|------|----------------|------|--------|----------|
| SDn_REF_CLKn_P/SDn_REF_CLKn_N frequency range  | $t_{CLK\_REF}$        | —    | 100/125/156.25 | —    | MHz    | (2)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N clock frequency tolerance  | $t_{CLK\_TOL}$        | –300 | —              | 300  | ppm    | (3)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N clock frequency tolerance  | $t_{CLK\_TOL}$        | –100 | —              | 100  | ppm    | (4)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N reference clock duty cycle   | $t_{CLK\_DUTY}$       | 40   | 50             | 60   | %      | (5)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N max deterministic peak-to-peak jitter at 10 <sup>–6</sup> BER                              | $t_{CLK\_DJ}$         | —    | —              | 42   | ps     | —        |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N total reference clock jitter at 10 <sup>–6</sup> BER (peak-to-peak jitter at refClk input) | $t_{CLK\_TJ}$         | —    | —              | 86   | ps     | (6)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter   | $t_{REFCLK-LF-RMS}$   | —    | —              | 3    | ps RMS | (7)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter  | $t_{REFCLK-HF-RMS}$   | —    | —              | 3.1  | ps RMS | (7)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N RMS reference clock jitter   | $t_{REFCLK-RMS-DC}$   | —    | —              | 1    | ps RMS | (8)      |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N rising/falling edge rate   | $t_{CLKRR}/t_{CLKFR}$ | 1    | —              | 4    | V/ns   | (9)      |
| Differential input high voltage  | $V_{IH}$              | 200  | —              | —    | mV     | (5)      |
| Differential input low voltage   | $V_{IL}$              | —    | —              | –200 | mV     | (5)      |
| Rising edge rate (SDn_REF_CLKn_P) to falling edge rate (SDn_REF_CLKn_P) matching   | Rise-Fall Matching    | —    | —              | 20   | %      | (10)(11) |

- Notes:
- For recommended operating conditions, see [Table 3-2](#).
  - Caution:** Only 100, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
  - For PCI Express (2.5, 5, 8 GT/s)
  - For SGMII, 2.5x SGMII, QSGMII, sRIO, HiGig/HiGig2, XAUI
  - Measurement taken from differential waveform
  - Limits from PCI Express CEM Rev 2.0
  - For PCI Express-5 GT/s, per PCI Express base specification rev 3.0
  - For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0
  - Measured from –200 mV to +200 mV on the differential waveform (derived from SDn\_REF\_CLKn\_P minus SDn\_REF\_CLKn\_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See [Figure 3-31](#).
  - Measurement taken from single-ended waveform
  - Matching applies to rising edge for SDn\_REF\_CLKn\_P and falling edge rate for SDn\_REF\_CLKn\_N. It is measured using a 200 mV window centered on the median cross point where SDn\_REF\_CLKn\_P rising meets SDn\_REF\_CLKn\_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SDn\_REF\_CLKn\_P must be compared to the fall edge rate of SDn\_REF\_CLKn\_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 3-32](#).

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud) and 10GBase-KR (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

**Table 3-60.** SDn\_REF\_CLKn\_P/SDn\_REF\_CLKn\_N input clock requirements ( $SV_{DDn} = 1.0\text{ V}$ )<sup>(1)</sup>

| Parameter  | Symbol          | Min  | Typ    | Max  | Unit   | Notes |
|--|-----------------|------|--------|------|--------|-------|
| SDn_REF_CLKn_P/SDn_REF_CLKn_N frequency range  | $t_{CLK\_REF}$  | -    | 156.25 | —    | MHz    | (2)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N clock frequency tolerance  | $t_{CLK\_TOL}$  | -100 | —      | 100  | ppm    | -     |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N reference clock duty cycle   | $t_{CLK\_DUTY}$ | 40   | 50     | 60   | %      | (3)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N single side band noise   | @1 kHz          | —    | —      | -85  | dBc/Hz | (4)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N single side band noise   | @10 kHz         | —    | —      | -108 | dBc/Hz | (4)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N single side band noise   | @100 kHz        | —    | —      | -128 | dBc/Hz | (4)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N single side band noise   | @1 MHz          | —    | —      | -138 | dBc/Hz | (4)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N single side band noise   | @10 MHz         | —    | —      | -138 | dBc/Hz | (4)   |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)                                  | $t_{CLK\_RJ}$   | —    | —      | 0.8  | ps     | —     |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N total reference clock jitter at $10^{-12}$ BER (1.2 MHz to 15 MHz) | $t_{CLK\_TJ}$   | —    | —      | 11   | ps     | —     |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)                                 | —               | —    | —      | -75  | dBc    | —     |

Notes: 1. For recommended operating conditions, see [Table 3-2](#).

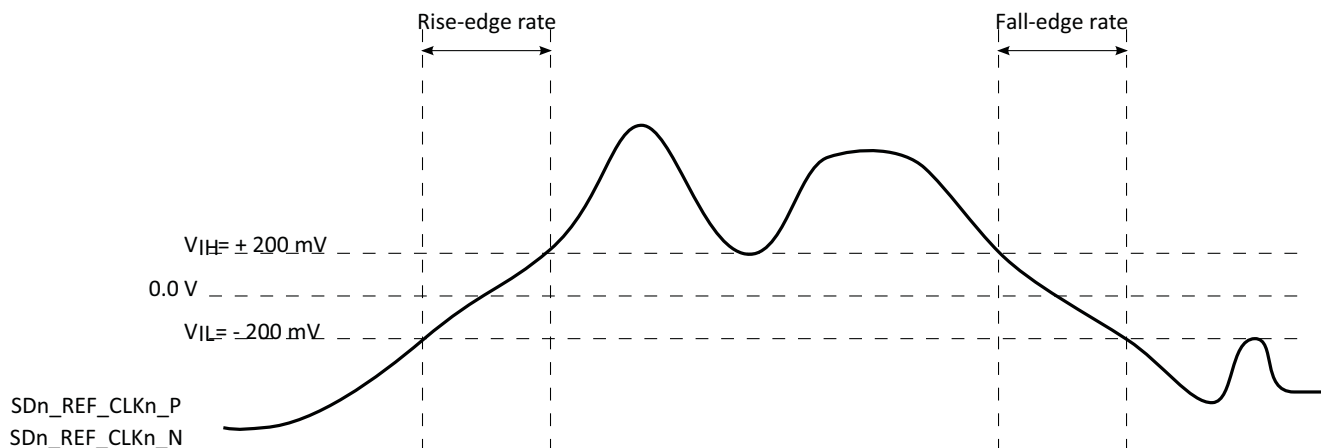
2. **Caution:** Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.

3. Measurement taken from differential waveform.

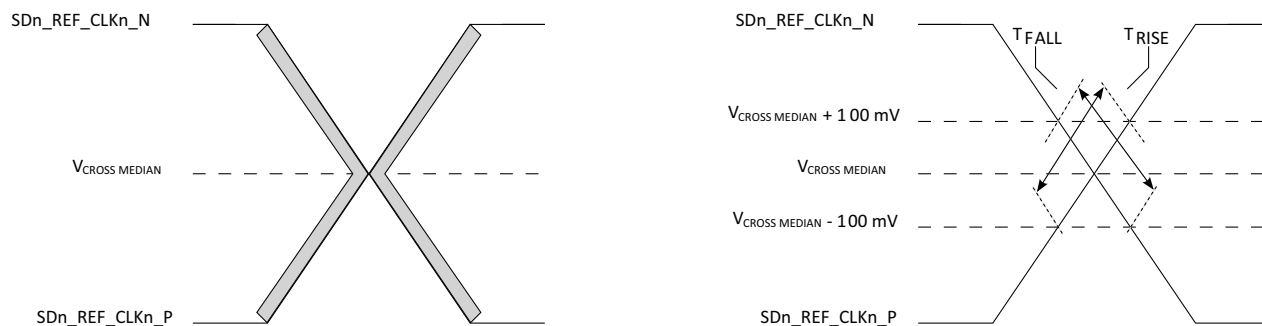
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.



**Figure 3-31.** Differential measurement points for rise and fall time



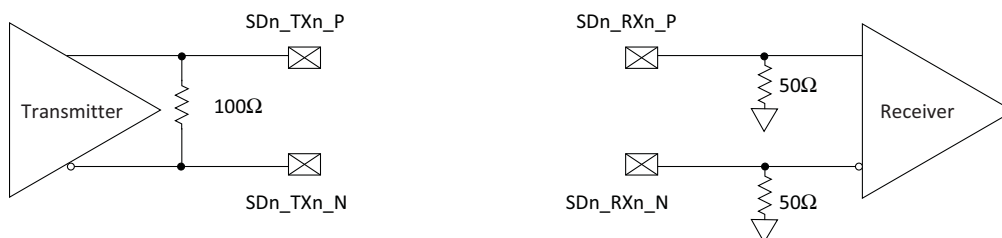
**Figure 3-32.** Single-ended measurement points for rise and fall time matching



### 3.19.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

**Figure 3-33.** SerDes transmitter and receiver reference circuits



The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial RapidIO (sRIO)
- XAUI interface
- Aurora interface
- Serial ATA (SATA) interface
- SGMII interface

- HiGig/HiGig2 interface
- XFI interface
- 10GBase-KR interface
- 1000Base-KX interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

### 3.19.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

#### 3.19.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a  $\pm 300$  ppm tolerance.

#### 3.19.4.2 PCI Express clocking requirements for $SDn\_REF\_CLKn\_P$ and $SDn\_REF\_CLKn\_N$

SerDes 1-2 ( $SD[1:2]\_REF\_CLK[1:2]_P$  and  $SD[1:2]\_REF\_CLK[1:2]_N$ ) may be used for various SerDes PCI Express configurations based on the RCW Configuration field  $SRDS\_PRTCL$ . PCI Express is not supported on SerDes 1 and 2.

#### NOTE

PCI Express operating in x8 mode is only supported at 2.5 and 5.0 GT/s.

For more information on these specifications, see [SerDes reference clocks](#).

#### 3.19.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

##### 3.19.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 3-61.** PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ( $XV_{DD} = 1.35\text{ V}$ )<sup>(1)</sup>

| Parameter                                | Symbol           | Min | Typical | Max  | Units | Notes   |
|--|------------------|-----|---------|------|-------|---|
| Differential peak-to-peak output voltage | $V_{TX-DIFFp-p}$ | 800 | 1000    | 1200 | mV    | $V_{TX-DIFFp-p} = 2 \times  V_{TX-D+} - V_{TX-D-} $ |

**Table 3-61.** PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ( $XV_{DD} = 1.35\text{ V}$ )<sup>(1)</sup>

|   |                   |     |     |     |          |  |
|---|-------------------|-----|-----|-----|----------|--|
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO}$ | 3.0 | 3.5 | 4.0 | dB       | Ratio of the $V_{TX-DIFFP-P}$ of the second and following bits after a transition divided by the $V_{TX-DIFFP-P}$ of the first bit after a transition. |
| DC differential transmitter impedance             | $Z_{TX-DIFF-DC}$  | 80  | 100 | 120 | $\Omega$ | Transmitter DC differential mode low Impedance   |
| Transmitter DC impedance                          | $Z_{TX-DC}$       | 40  | 50  | 60  | $\Omega$ | Required transmitter D+ as well as D- DC Impedance during all states   |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 3-62.** PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ( $XV_{DD} = 1.35\text{ V}$ )<sup>1</sup>

| Parameter  | Symbol                  | Min | Typical | Max  | Units    | Notes  |
|--|-------------------------|-----|---------|------|----------|--|
| Differential peak-to-peak output voltage           | $V_{TX-DIFFP-P}$        | 800 | 1000    | 1200 | mV       | $V_{TX-DIFFP-P} = 2 \times  V_{TX-D+} - V_{TX-D-} $  |
| Low power differential peak-to-peak output voltage | $V_{TX-DIFFP-P\_LOW}$   | 400 | 500     | 1200 | mV       | $V_{TX-DIFFP-P} = 2 \times  V_{TX-D+} - V_{TX-D-} $  |
| De-emphasized differential output voltage (ratio)  | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5     | 4.0  | dB       | Ratio of the $V_{TX-DIFFP-P}$ of the second and following bits after a transition divided by the $V_{TX-DIFFP-P}$ of the first bit after a transition. |
| De-emphasized differential output voltage (ratio)  | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0     | 6.5  | dB       | Ratio of the $V_{TX-DIFFP-P}$ of the second and following bits after a transition divided by the $V_{TX-DIFFP-P}$ of the first bit after a transition. |
| DC differential transmitter impedance              | $Z_{TX-DIFF-DC}$        | 80  | 100     | 120  | $\Omega$ | Transmitter DC differential mode low impedance   |
| Transmitter DC Impedance                           | $Z_{TX-DC}$             | 40  | 50      | 60   | $\Omega$ | Required transmitter D+ as well as D- DC impedance during all states   |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This table defines the PCI Express 3.0 (8 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 3-63.** PCI Express 3.0 (8 GT/s) differential transmitter output DC specifications ( $XV_{DD} = 1.35\text{ V}$ )<sup>(3)</sup>

| Parameter   | Symbol                  | Min | Typical | Max  | Units | Notes                     |
|---|-------------------------|-----|---------|------|-------|---------------------------|
| Full swing transmitter voltage with no TX Eq      | $V_{TX-FS-NO-EQ}$       | 800 | —       | 1300 | mVp-p | See Note <sup>(1)</sup> . |
| Reduced swing transmitter voltage with no TX Eq   | $V_{TX-RS-NO-EQ}$       | 400 | —       | 1300 | mV    | See Note <sup>(1)</sup> . |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5     | 4.0  | dB    | —                         |

**Table 3-63.** PCI Express 3.0 (8 GT/s) differential transmitter output DC specifications (XVDD = 1.35 V)<sup>(3)</sup>

|   |                         |     |     |     |          |  |
|---|-------------------------|-----|-----|-----|----------|--|
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0 | 6.5 | dB       | –  |
| Minimum swing during EIEOS for full swing         | $V_{TX-EIEOS-FS}$       | 250 | –   | –   | mVp-p    | See Note <sup>(2)</sup>  |
| Minimum swing during EIEOS for reduced swing      | $V_{TX-EIEOS-RS}$       | 232 | –   | –   | mVp-p    | See Note <sup>(2)</sup>  |
| DC differential transmitter impedance             | $Z_{TX-DIFF-DC}$        | 80  | 100 | 120 | $\Omega$ | Transmitter DC differential mode low impedance                       |
| Transmitter DC Impedance                          | $Z_{TX-DC}$             | 40  | 50  | 60  | $\Omega$ | Required transmitter D+ as well as D- DC impedance during all states |

- Notes:
1. Voltage measurements for  $V_{TX-FS-NO-EQ}$  and  $V_{TX-RS-NO-EQ}$  are made using the 64-zeroes/64-ones pattern in the compliance pattern.
  2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the  $V_{TX-FS-NO-EQ}$  measurement which represents the maximum peak voltage the transmitter can drive. The  $V_{TX-EIEOS-FS}$  and  $V_{TX-EIEOS-RS}$  voltage limits are imposed to guarantee the EIEOS threshold of 175 mV<sub>p-p</sub> at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.
  3. For recommended operating conditions, see Table 3-2.

#### 3.19.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 3-64.** PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SVDD = 1.0 V)<sup>(4)</sup>

| Parameter                               | Symbol                    | Min | Typical | Max  | Units      | Notes   |
|---|---------------------------|-----|---------|------|------------|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$          | 120 | 1000    | 1200 | mV         | $V_{RX-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} $ See Note <sup>(1)</sup> .   |
| DC differential input impedance         | $Z_{RX-DIFF-DC}$          | 80  | 100     | 120  | $\Omega$   | Receiver DC differential mode impedance. See Note <sup>(2)</sup>  |
| DC input impedance                      | $Z_{RX-DC}$               | 40  | 50      | 60   | $\Omega$   | Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes <sup>(1)</sup> and <sup>(2)</sup> .         |
| Powered down DC input impedance         | $Z_{RX-HIGH-IMP-DC}$      | 50  | -       | -    | k $\Omega$ | Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note <sup>(3)</sup> . |
| Electrical idle detect threshold        | $V_{RX-IDLE-DET-DIFFp-p}$ | 65  | -       | 175  | mV         | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} $<br>Measured at the package pins of the receiver                |

- Notes:
1. Measured at the package pins with a test load of 50 $\Omega$  to GND on each pin.
  2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
  3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
  4. For recommended operating conditions, see Table 3-2.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 3-65.** PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SVDD = 1.0 V)<sup>(4)</sup>

| Parameter                               | Symbol                    | Min | Typical | Max  | Units      | Notes   |
|---|---------------------------|-----|---------|------|------------|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFP-P}$          | 120 | 1000    | 1200 | mV         | $V_{RX-DIFFP-P} = 2 \times  V_{RX-D+} - V_{RX-D-} $<br>See Note <sup>(1)</sup> .  |
| DC differential input impedance         | $Z_{RX-DIFF-DC}$          | 80  | 100     | 120  | $\Omega$   | Receiver DC differential mode impedance. See Note <sup>(2)</sup>  |
| DC input impedance                      | $Z_{RX-DC}$               | 40  | 50      | 60   | $\Omega$   | Required receiver D+ as well as D- DC Impedance ( $50 \pm 20\%$ tolerance). See Notes <sup>(1)</sup> and <sup>(2)</sup> .   |
| Powered down DC input impedance         | $Z_{RX-HIGH-IMP-DC}$      | 50  | —       | —    | k $\Omega$ | Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note <sup>(3)</sup> . |
| Electrical idle detect threshold        | $V_{RX-IDLE-DET-DIFFP-P}$ | 65  | —       | 175  | mV         | $V_{RX-IDLE-DET-DIFFP-P} = 2 \times  V_{RX-D+} - V_{RX-D-} $<br>Measured at the package pins of the receiver                |

- Notes:
1. Measured at the package pins with a test load of 50 $\Omega$  to GND on each pin.
  2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
  3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
  4. For recommended operating conditions, see Table 3-2.

This table defines the DC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 3-66.** PCI Express 3.0 (8 GT/s) differential receiver input DC specifications (SVDD = 1.0 V)<sup>(6)</sup>

| Parameter                        | Symbol                    | Min | Typ | Max | Units      | Notes   |
|----------------------------------|---------------------------|-----|-----|-----|------------|---|
| DC differential input impedance  | $Z_{RX-DIFF-DC}$          | 80  | 100 | 120 | $\Omega$   | Receiver DC differential mode impedance. See Note <sup>(2)</sup>  |
| DC input impedance               | $Z_{RX-DC}$               | 40  | 50  | 60  | $\Omega$   | Required receiver D+ as well as D- DC Impedance ( $50 \pm 20\%$ tolerance). See Notes <sup>(1)</sup> and <sup>(2)</sup> .   |
| Powered down DC input impedance  | $Z_{RX-HIGH-IMP-DC}$      | 50  | —   | —   | k $\Omega$ | Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note <sup>(3)</sup> . |
| Generator launch voltage         | $V_{RX-LAUNCH-8G}$        | —   | 800 | —   | mV         | Measured at TP1 per PCI Express base spec. rev 3.0  |
| Eye height (–20dB Channel)       | $V_{RX-SV-8G}$            | 25  | —   | —   | mV         | Measured at TP2P per PCI Express base spec. rev 3.0. See Notes <sup>(4)</sup> <sup>(5)</sup>                                |
| Eye height (–12dB Channel)       | $V_{RX-SV-8G}$            | 50  | —   | —   | mV         | Measured at TP2P per PCI Express base spec. rev 3.0. See Notes <sup>(4)</sup> <sup>(5)</sup>                                |
| Eye height (–3dB Channel)        | $V_{RX-SV-8G}$            | 200 | —   | —   | mV         | Measured at TP2P per PCI Express base spec. rev 3.0. See Notes <sup>(4)</sup> <sup>(5)</sup>                                |
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFP-P}$ | 65  | —   | 175 | mV         | $V_{RX-IDLE-DET-DIFFP-P} = 2 \times  V_{RX-D+} - V_{RX-D-} $<br>Measured at the package pins of the receiver                |

- Notes:
1. Measured at the package pins with a test load of 50 $\Omega$  to GND on each pin.
  2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4.  $V_{RX-SV-8G}$  is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.
5.  $V_{RX-SV-8G}$  is referenced to TP2P and is obtained after post processing data captured at TP2.
6. For recommended operating conditions, see [Table 3-2](#).

### 3.19.4.5 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

#### 3.19.4.5.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-67.** PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications<sup>(4)</sup>

| Parameter  | Symbol                            | Min    | Typ | Max    | Units | Notes   |
|--|-----------------------------------|--------|-----|--------|-------|---|
| Unit interval  | UI                                | 399.88 | 400 | 400.12 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations.   |
| Minimum transmitter eye width  | $T_{TX-EYE}$                      | 0.75   | —   | —      | UI    | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at $10^{-12}$ . See Notes <sup>(1)</sup> and <sup>(2)</sup> .   |
| Maximum time between the jitter median and maximum deviation from the median | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ |        |     | 0.125  | UI    | Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes <sup>(1)</sup> and <sup>(2)</sup> . |
| AC coupling capacitor  | CTX                               | 75     |     | 200    | nF    | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note <sup>(3)</sup> .   |

- Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in [Figure 3-35](#) and measured over any 250 consecutive transmitter UIs.
  2. A  $T_{TX-EYE} = 0.75$  UI provides for a total sum of deterministic and random jitter budget of  $T_{TX-JITTER-MAX} = 0.25$  UI for the transmitter collected over any 250 consecutive transmitter UIs. The  $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$  median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have  $C_{TX}$  built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see [Table 3-2](#).

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-68.** PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications<sup>(3)</sup>

| Parameter                                      | Symbol            | Min    | Typ    | Max    | Units | Notes   |
|--|-------------------|--------|--------|--------|-------|---|
| Unit Interval                                  | UI                | 199.94 | 200.00 | 200.06 | ps    | Each UI is 200 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations.   |
| Minimum transmitter eye width                  | $T_{TX-EYE}$      | 0.75   | —      | —      | UI    | The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Note <sup>(1)</sup> .                                     |
| Transmitter RMS deterministic jitter > 1.5 MHz | $T_{TX-HF-DJ-DD}$ | —      | —      | 0.15   | ps    | —   |
| Transmitter RMS deterministic jitter < 1.5 MHz | $T_{TX-LF-RMS}$   | —      | 3.0    | —      | ps    | Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps  |
| AC coupling capacitor                          | $C_{TX}$          | 75     | —      | 200    | nF    | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note <sup>(2)</sup> . |

- Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in [Figure 3-35](#) and measured over any 250 consecutive transmitter UIs.
  2. The chip's SerDes transmitter does not have  $C_{TX}$  built-in. An external AC coupling capacitor is required.
  3. For recommended operating conditions, see [Table 3-2](#).

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-69.** PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications<sup>(4)</sup>

| Parameter                                     | Symbol          | Min      | Typ    | Max      | Units  | Notes   |
|---|-----------------|----------|--------|----------|--------|---|
| Unit Interval                                 | UI              | 124.9625 | 125.00 | 125.0375 | ps     | Each UI is 125 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations. |
| Transmitter uncorrelated total jitter         | $T_{TX-UTJ}$    | —        | —      | 31.25    | ps p-p | —   |
| Transmitter uncorrelated deterministic jitter | $T_{TX-UDJ-DD}$ | —        | —      | 12       | ps p-p | —   |
| Total uncorrelated pulse width jitter (PWJ)   | $T_{TX-UPW-TJ}$ | —        | —      | 24       | ps p-p | See Note <sup>(1)</sup> <sup>(2)</sup>  |

**Table 3-69.** PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications<sup>(4)</sup>

|  |                   |     |   |     |        |   |
|--|-------------------|-----|---|-----|--------|---|
| Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ) | $T_{TX-UPW-DJDD}$ | —   | — | 10  | ps p-p | See Note <sup>(1)</sup> <sup>(2)</sup>  |
| Data dependent jitter  | $T_{TX-DDJ}$      | —   | — | 18  | ps p-p | See Note <sup>(2)</sup>   |
| AC coupling capacitor  | $C_{TX}$          | 176 | — | 265 | nF     | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note <sup>(3)</sup> . |

- Notes:
1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
  2. Measured with optimized preset value after de-embedding to transmitter pin.
  3. The chip's SerDes transmitter does not have  $C_{TX}$  built-in. An external AC coupling capacitor is required.
  4. For recommended operating conditions, see [Table 3-2](#).

### 3.19.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-70.** PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications<sup>(4)</sup>

| Parameter   | Symbol                            | Min    | Typ    | Max    | Units | Notes   |
|---|-----------------------------------|--------|--------|--------|-------|---|
| Unit Interval   | UI                                | 399.88 | 400.00 | 400.12 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations.   |
| Minimum receiver eye width  | $T_{RX-EYE}$                      | 0.4    | —      | —      | UI    | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes <sup>(1)</sup> and <sup>(2)</sup> .  |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | —      | v      | 0.3    | UI    | Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFF-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes <sup>(1)</sup> <sup>(2)</sup> and <sup>(3)</sup> . |

- Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 3-35](#) must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
  2. A  $T_{RX-EYE} = 0.40$  UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The  $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
  3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
  4. For recommended operating conditions, see [Table 3-2](#).



This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-71.** PCI Express 2.0 (5 GT/s) differential receiver input AC specifications<sup>(1)</sup>

| Parameter  | Symbol            | Min    | Typ    | Max    | Units | Notes   |
|--|-------------------|--------|--------|--------|-------|---|
| Unit Interval                                    | UI                | 199.94 | 200.00 | 200.06 | ps    | Each UI is 200 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations. |
| Max receiver inherent timing error               | $T_{RX-TJ-CC}$    | –      | –      | 0.4    | UI    | The maximum inherent total timing error for common RefClk receiver architecture                     |
| Max receiver inherent deterministic timing error | $T_{RX-DJ-DD-CC}$ | –      | –      | 0.30   | UI    | The maximum inherent deterministic timing error for common RefClk receiver architecture             |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 3-72.** PCI Express 3.0 (8 GT/s) differential receiver input AC specifications<sup>(5)</sup>

| Parameter                      | Symbol              | Min      | Typ    | Max      | Units  | Notes   |
|--------------------------------|---------------------|----------|--------|----------|--------|---|
| Unit Interval                  | UI                  | 124.9625 | 125.00 | 125.0375 | ps     | Each UI is 125 ps $\pm$ 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note <sup>(1)</sup> . |
| Eye Width at TP2P              | $T_{RX-SV-8G}$      | 0.3      | –      | 0.35     | UI     | See Note <sup>(1)</sup>   |
| Differential mode interference | $V_{RX-SV-DIFF-8G}$ | 14       | –      | –        | mV     | Frequency = 2.1GHz. See Note <sup>(2)</sup> .   |
| Sinusoidal Jitter at 100 MHz   | $T_{RX-SV-SJ-8G}$   | –        | –      | 0.1      | UI p-p | Fixed at 100 MHz. See Note <sup>(3)</sup> .   |
| Random Jitter                  | $T_{RX-SV-RJ-8G}$   | –        | –      | 2.0      | ps RMS | Random jitter spectrally flat before filtering. See Note <sup>(4)</sup> .   |

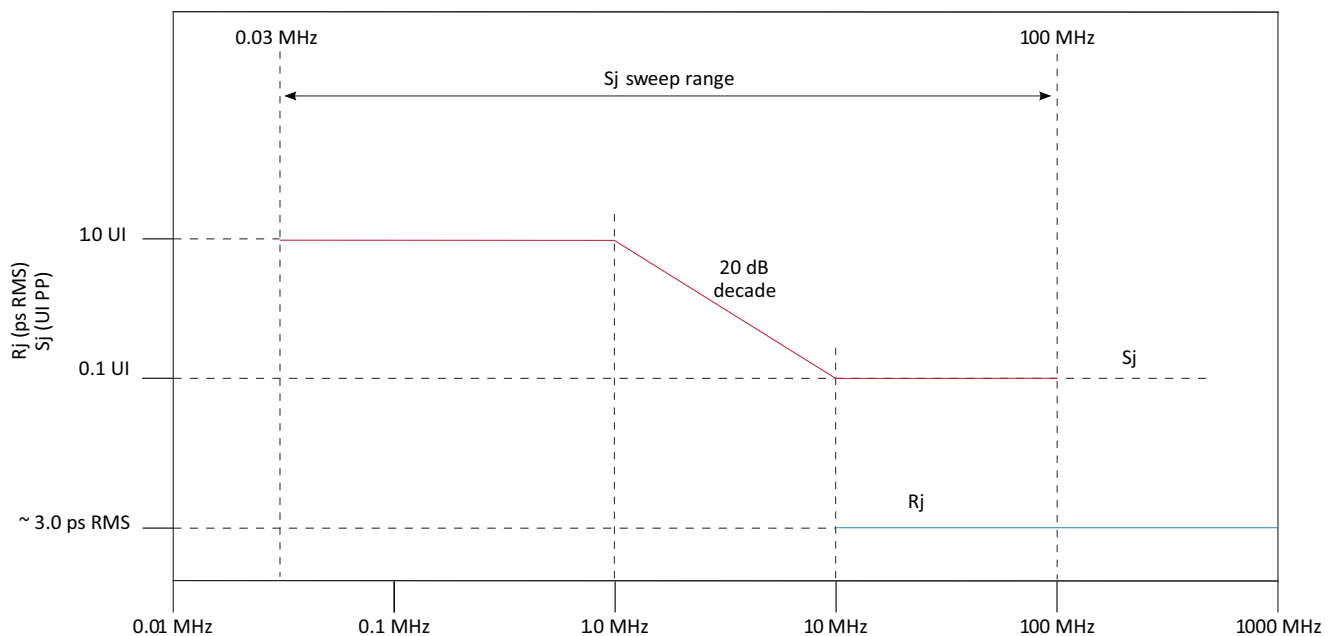
Notes: 1.  $T_{RX-SV-8G}$  is referenced to TP2P and obtained after post processing data captured at TP2.  $T_{RX-SV-8G}$  includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

2.  $V_{RX-SV-DIFF-8G}$  voltage may need to be adjusted over a wide range for the different loss calibration channels.

3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in [Figure 3-34](#).

4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See [Figure 3-34](#) for details. Rj may be adjusted to meet the 0.3 UI value for  $T_{RX-SV-8G}$ .

5. For recommended operating conditions, see [Table 3-2](#).

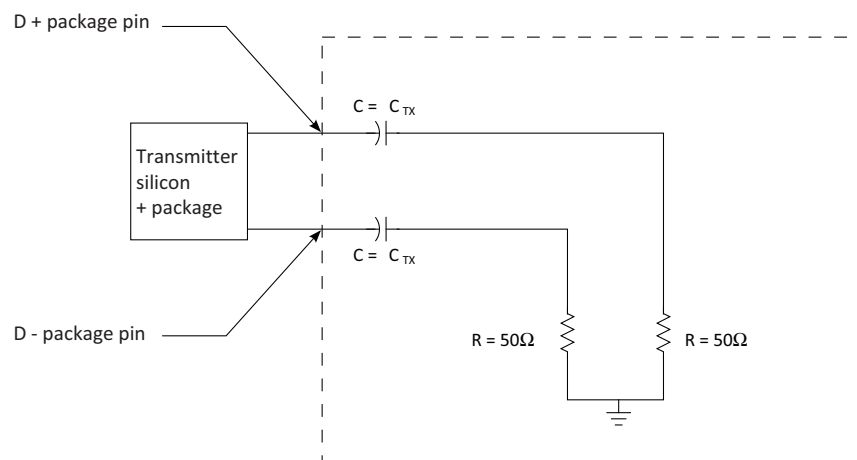
**Figure 3-34.** Swept sinusoidal jitter mask

#### 3.19.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

##### NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

**Figure 3-35.** Test/measurement load

## 3.19.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125 and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane.

All unit intervals are specified with a tolerance of  $\pm 100$  ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

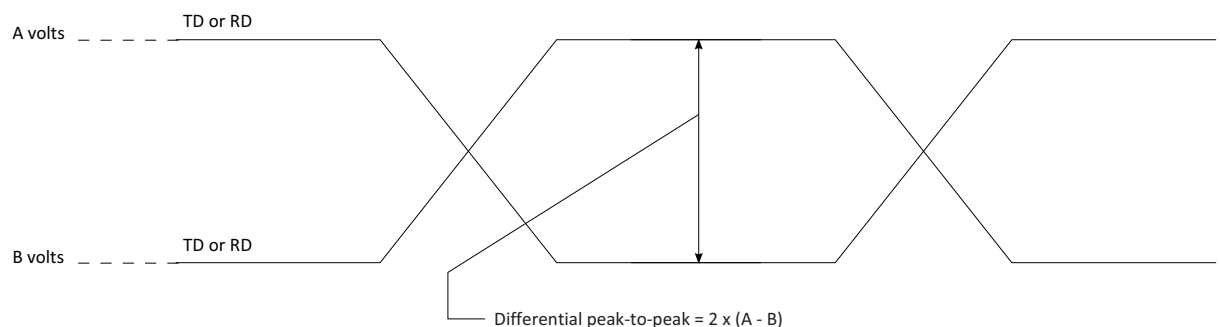
To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

### 3.19.5.1 Signal definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. The following figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and TD\_B) or a receiver input (RD and RD\_B). Each signal swings between A volts and B volts where  $A > B$ . Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals-TD, TD\_B, RD, and RD\_B-each have a peak-to-peak swing of  $A - B$  volts.
- The differential output signal of the transmitter,  $V_{OD}$ , is defined as  $V_{TD} - V_{TD\_B}$
- The differential input signal of the receiver,  $V_{ID}$ , is defined as  $V_{RD} - V_{RD\_B}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from  $A - B$  to  $-(A - B)$  volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is  $A - B$  volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is  $2 \times (A - B)$  volts.

**Figure 3-36.** Differential peak-to-peak voltage of transmitter or receiver



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs TD and TD\_B, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD\_B is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

### 3.19.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

### 3.19.5.3 Serial RapidIO clocking requirements for SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

SerDes 2 (SD2\_REF\_CLK[1:2]\_P and SD2\_REF\_CLK[1:2]\_N) may be used for various SerDes serial RapidIO configurations based on the RCW Configuration field SRDS\_PRTCL. Serial RapidIO is not supported on SerDes 1 and 2.

For more information on these specifications, see SerDes reference clocks.

### 3.19.5.4 DC requirements for serial RapidIO

This section explains the DC requirements for the serial RapidIO interface.

#### 3.19.5.4.1 DC serial RapidIO timing transmitter specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- –10 dB for (Baud Frequency)  $\sim 10 < \text{Freq}(f) < 625 \text{ MHz}$
- $-10 \text{ dB} + 10\log(f \sim 625 \text{ MHz}) \text{ dB}$  for  $625 \text{ MHz} = \text{Freq}(f) = \text{Baud Frequency}$

The reference impedance for the differential return loss measurements is 100- $\Omega$  resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud and 10ps at 5 GBaud.

This table defines the transmitter DC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud.

**Table 3-73.** Serial RapidIO transmitter DC timing specifications–2.5 GBaud, 3.125 GBaud<sup>(2)</sup>

| Parameter                             | Symbol                  | Min   | Typ | Max  | Unit     | Notes                                 |
|---------------------------------------|-------------------------|-------|-----|------|----------|---------------------------------------|
| Output voltage                        | $V_o$                   | –0.40 | –   | 2.30 | V        | (1)                                   |
| Long-run differential output voltage  | $V_{\text{DIFFPP}}$     | 800   | –   | 1600 | mV p-p   | –                                     |
| Short-run differential output voltage | $V_{\text{DIFFPP}}$     | 500   | –   | 1000 | mV p-p   | –                                     |
| DC Differential transmitter impedance | $Z_{\text{TX-DIFF-DC}}$ | 80    | 100 | 120  | $\Omega$ | Transmitter DC differential impedance |

Notes: 1. Voltage relative to COMMON of either signal comprising a differential pair

2. For recommended operating conditions, see Table 3-2.

This table defines the transmitter DC specifications for serial RapidIO operating at 5 GBaud.

**Table 3-74.** Serial RapidIO transmitter DC timing specifications-5 GBaud<sup>(1)</sup>

| Parameter  | Symbol                  | Min | Typ | Max  | Unit     | Notes |
|--|-------------------------|-----|-----|------|----------|-------|
| Long-run differential output voltage                       | $V_{DIFF}$              | 800 | —   | 1200 | mV       | —     |
| Short-run differential output voltage                      | $V_{DIFF}$              | 400 | —   | 750  | mV       | —     |
| Long-run de-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-3.5dB}$ | 3   | 3.5 | 4    | dB       | —     |
| Long-run de-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0 | 6.5  | dB       | —     |
| Differential resistance                                    | $T_{RD}$                | 80  | 100 | 120  | $\Omega$ | —     |

Notes: 1. For recommended operating conditions, see [Table 3-2](#).

## 3.19.5.4.2 DC serial RapidIO receiver specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to  $(0.8) \times (\text{Baud Frequency})$ . This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100- $\Omega$  resistive for differential return loss and 25- $\Omega$  resistive for common mode.

This table defines the receiver DC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud.

**Table 3-75.** Serial RapidIO receiver DC timing specifications—2.5 GBaud, 3.125 GBaud<sup>(2)</sup>

| Parameter                                | Symbol           | Min | Typ | Max  | Unit     | Notes                              |
|--|------------------|-----|-----|------|----------|------------------------------------|
| Differential input voltage               | $V_{IN}$         | 200 | —   | 1600 | mV p-p   | <sup>(1)</sup>                     |
| DC differential receiver input impedance | $Z_{RX-DIFF-DC}$ | 80  | 100 | 120  | $\Omega$ | Receiver DC differential impedance |

Notes: 1. Measured at the receiver

2. For recommended operating conditions, see [Table 3-2](#).

This table defines the receiver DC specifications for serial RapidIO operating at 5 GBaud.

**Table 3-76.** Serial RapidIO receiver DC timing specifications-5 GBaud<sup>(2)</sup>

| Parameter                            | Symbol     | Min | Typ | Max  | Unit     | Notes          |
|--------------------------------------|------------|-----|-----|------|----------|----------------|
| Long-run differential input voltage  | $V_{DIFF}$ | —   | —   | 1200 | mV       | <sup>(1)</sup> |
| Short-run differential input voltage | $V_{DIFF}$ | 125 | —   | 1200 | mV       | <sup>(1)</sup> |
| Differential resistance              | $R_{RD}$   | 80  | —   | 120  | $\Omega$ | —              |

Notes: 1. Measured at the receiver.

2. For recommended operating conditions, see [Table 3-2](#).

## 3.19.5.5 AC requirements for serial RapidIO

This section explains the AC requirements for the serial RapidIO interface.

### 3.19.5.5.1 AC requirements for serial RapidIO transmitter

This table defines the transmitter AC specifications for the serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

**Table 3-77.** Serial RapidIO transmitter AC timing specifications<sup>(1)</sup>

| Parameter                  | Symbol | Min          | Typical | Max          | Unit   |
|----------------------------|--------|--------------|---------|--------------|--------|
| Deterministic jitter       | $J_D$  | –            | –       | 0.17         | UI p-p |
| Total jitter               | $J_T$  | –            | –       | 0.35         | UI p-p |
| Unit Interval: 2.5 GBaud   | UI     | 400 – 100ppm | 400     | 400 + 100ppm | ps     |
| Unit Interval: 3.125 GBaud | UI     | 320 – 100ppm | 320     | 320 + 100ppm | ps     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This table defines the transmitter AC specifications for the serial RapidIO operating at 5 GBaud. The AC timing specifications do not include RefClk jitter.

**Table 3-78.** Serial RapidIO transmitter AC timing specifications<sup>(1)</sup>

| Parameter                            | Symbol     | Min            | Typical | Max            | Unit   |
|--------------------------------------|------------|----------------|---------|----------------|--------|
| Baud rate                            | $T_{BAUD}$ | 5.000 – 100ppm | 5.000   | 5.000 + 100ppm | Gb/s   |
| Uncorrelated high probability jitter | $T_{UHPJ}$ | –              | –       | 0.15           | UI p-p |
| Total jitter                         | $T_J$      | –              | –       | 0.30           | UI p-p |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This table defines the receiver AC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

**Table 3-79.** Serial RapidIO receiver AC timing specifications<sup>(3)</sup>

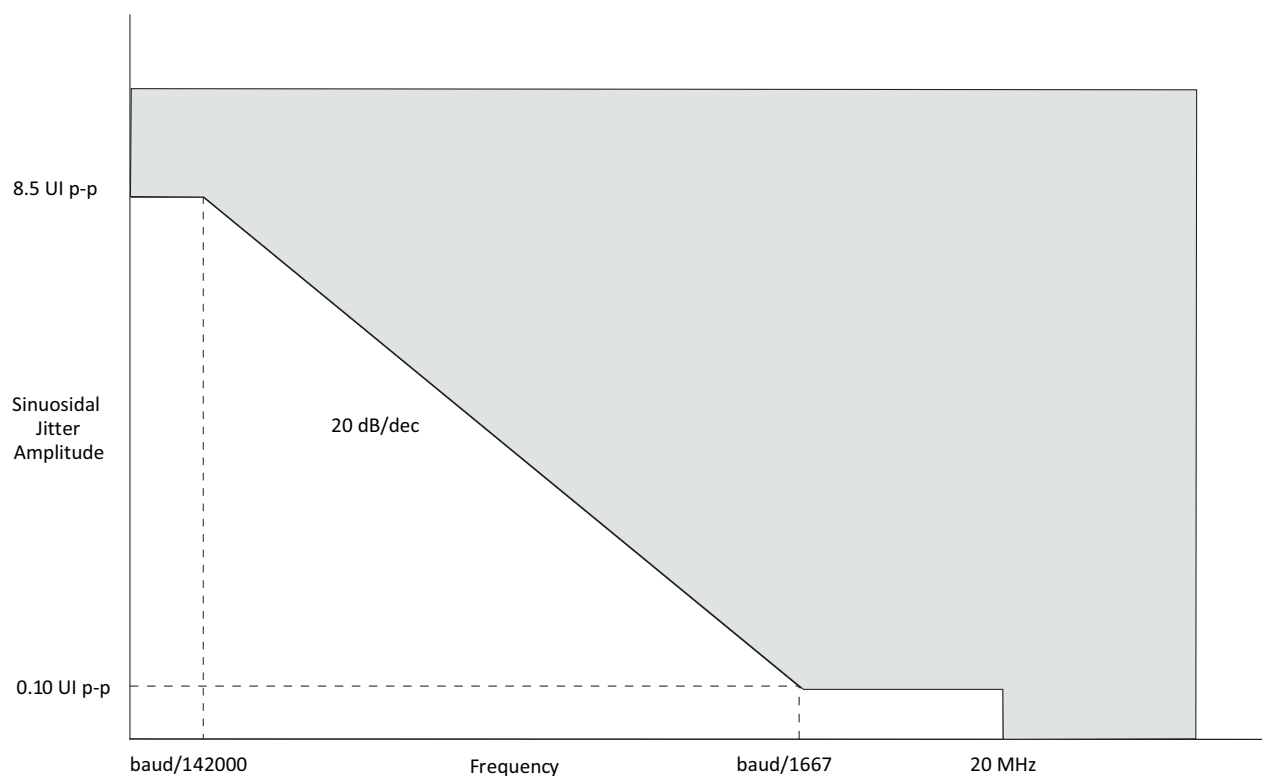
| Parameter  | Symbol   | Min          | Typical | Max          | Unit   | Notes |
|--|----------|--------------|---------|--------------|--------|-------|
| Deterministic jitter tolerance                     | $J_D$    | –            | –       | 0.37         | UI p-p | (1)   |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | –            | –       | 0.55         | UI p-p | (1)   |
| Total jitter tolerance <sup>(2)</sup>              | $J_T$    | –            | –       | 0.65         | UI p-p | (1)   |
| Bit error rate                                     | BER      | –            | –       | $10^{-12}$   | –      | –     |
| Unit Interval: 2.5 GBaud                           | UI       | 400 – 100ppm | 400     | 400 + 100ppm | ps     | –     |
| Unit Interval: 3.125 GBaud                         | UI       | 320 – 100ppm | 320     | 320 + 100ppm | ps     | –     |

Notes: 1. Measured at receiver

- Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 3-37](#). The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.
- For recommended operating conditions, see [Table 3-2](#).

This figure shows the single-frequency sinusoidal jitter limits for 2.5GBaud and 3.125GBaud rates.

**Figure 3-37.** Single-frequency sinusoidal jitter limits



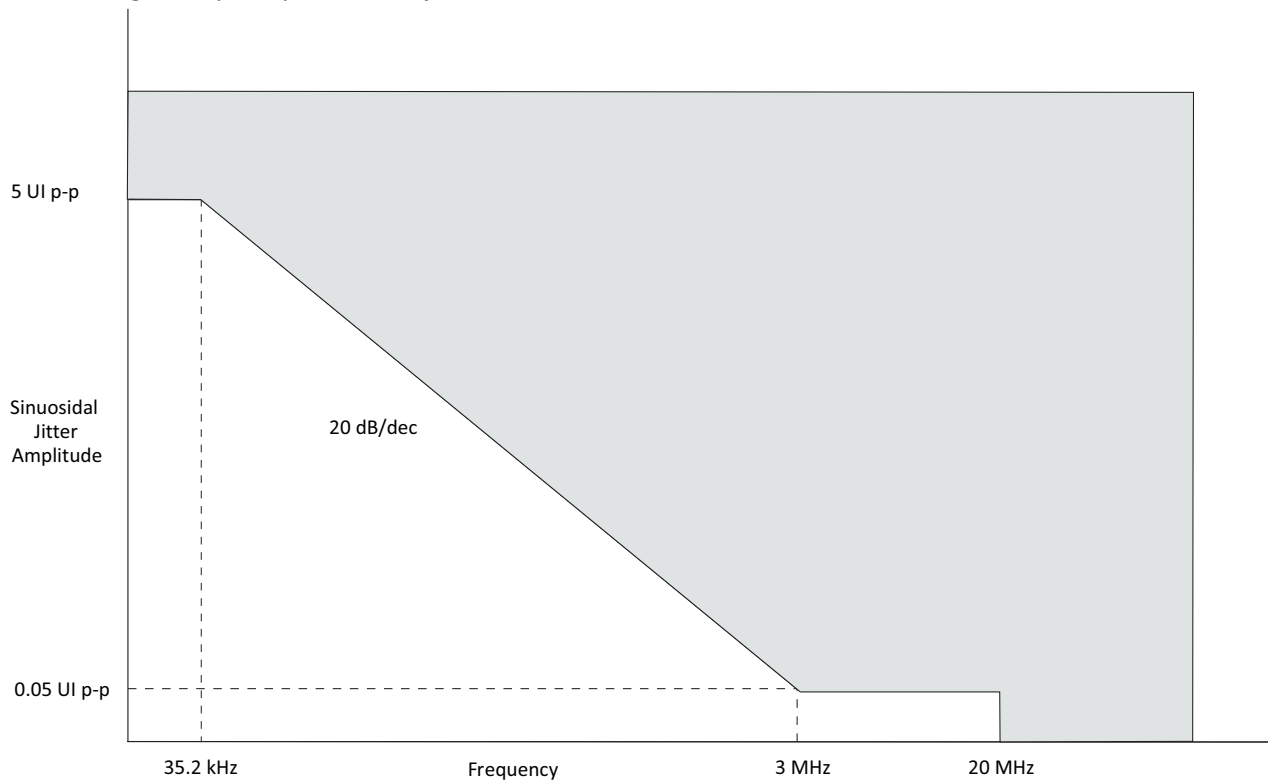
This table defines the receiver AC specifications for serial RapidIO operating at 5 GBaud. The AC timing specifications do not include RefClk jitter.

**Table 3-80.** Serial RapidIO receiver AC timing specifications<sup>(1)</sup>

| Parameter   | Symbol              | Min            | Typical | Max            | Unit   | Notes |
|---|---------------------|----------------|---------|----------------|--------|-------|
| Receiver baud rate  | $R_{\text{BAUD}}$   | 5.000 - 100ppm | 5.000   | 5.000 + 100ppm | Gb/s   | –     |
| Long-run Gaussian jitter                                    | $R_{\text{GJ}}$     | –              | –       | 0.275          | UI p-p | –     |
| Uncorrelated bounded high probability jitter                | $R_{\text{DJ}}$     | –              | –       | 0.15           | UI p-p | –     |
| Long-run correlated bounded high probability jitter         | $R_{\text{CBHPJ}}$  | –              | –       | 0.525          | UI p-p | –     |
| Short-run correlated bounded high probability jitter        | $R_{\text{CBHPJ}}$  | –              | –       | 0.30           | UI p-p | –     |
| Long-run bounded high probability jitter                    | $R_{\text{BHPJ}}$   | –              | –       | 0.675          | UI p-p | –     |
| Short-run bounded high probability jitter                   | $R_{\text{BHPJ}}$   | –              | –       | 0.45           | UI p-p | –     |
| Sinusoidal jitter, maximum                                  | $R_{\text{SJ-max}}$ | –              | –       | 5.00           | UI p-p | –     |
| Sinusoidal jitter, high frequency                           | $R_{\text{SJ-hf}}$  | –              | –       | 0.05           | UI p-p | –     |
| Long-run total jitter (does not include sinusoidal jitter)  | $R_{\text{TJ}}$     | –              | –       | 0.95           | UI p-p | –     |
| Short-run total jitter (does not include sinusoidal jitter) | $R_{\text{TJ}}$     | –              | –       | 0.60           | UI p-p | –     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

This figure shows the single-frequency sinusoidal jitter limits for 5GBaud rate.

**Figure 3-38.** Single-frequency sinusoidal jitter limits

### 3.19.6 XAUI interface

This section describes the DC and AC electrical specifications for the XAUI bus.

#### 3.19.6.1 XAUI DC electrical characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

##### 3.19.6.1.1 DC requirements for XAUI SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

Only SerDes 1 (SD1\_REF\_CLK[1:2]\_P and SD1\_REF\_CLK[1:2]\_N) may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS\_PRTCL.

For more information on these specifications, see [SerDes reference clocks](#).

##### 3.19.6.1.2 XAUI transmitter DC electrical characteristics

This table defines the XAUI transmitter DC electrical characteristics.

**Table 3-81.** XAUI transmitter DC electrical characteristics (XVDD = 1.35 V)<sup>(1)</sup>

| Parameter                             | Symbol           | Min   | Typical | Max  | Unit     | Notes |
|---------------------------------------|------------------|-------|---------|------|----------|-------|
| Output voltage                        | $V_o$            | -0.40 | –       | 2.30 | V        | (2)   |
| Differential output voltage           | $V_{DIFFPP}$     | 800   | 1000    | 1600 | mV p-p   | –     |
| DC Differential transmitter impedance | $Z_{TX-DIFF-DC}$ | 80    | 100     | 120  | $\Omega$ | (3)   |

Notes: 1. For recommended operating conditions, see [Table 3-2](#).

2. Absolute output voltage limit

3. Transmitter DC differential impedance

##### 3.19.6.1.3 XAUI receiver DC electrical characteristics



This table defines the XAUI receiver DC electrical characteristics.

**Table 3-82.** XAUI receiver DC timing specifications (SVDD = 1.0 V)<sup>(1)</sup>

| Parameter                                | Symbol           | Min | Typical | Max  | Unit     | Notes |
|--|------------------|-----|---------|------|----------|-------|
| Differential input voltage               | $V_{IN}$         | 200 | –       | 1600 | mV p-p   | (2)   |
| DC Differential receiver input impedance | $Z_{RX-DIFF-DC}$ | 80  | 100     | 120  | $\Omega$ | (3)   |

- Notes:
1. For recommended operating conditions, see [Table 3-2](#).
  2. Measured at the receiver
  3. Receiver DC differential impedance

## 3.19.6.2 XAUI AC timing specifications

This section explains the AC requirements for the XAUI interface.

### 3.19.6.2.1 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

**Table 3-83.** XAUI transmitter AC timing specifications<sup>(1)</sup>

| Parameter                  | Symbol | Min           | Typical | Max           | Unit   |
|----------------------------|--------|---------------|---------|---------------|--------|
| Deterministic jitter       | $J_D$  | –             | –       | 0.17          | UI p-p |
| Total jitter               | $J_T$  | –             | –       | 0.35          | UI p-p |
| Unit Interval: 3.125 GBaud | UI     | 320 – 100 ppm | 320     | 320 + 100 ppm | ps     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.6.2.2 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

**Table 3-84.** XAUI receiver AC timing specifications<sup>(1)</sup>

| Parameter  | Symbol   | Min           | Typical | Max           | Unit   | Notes  |
|--|----------|---------------|---------|---------------|--------|--------|
| Deterministic jitter tolerance                     | $J_D$    | –             | –       | 0.37          | UI p-p | (2)    |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | –             | –       | 0.55          | UI p-p | (2)    |
| Total jitter tolerance                             | $J_T$    | –             | –       | 0.65          | UI p-p | (2)(3) |
| Bit error rate                                     | BER      | –             | –       | $10^{-12}$    | –      | –      |
| Unit Interval: 3.125 GBaud                         | UI       | 320 – 100 ppm | 320     | 320 + 100 ppm | ps     | –      |

- Notes:
1. For recommended operating conditions, see [Table 3-2](#).
  2. Measured at receiver
  3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 3-38](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

## 3.19.7 Aurora interface

This section describes the Aurora clocking requirements and its DC and AC electrical characteristics.

### 3.19.7.1 Aurora clocking requirements for SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

Only SerDes 2 (SD2\_REF\_CLK[1:2]\_P and SD2\_REF\_CLK[1:2]\_N) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS\_PRTCL. Aurora is not supported on SerDes 1-3.

For more information on these specifications, see SerDes reference clocks.

### 3.19.7.2 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for the Aurora interface.

#### 3.19.7.2.1 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

**Table 3-85.** Aurora transmitter DC electrical characteristics (XVDD = 1.35 V)<sup>(1)</sup>

| Parameter                             | Symbol           | Min | Typical | Max  | Unit     |
|---------------------------------------|------------------|-----|---------|------|----------|
| Differential output voltage           | $V_{DIFFPP}$     | 800 | 1000    | 1600 | mV p-p   |
| DC Differential transmitter impedance | $Z_{TX-DIFF-DC}$ | 80  | 100     | 120  | $\Omega$ |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

#### 3.19.7.2.2 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for the Aurora interface.

**Table 3-86.** Aurora receiver DC electrical characteristics (SVDD = 1.0 V)<sup>(1)</sup>

| Parameter                          | Symbol           | Min | Typical | Max  | Unit     | Notes |
|------------------------------------|------------------|-----|---------|------|----------|-------|
| Differential input voltage         | $V_{IN}$         | 200 | —       | 1600 | mV p-p   | (2)   |
| DC Differential receiver impedance | $Z_{RX-DIFF-DC}$ | 80  | 100     | 120  | $\Omega$ | (3)   |

Notes: 1. For recommended operating conditions, see [Table 3-2](#).

2. Measured at receiver

3. C Differential receiver impedance

### 3.19.7.3 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

#### 3.19.7.3.1 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

**Table 3-87.** Aurora transmitter AC timing specifications<sup>(1)</sup>

| Parameter            | Symbol | Min | Typical | Max  | Unit   |
|----------------------|--------|-----|---------|------|--------|
| Deterministic jitter | $J_D$  | —   | —       | 0.17 | UI p-p |
| Total jitter         | $J_T$  | —   | —       | 0.35 | UI p-p |

**Table 3-87.** Aurora transmitter AC timing specifications<sup>(1)</sup>

|                            |    |               |     |               |    |
|----------------------------|----|---------------|-----|---------------|----|
| Unit interval: 2.5 GBaud   | UI | 400 – 100 ppm | 400 | 400 + 100 ppm | ps |
| Unit interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps |
| Unit interval: 5.0 GBaud   | UI | 200 – 100 ppm | 200 | 200 + 100 ppm | ps |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.7.3.2 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

**Table 3-88.** Aurora receiver AC timing specifications<sup>(3)</sup>

| Parameter  | Symbol          | Min           | Typ | Max               | Units  | Notes  |
|--|-----------------|---------------|-----|-------------------|--------|--------|
| Deterministic jitter tolerance                     | J <sub>D</sub>  | –             | –   | 0.37              | UI p-p | (1)    |
| Combined deterministic and random jitter tolerance | J <sub>DR</sub> | –             | –   | 0.55              | UI p-p | (1)    |
| Total jitter tolerance                             | J <sub>T</sub>  | –             | –   | 0.65              | UI p-p | (1)(2) |
| Bit error rate                                     | BER             | –             | –   | 10 <sup>-12</sup> | –      | –      |
| Unit Interval: 2.5 GBaud                           | UI              | 400 – 100 ppm | 400 | 400 + 100 ppm     | ps     | –      |
| Unit Interval: 3.125 GBaud                         | UI              | 320 – 100 ppm | 320 | 320 + 100 ppm     | ps     | –      |
| Unit Interval: 5.0 GBaud                           | UI              | 200 – 100 ppm | 200 | 200 + 100 ppm     | ps     | –      |

Notes: 1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 3-37](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see [Table 3-2](#).

## 3.19.8 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

### 3.19.8.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

#### 3.19.8.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

**Table 3-89.** Gen1i/1m 1.5G transmitter DC specifications (XVDD = 1.35 V)<sup>(3)</sup>

| Parameter                      | Symbol                     | Min | Typ | Max | Units  | Notes |
|--------------------------------|----------------------------|-----|-----|-----|--------|-------|
| Tx differential output voltage | V <sub>SATA_TXDIFF</sub>   | 400 | 500 | 600 | mV p-p | (1)   |
| Tx differential pair impedance | Z <sub>SATA_TXDIFFIM</sub> | 85  | 100 | 115 | Ω      | (2)   |

Notes: 1. Terminated by 50Ω load.

2. DC impedance

3. For recommended operating conditions, see [Table 3-2](#).

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

**Table 3-90.** Gen 2i/2m 3G transmitter DC specifications (XVDD = 1.35 V)<sup>(2)</sup>

| Parameter                               | Symbol                      | Min | Typ | Max | Units    | Notes |
|---|-----------------------------|-----|-----|-----|----------|-------|
| Transmitter differential output voltage | $V_{\text{SATA\_TXDIFF}}$   | 400 | –   | 700 | mV p-p   | (1)   |
| Transmitter differential pair impedance | $Z_{\text{SATA\_TXDIFFIM}}$ | 85  | 100 | 115 | $\Omega$ | –     |

Notes: 1. Terminated by 50 $\Omega$  load.

2. For recommended operating conditions, see [Table 3-2](#).

### 3.19.8.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

**Table 3-91.** Gen1i/1m 1.5 G receiver input DC specifications (SVDD = 1.0 V)<sup>(3)</sup>

| Parameter                             | Symbol                    | Min | Typical | Max | Units    | Notes |
|---------------------------------------|---------------------------|-----|---------|-----|----------|-------|
| Differential input voltage            | $V_{\text{SATA\_RXDIFF}}$ | 240 | 500     | 600 | mV p-p   | (1)   |
| Differential receiver input impedance | $Z_{\text{SATA\_RXSEIM}}$ | 85  | 100     | 115 | $\Omega$ | (2)   |
| OOB signal detection threshold        | $V_{\text{SATA\_OOB}}$    | 50  | 120     | 240 | mV p-p   | –     |

Notes: 1. Voltage relative to common of either signal comprising a differential pair

2. DC impedance

3. For recommended operating conditions, see [Table 3-2](#).

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

**Table 3-92.** Gen2i/2m 3 G receiver input DC specifications (SVDD = 1.0 V)<sup>(3)</sup>

| Parameter                             | Symbol                    | Min | Typ | Max | Unit     | Notes |
|---------------------------------------|---------------------------|-----|-----|-----|----------|-------|
| Differential input voltage            | $V_{\text{SATA\_RXDIFF}}$ | 240 | –   | 750 | mV p-p   | (1)   |
| Differential receiver input impedance | $Z_{\text{SATA\_RXSEIM}}$ | 85  | 100 | 115 | $\Omega$ | (2)   |
| OOB signal detection threshold        | $V_{\text{SATA\_OOB}}$    | 75  | 120 | 240 | mV p-p   | (2)   |

Notes: 1. Voltage relative to common of either signal comprising a differential pair

2. DC impedance

3. For recommended operating conditions, see [Table 3-2](#).

### 3.19.8.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

#### 3.19.8.2.1 AC requirements for SATA REF\_CLK

The AC requirements for the SATA reference clock listed in this table are to be guaranteed by the customer's application design.

This figure shows the reference clock timing waveform.

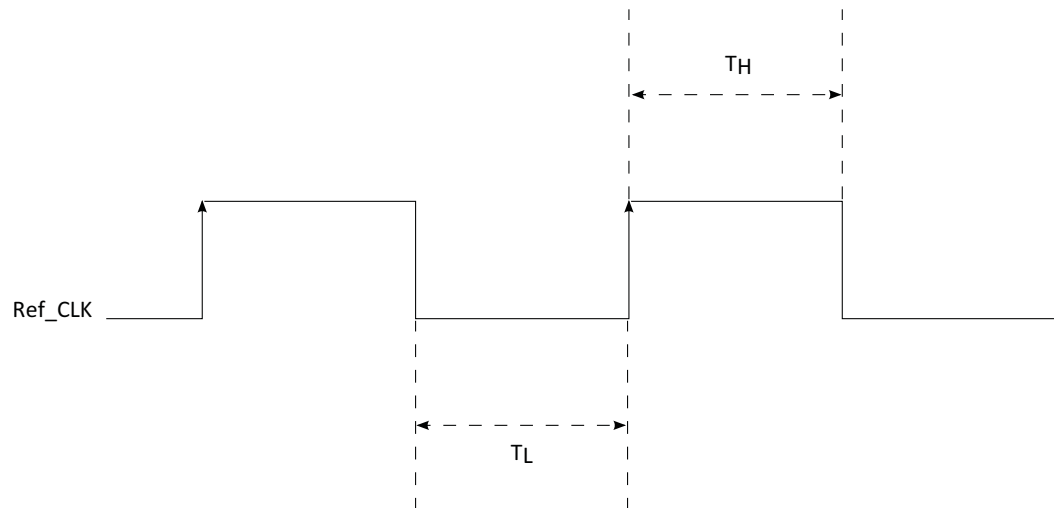
**Table 3-93.** SATA reference clock input requirements<sup>(6)</sup>

| Parameter   | Symbol          | Min  | Typ     | Max  | Unit | Notes     |
|---|-----------------|------|---------|------|------|-----------|
| SDn_REF_CLKn_P/SDn_REF_CLKn_N frequency range   | $t_{CLK\_REF}$  | —    | 100/125 | —    | MHz  | (1)       |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N clock frequency tolerance                                 | $t_{CLK\_TOL}$  | −350 | —       | +350 | ppm  | —         |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N reference clock duty cycle                                | $t_{CLK\_DUTY}$ | 40   | 50      | 60   | %    | (5)       |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N cycle- to-cycle clock jitter (period jitter)              | $t_{CLK\_CJ}$   | —    | —       | 100  | ps   | (2)       |
| SDn_REF_CLKn_P/SDn_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak) | $t_{CLK\_PJ}$   | −50  | —       | +50  | ps   | (2)(3)(4) |

Notes: 1. **Caution:** Only 100 and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.

- At RefClk input
- In a frequency band from 150 kHz to 15 MHz at BER of  $10^{-12}$
- Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
- Measurement taken from differential waveform
- For recommended operating conditions, see [Table 3-2](#).

**Figure 3-39.** Reference clock timing waveform



### 3.19.8.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 3-94.** Gen1i/1m 1.5 G transmitter AC specifications<sup>(2)</sup>

| Parameter                   | Symbol              | Min      | Typical  | Max      | Units  | Notes |
|-----------------------------|---------------------|----------|----------|----------|--------|-------|
| Channel speed               | $t_{CH\_SPEED}$     | —        | 1.5      | —        | Gbps   | —     |
| Unit Interval               | $T_{UI}$            | 666.4333 | 666.6667 | 670.2333 | ps     | —     |
| Total jitter data-data 5 UI | $U_{SATA\_TXTJSUI}$ | —        | —        | 0.355    | UI p-p | (1)   |

**Table 3-94.** Gen1i/1m 1.5 G transmitter AC specifications<sup>(2)</sup>

|  |                              |   |   |       |        |     |
|--|------------------------------|---|---|-------|--------|-----|
| Total jitter, data-data 250 UI         | $U_{\text{SATA\_TXTJ250UI}}$ | — | — | 0.47  | UI p-p | (1) |
| Deterministic jitter, data-data 5 UI   | $U_{\text{SATA\_TXDJ5UI}}$   | — | — | 0.175 | UI p-p | (1) |
| Deterministic jitter, data-data 250 UI | $U_{\text{SATA\_TXDJ250UI}}$ | — | — | 0.22  | UI p-p | (1) |

Notes: 1. Measured at transmitter output pins peak to peak phase variation, random data pattern  
 2. For recommended operating conditions, see [Table 3-2](#).

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 3-95.** Gen 2i/2m 3 G transmitter AC specifications<sup>(2)</sup>

| Parameter   | Symbol                         | Min      | Typical  | Max      | Units  | Notes |
|---|--------------------------------|----------|----------|----------|--------|-------|
| Channel speed   | $t_{\text{CH\_SPEED}}$         | —        | 3.0      | —        | Gbps   | —     |
| Unit Interval   | $T_{\text{UI}}$                | 333.2167 | 333.3333 | 335.1167 | ps     | —     |
| Total jitter $f_{\text{C3dB}} = f_{\text{BAUD}} \div 500$           | $U_{\text{SATA\_TXTJfB/500}}$  | —        | —        | 0.37     | UI p-p | (1)   |
| Total jitter $f_{\text{C3dB}} = f_{\text{BAUD}} \div 1667$          | $U_{\text{SATA\_TXTJfB/1667}}$ | —        | —        | 0.55     | UI p-p | (1)   |
| Deterministic jitter, $f_{\text{C3dB}} = f_{\text{BAUD}} \div 500$  | $U_{\text{SATA\_TXDJfB/500}}$  | —        | —        | 0.19     | UI p-p | (1)   |
| Deterministic jitter, $f_{\text{C3dB}} = f_{\text{BAUD}} \div 1667$ | $U_{\text{SATA\_TXDJfB/1667}}$ | —        | —        | 0.35     | UI p-p | (1)   |

Notes: 1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern  
 2. For recommended operating conditions, see [Table 3-2](#).

#### 3.19.8.4 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

**Table 3-96.** Gen 1i/1m 1.5G receiver AC specifications<sup>(2)</sup>

| Parameter                              | Symbol                       | Min      | Typical  | Max      | Units  | Notes |
|--|------------------------------|----------|----------|----------|--------|-------|
| Unit Interval                          | $T_{\text{UI}}$              | 666.4333 | 666.6667 | 670.2333 | ps     | —     |
| Total jitter data-data 5 UI            | $U_{\text{SATA\_RXTJ5UI}}$   | —        | —        | 0.43     | UI p-p | (1)   |
| Total jitter, data-data 250 UI         | $U_{\text{SATA\_RXTJ250UI}}$ | —        | —        | 0.60     | UI p-p | (1)   |
| Deterministic jitter, data-data 5 UI   | $U_{\text{SATA\_RXDJ5UI}}$   | —        | —        | 0.25     | UI p-p | (1)   |
| Deterministic jitter, data-data 250 UI | $U_{\text{SATA\_RXDJ250UI}}$ | —        | —        | 0.35     | UI p-p | (1)   |

Notes: 1. Measured at receiver.  
 2. For recommended operating conditions, see [Table 3-2](#).

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 3-97.** Gen 2i/2m 3G receiver AC specifications<sup>(2)</sup>

| Parameter   | Symbol                        | Min      | Typical  | Max      | Units  | Notes |
|---|-------------------------------|----------|----------|----------|--------|-------|
| Unit Interval   | $T_{\text{UI}}$               | 333.2167 | 333.3333 | 335.1167 | ps     | —     |
| Total jitter $f_{\text{C3dB}} = f_{\text{BAUD}} \div 500$ | $U_{\text{SATA\_RXTJfB/500}}$ | —        | —        | 0.60     | UI p-p | (1)   |

**Table 3-97.** Gen 2i/2m 3G receiver AC specifications<sup>(2)</sup>

|   |                         |   |   |      |        |     |
|---|-------------------------|---|---|------|--------|-----|
| Total jitter $f_{C3dB} = f_{BAUD} \div 1667$          | $U_{SATA\_RXTJfB/1667}$ | — | — | 0.65 | UI p-p | (1) |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$  | $U_{SATA\_RXDJfB/500}$  | — | — | 0.42 | UI p-p | (1) |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA\_RXDJfB/1667}$ | — | — | 0.35 | UI p-p | (1) |

Notes: 1. Measured at receiver  
2. For recommended operating conditions, see [Table 3-2](#).

## 3.19.9 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in [Figure 3-40](#), where CTX is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGNDn. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 3-33](#).

### 3.19.9.1 SGMII clocking requirements for SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

When operating in SGMII mode, the ECn\_GTX\_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1\_REF\_CLK[1:2]\_P and SD1\_REF\_CLK[1:2]\_Npins. SerDes 1 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS\_PRTCL.

For more information on these specifications, see SerDes reference clocks.

### 3.19.9.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

#### 3.19.9.2.1 SGMII and SGMII 2.5x transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn\_TXn\_P and SDn\_TXn\_N) as shown in [Figure 3-41](#).

**Table 3-98.** SGMII DC transmitter electrical characteristics (XVDD = 1.35 V)<sup>(4)</sup>

| Parameter   | Symbol     | Min                  | Typ   | Max                           | Unit | Notes |
|---|------------|----------------------|-------|-------------------------------|------|-------|
| Output high voltage   | $V_{OH}$   | —                    | —     | $1.5 \times  V_{OD} _{I-max}$ | mV   | (1)   |
| Output low voltage  | $V_{OL}$   | $ V_{OD} _{I-min}/2$ | —     | —                             | mV   | (1)   |
| Output differential voltage <sup>(2)(3)</sup><br>(XV <sub>DD-Typ</sub> at 1.35 V) | $ V_{OD} $ | 320                  | 500.0 | 725.0                         | mV   | —     |
|   |            | 293.8                | 459.0 | 665.6                         |      | —     |
|   |            | 266.9                | 417.0 | 604.7                         |      | —     |
|   |            | 240.6                | 376.0 | 545.2                         |      | —     |
|   |            | 213.1                | 333.0 | 482.9                         |      | —     |
|   |            | 186.9                | 292.0 | 423.4                         |      | —     |
|   |            | 160.0                | 250.0 | 362.5                         |      | —     |
| Output impedance (differential)   | $R_O$      | 80                   | 100   | 120                           | Ω    | —     |

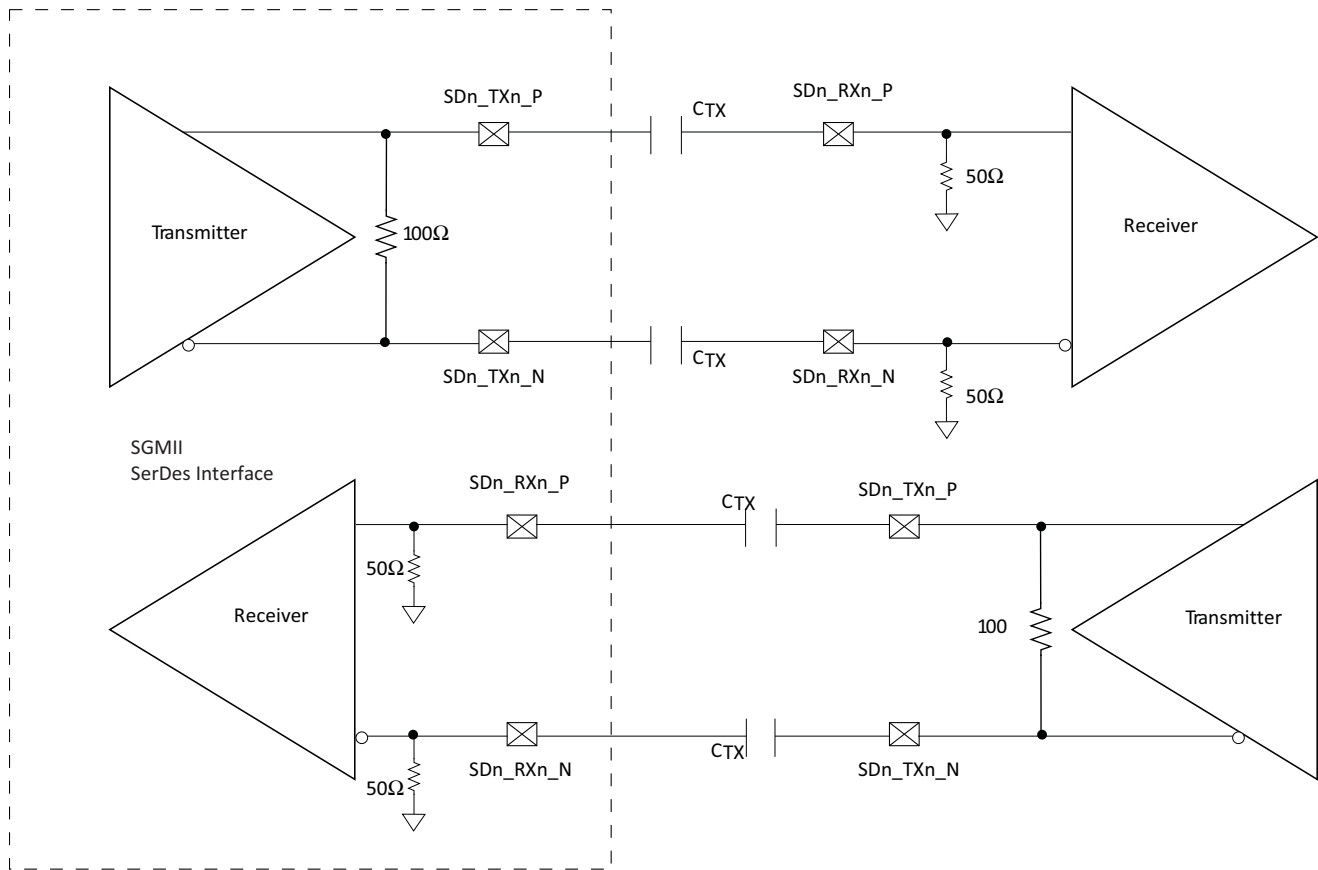
Notes: 1. This does not align to DC-coupled SGMII.

2.  $|V_{OD}| = |V_{SD\_TXn\_P} - V_{SD\_TXn\_N}|$ .  $|V_{OD}|$  is also referred to as output differential peak voltage.  $V_{TX-DIFFP-P} = 2 \times |V_{OD}|$ .
3. The  $|V_{OD}|$  value shown in the Typ column is based on the condition of  $XVDD\_SRDSn-Typ = 1.35\text{ V}$ , no common mode offset variation. SerDes transmitter is terminated with  $100\text{-}\Omega$  differential load between  $SDn\_TXn\_P$  and  $SDn\_TXn\_N$ .
4. For recommended operating conditions, see [Table 3-2](#).

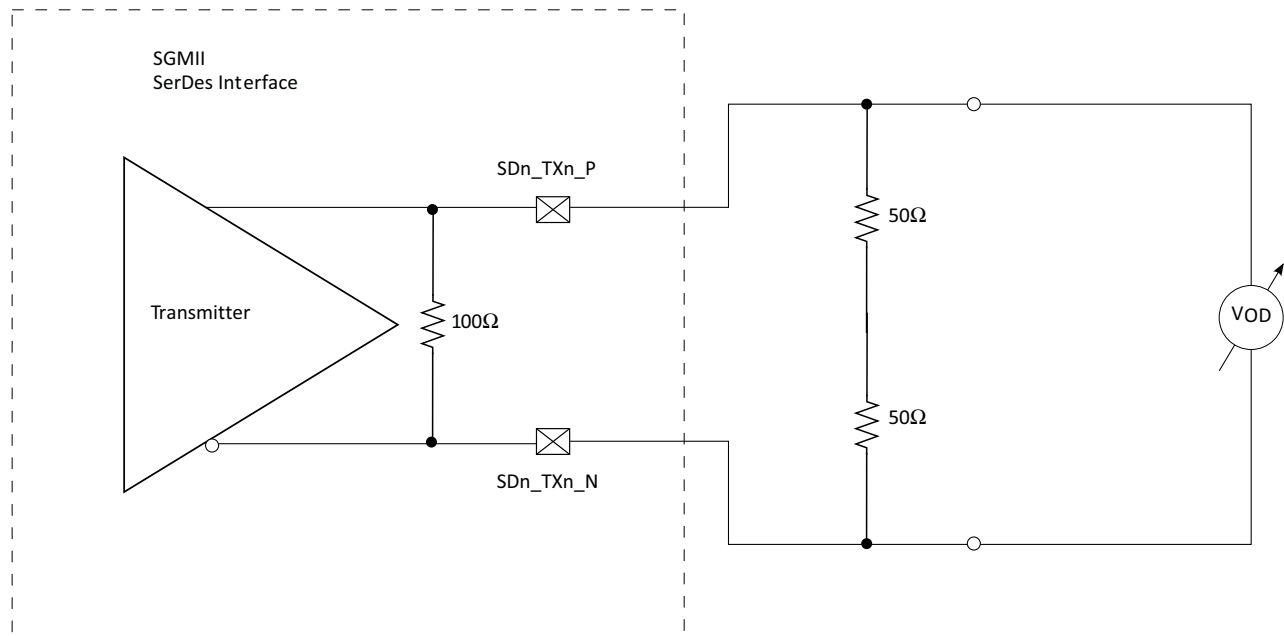
This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.



**Figure 3-40.** 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

**Figure 3-41.** SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 Gbaud.

**Table 3-99.** SGMII 2.5x transmitter DC electrical characteristics (XVDD = 1.35 V)<sup>(1)</sup>

| Parameter                       | Symbol     | Min | Typical | Max | Unit     | Notes |
|---------------------------------|------------|-----|---------|-----|----------|-------|
| Output differential voltage     | $ V_{OD} $ | 400 | –       | 600 | mV       | –     |
| Output impedance (differential) | $R_o$      | 80  | 100     | 120 | $\Omega$ | –     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.9.2.2 SGMII and SGMII 2.5x DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

**Table 3-100.** SGMII DC receiver electrical characteristics (SVDD = 1.0V)<sup>(4)</sup>

| Parameter                             |   | Symbol                  | Min | Typ | Max  | Unit | Notes |
|---------------------------------------|---|-------------------------|-----|-----|------|------|-------|
| DC input voltage range                |   | –                       | N/A |     |      | –    | (1)   |
| Input differential voltage            | – | V <sub>RX_DIFFp-p</sub> | 100 | –   | 1200 | mV   | (2)   |
|                                       | – |                         | 175 | –   |      |      |       |
| Loss of signal threshold              | – | V <sub>LOS</sub>        | 30  | –   | 100  | mV   | (3)   |
|                                       | – |                         | 65  | –   | 175  |      |       |
| Receiver differential input impedance |   | Z <sub>RX_DIFF</sub>    | 80  | –   | 120  | Ω    | –     |

Notes: 1. Input must be externally AC coupled.

2.  $V_{RX\_DIFFp-p}$  is also referred to as peak-to-peak input differential voltage.

3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See [PCI Express DC physical layer receiver specifications](#), and [PCI Express AC physical layer receiver specifications](#), for further explanation.

4. For recommended operating conditions, see [Table 3-2](#).

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

**Table 3-101.** SGMII 2.5x receiver DC timing specifications (SVDD = 1.0V)<sup>(1)</sup>

| Parameter                             | Symbol            | Min | Typical | Max  | Unit     | Notes |
|---------------------------------------|-------------------|-----|---------|------|----------|-------|
| Input differential voltage            | $V_{RX\_DIFFp-p}$ | 200 | —       | 1200 | mV       | —     |
| Loss of signal threshold              | $V_{LOS}$         | 75  | —       | 200  | mV       | —     |
| Receiver differential input impedance | $Z_{RX\_DIFF}$    | 80  | —       | 120  | $\Omega$ | —     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

## 3.19.9.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

### 3.19.9.3.1 SGMII and SGMII 2.5x transmit AC timing specifications

This table provides the SGMII and SGMII 2.5x transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

**Table 3-102.** SGMII transmit AC timing specifications<sup>(4)</sup>

| Parameter                               | Symbol   | Min           | Typ | Max           | Unit   | Notes |
|---|----------|---------------|-----|---------------|--------|-------|
| Deterministic jitter                    | $J_D$    | —             | —   | 0.17          | UI p-p | —     |
| Total jitter                            | $J_T$    | —             | —   | 0.35          | UI p-p | (2)   |
| Unit Interval: 1.25 GBaud (SGMII)       | UI       | 800 - 100 ppm | 800 | 800 + 100 ppm | ps     | (1)   |
| Unit Interval: 3.125 GBaud (2.5x SGMII) | UI       | 320 - 100 ppm | 320 | 320 + 100 ppm | ps     | (1)   |
| AC coupling capacitor                   | $C_{TX}$ | 10            | —   | 200           | nF     | (3)   |

Notes: 1. Each UI is 800 ps  $\pm$  100 ppm or 320 ps  $\pm$  100 ppm.

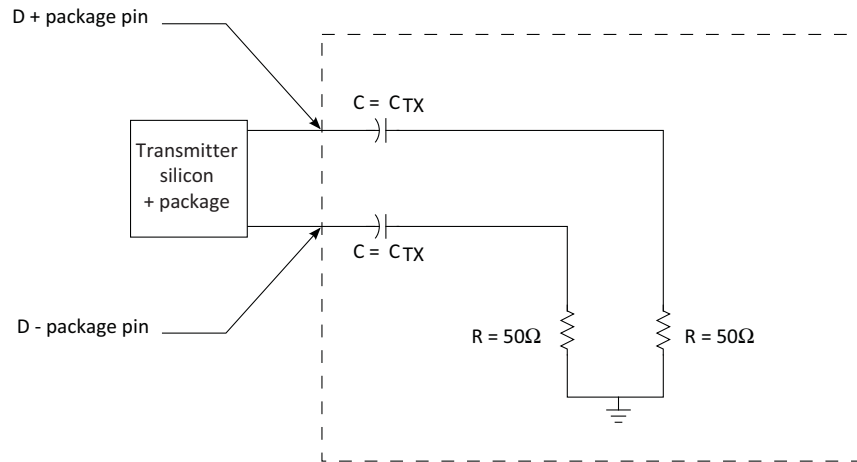
2. See [Figure 3-37](#) for single frequency sinusoidal jitter measurements.

3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

4. For recommended operating conditions, see [Table 3-2](#).

### 3.19.9.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SDn\_TXn\_P and SDn\_TXn\_N) or at the receiver inputs (SDn\_RXn\_P and SDn\_RXn\_N) respectively, as depicted in this figure.

**Figure 3-42.** SGMII AC test/measurement load

### 3.19.9.3.3 SGMII and SGMII 2.5x receiver AC timing Specification

This table provides the SGMII and SGMII 2.5x receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

**Table 3-103.** SGMII Receive AC timing specifications<sup>(3)</sup>

| Parameter  | Symbol   | Min           | Typ | Max           | Unit   | Notes  |
|--|----------|---------------|-----|---------------|--------|--------|
| Deterministic jitter tolerance                     | $J_D$    | —             | —   | 0.37          | UI p-p | (1)    |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | —             | —   | 0.55          | UI p-p | (1)    |
| Total jitter tolerance                             | $J_T$    | —             | —   | 0.65          | UI p-p | (1)(2) |
| Bit error ratio                                    | BER      | —             | —   | $10^{-12}$    | —      | —      |
| Unit Interval: 1.25 GBaud (SGMII)                  | UI       | 800 - 100 ppm | 800 | 800 + 100 ppm | ps     | (1)    |
| Unit Interval: 3.125 GBaud (2.5x SGMII)            | UI       | 320 - 100 ppm | 320 | 320 + 100 ppm | ps     | (1)    |

Notes: 1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 3-37. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 3-2.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 3-38.

### 3.19.10 HiGig/HiGig2 interface

This section describes the HiGig/HiGig2 clocking requirements and its DC and AC electrical characteristics.

## 3.19.10.1 HiGig/HiGig2 clocking requirements for SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

Only SerDes 1 (SD1\_REF\_CLK[1:2]\_P and SD1\_REF\_CLK[1:2]\_N) may be used for SerDes HiGig/HiGig2 configurations based on the RCW Configuration field SRDS\_PRTCL.

For more information on these specifications, see SerDes reference clocks.

## 3.19.10.2 HiGig/HiGig2 DC electrical characteristics

This section describes the DC electrical characteristics for HiGig/HiGig2.

### 3.19.10.2.1 HiGig/HiGig2 transmitter DC electrical characteristics

This table defines the HiGig/HiGig2 transmitter DC electrical characteristics.

**Table 3-104.** HiGig/HiGig2 transmitter DC electrical characteristics (XVDD = 1.35 V)<sup>(2)</sup>

| Parameter                             | Symbol           | Min   | Typical | Max  | Unit     | Notes                                 |
|---------------------------------------|------------------|-------|---------|------|----------|---------------------------------------|
| Output voltage                        | $V_O$            | -0.40 | –       | 2.30 | V        | (1)                                   |
| Differential output voltage           | $V_{DIFFPP}$     | 800   | 1000    | 1600 | mV p-p   | –                                     |
| DC Differential transmitter impedance | $Z_{TX-DIFF-DC}$ | 80    | 100     | 120  | $\Omega$ | Transmitter DC differential impedance |

Notes: 1. Absolute output voltage limit  
2. For recommended operating conditions, see [Table 3-2](#).

### 3.19.10.2.2 HiGig/HiGig2 receiver DC electrical characteristics

This table defines the HiGig/HiGig2 receiver DC electrical characteristics.

**Table 3-105.** HiGig/HiGig2 receiver DC electrical characteristics (SVDD = 1.0V)<sup>(2)</sup>

| Parameter                          | Symbol           | Min | Typical | Max  | Unit     | Notes                              |
|------------------------------------|------------------|-----|---------|------|----------|------------------------------------|
| Differential input voltage         | $V_{IN}$         | 200 | –       | 1600 | mV p-p   | (1)                                |
| DC Differential receiver impedance | $Z_{RX-DIFF-DC}$ | 80  | 100     | 120  | $\Omega$ | DC Differential receiver impedance |

Notes: 1. Measured at receiver  
2. For recommended operating conditions, see [Table 3-2](#).

## 3.19.10.3 HiGig/HiGig2 AC timing specifications

This section describes the AC timing specifications for HiGig/HiGig2.

### 3.19.10.3.1 HiGig/HiGig2 transmitter AC timing specifications

This table defines the HiGig/HiGig2 transmitter AC timing specifications. RefClk jitter is not included.

**Table 3-106.** HiGig/HiGig2 transmitter AC timing specifications<sup>(1)</sup>

| Parameter                                 | Symbol | Min              | Typical | Max              | Unit   |
|---|--------|------------------|---------|------------------|--------|
| Deterministic jitter                      | $J_D$  | —                | —       | 0.17             | UI p-p |
| Total jitter                              | $J_T$  | —                | —       | 0.35             | UI p-p |
| Unit Interval: 3.125 GBaud (HiGig/HiGig2) | UI     | 320 - 100 ppm    | 320     | 320 + 100 ppm    | ps     |
| Unit Interval: 3.75 GBaud (HiGig/HiGig2)  | UI     | 266.66 - 100 ppm | 266.66  | 266.66 + 100 ppm | ps     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.10.3.2 HiGig/HiGig2 receiver AC timing specifications

This table defines the HiGig/HiGig2 receiver AC timing specifications. RefClk jitter is not included.

**Table 3-107.** HiGig/HiGig2 receiver AC timing specifications<sup>(3)</sup>

| Parameter  | Symbol   | Min             | Typical | Max             | Unit   | Notes  |
|--|----------|-----------------|---------|-----------------|--------|--------|
| Deterministic jitter tolerance                     | $J_D$    | —               | —       | 0.37            | UI p-p | (1)    |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | —               | —       | 0.55            | UI p-p | (1)    |
| Total jitter tolerance                             | $J_T$    | —               | —       | 0.65            | UI p-p | (1)(2) |
| Unit Interval: 3.125 GBaud (HiGig/HiGig2)          | UI       | 320 - 100ppm    | 320     | 320 + 100ppm    | ps     | —      |
| Unit Interval: 3.75 GBaud (HiGig/HiGig2)           | UI       | 266.66 - 100ppm | 266.66  | 266.66 + 100ppm | ps     | —      |

Notes: 1. Measured at receiver

- Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 3-38](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
- For recommended operating conditions, see [Table 3-2](#).

## 3.19.11 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

### 3.19.11.1 XFI clocking requirements for SDn\_REF\_CLKn\_P and SDn\_REF\_CLKn\_N

Only SerDes 1 (SD1\_REF\_CLK[1:2]\_P and SD1\_REF\_CLK[1:2]\_N) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS\_PRTCL.

For more information on these specifications, see SerDes reference clocks.

#### 3.19.11.1 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

##### 3.19.11.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

**Table 3-108.** XFI transmitter DC electrical characteristics (XVDD = 1.35 V)<sup>(1)</sup>

| Parameter   | Symbol                            | Min | Typical | Max | Unit     | Notes |
|---|-----------------------------------|-----|---------|-----|----------|-------|
| Output differential voltage                       | $V_{TX-DIFF}$                     | 360 | –       | 770 | mV       | –     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-1.14\text{ dB}}$ | 0.6 | 1.1     | 1.6 | dB       | –     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-3.5\text{ dB}}$  | 3   | 3.5     | 4   | dB       | –     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-4.66\text{ dB}}$ | 4.1 | 4.6     | 5.1 | dB       | –     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-6.0\text{ dB}}$  | 5.5 | 6.0     | 6.5 | dB       | –     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-9.5\text{ dB}}$  | 9   | 9.5     | 10  | dB       | –     |
| Differential resistance                           | $T_{RD}$                          | 80  | 100     | 120 | $\Omega$ | –     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.11.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

**Table 3-109.** XFI receiver DC electrical characteristics (SVDD = 1.0V)<sup>(2)</sup>

| Parameter                  | Symbol        | Min | Typical | Max  | Unit     | Notes |
|----------------------------|---------------|-----|---------|------|----------|-------|
| Input differential voltage | $V_{RX-DIFF}$ | 110 | –       | 1050 | mV       | (1)   |
| Differential resistance    | $R_{RD}$      | 80  | 100     | 120  | $\Omega$ | –     |

Notes: 1. Measured at receiver

2. For recommended operating conditions, see [Table 3-2](#)

### 3.19.11.2 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

#### 3.19.11.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

**Table 3-110.** XFI transmitter AC timing specifications<sup>(1)</sup>

| Parameter             | Symbol     | Min              | Typical | Max              | Unit   |
|-----------------------|------------|------------------|---------|------------------|--------|
| Transmitter baud rate | $T_{BAUD}$ | 10.3125 – 100ppm | 10.3125 | 10.3125 + 100ppm | Gb/s   |
| Unit Interval         | UI         | –                | 96.96   | –                | ps     |
| Deterministic jitter  | $D_J$      | –                | –       | 0.15             | UI p-p |
| Total jitter          | $T_J$      | –                | –       | 0.30             | UI p-p |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

#### 3.19.11.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

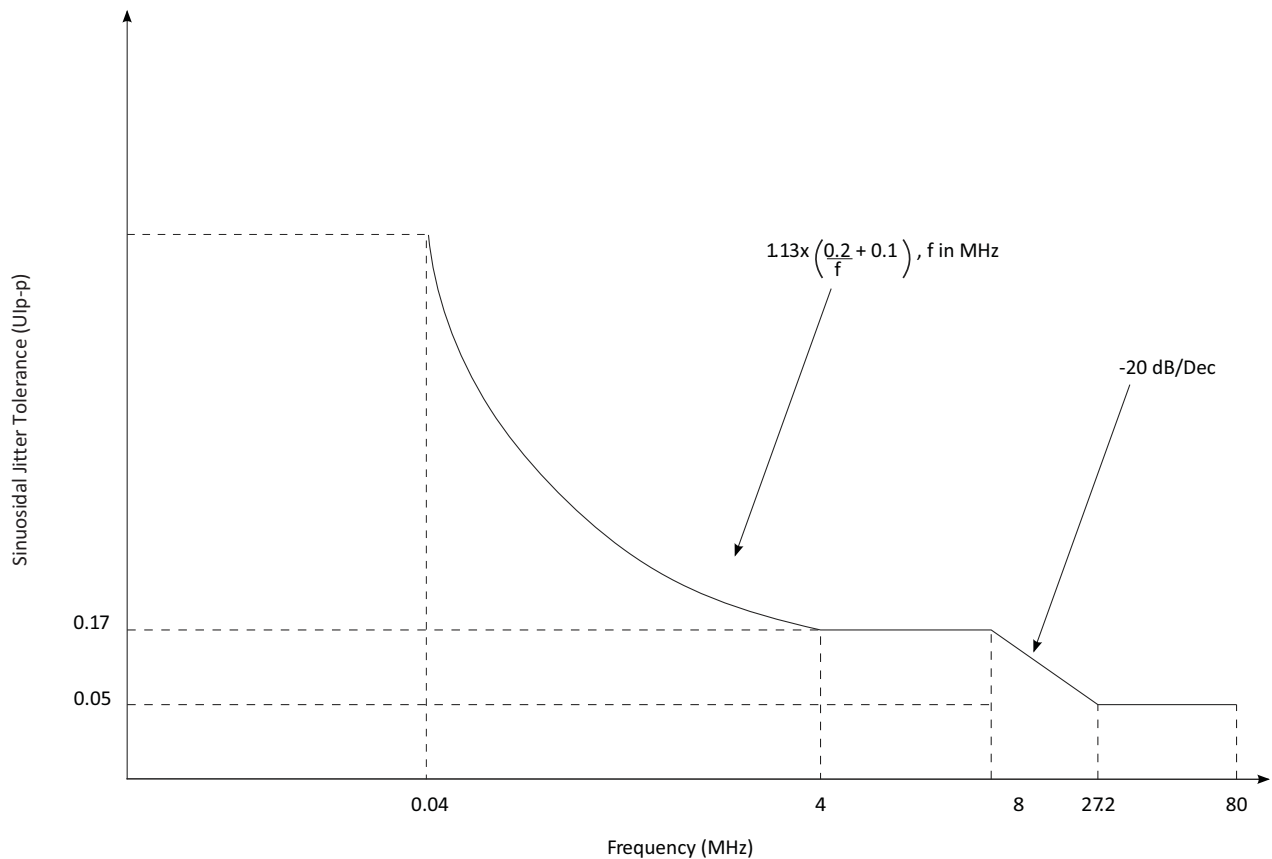
**Table 3-111.** XFI receiver AC timing specifications<sup>(3)</sup>

| Parameter              | Symbol               | Min              | Typical | Max              | Unit   | Notes  |
|------------------------|----------------------|------------------|---------|------------------|--------|--------|
| Receiver baud rate     | $R_{\text{BAUD}}$    | 10.3125 - 100ppm | 10.3125 | 10.3125 + 100ppm | Gb/s   | –      |
| Unit Interval          | UI                   | –                | 96.96   | –                | ps     | –      |
| Total non-EQJ jitter   | $T_{\text{NON-EQJ}}$ | –                | –       | 0.45             | UI p-p | (1)    |
| Total jitter tolerance | $T_J$                | –                | –       | 0.65             | UI p-p | (1)(2) |

- Notes:
1. The total jitter ( $T_J$ ) consists of Random Jitter ( $R_J$ ), Duty Cycle Distortion (DCD), Periodic Jitter ( $P_J$ ), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter ( $R_J$ ), and periodic jitter ( $P_J$ ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ =  $T_J$  - ISI =  $R_J$  + DCD +  $P_J$ .
  2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.
  3. For recommended operating conditions, see [Table 3-2](#).

This figure shows the sinusoidal jitter tolerance of XFI receiver.

**Figure 3-43.** XFI host receiver input sinusoidal jitter tolerance





## 3.19.12 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

### 3.19.12.1 10GBase-KR clocking requirements for SDn\_REF\_CLKn and SDn\_REF\_CLKn\_B

Only SerDes 1 (SD1\_REF\_CLK[1:2]\_Pand SD1\_REF\_CLK[1:2]\_N) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS\_PRTCL.

For more information on these specifications, see SerDes reference clocks.

### 3.19.12.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

#### 3.19.12.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

**Table 3-112.** 10GBaseKR transmitter DC electrical characteristics (XVDD = 1.35V or 1.5V)<sup>(1)</sup>

| Parameter   | Symbol                    | Min | Typical | Max  | Unit     | Notes |
|---|---------------------------|-----|---------|------|----------|-------|
| Output differential voltage                       | $V_{TX-DIFF}$             | 800 | —       | 1200 | mV       | —     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-1.14dB}$ | 0.6 | 1.1     | 1.6  | dB       | —     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-3.5dB}$  | 3   | 3.5     | 4    | dB       | —     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-4.66dB}$ | 4.1 | 4.6     | 5.1  | dB       | —     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-6.0dB}$  | 5.5 | 6.0     | 6.5  | dB       | —     |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE- RATIO-9.5dB}$  | 9   | 9.5     | 10   | dB       | —     |
| Differential resistance                           | $T_{RD}$                  | 80  | 100     | 120  | $\Omega$ | —     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

#### 3.19.12.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

**Table 3-113.** 10GBase-KR receiver DC electrical characteristics (XVDD = 1.35V or 1.5V)<sup>(1)</sup>

| Parameter                  | Symbol        | Min | Typical | Max  | Unit | Notes |
|----------------------------|---------------|-----|---------|------|------|-------|
| Input differential voltage | $V_{RX-DIFF}$ | —   | —       | 1200 | mV   | —     |
| Differential resistance    | $R_{RD}$      | 80  | —       | 120  | ?    | —     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

### 3.19.12.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

#### 3.19.12.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

**Table 3-114.** 10GBase-KR transmitter AC timing specifications<sup>(1)</sup>

| Parameter  | Symbol        | Min               | Typical | Max               | Unit   |
|--|---------------|-------------------|---------|-------------------|--------|
| Transmitter baud rate                              | $T_{BAUD}$    | 10.3125 – 100 ppm | 10.3125 | 10.3125 + 100 ppm | Gb/s   |
| Uncorrelated high probability jitter/Random jitter | $U_{HPJ}/R_J$ | –                 | –       | 0.15              | UI p-p |
| Deterministic jitter                               | $D_J$         | –                 | –       | 0.15              | UI p-p |
| Total jitter                                       | $T_J$         | –                 | –       | 0.30              | UI p-p |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

#### 3.19.12.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

**Table 3-115.** 10GBase-KR receiver AC timing specifications<sup>(2)</sup>

| Parameter                  | Symbol      | Min               | Typical | Max                     | Unit   | Notes          |
|----------------------------|-------------|-------------------|---------|-------------------------|--------|----------------|
| Receiver baud rate         | $R_{BAUD}$  | 10.3125 – 100 ppm | 10.3125 | 10.3125 + 100 ppm       | Gb/s   | –              |
| Random jitter              | $R_J$       | –                 | –       | 0.130                   | UI p-p | –              |
| Sinusoidal jitter, maximum | $S_{J-max}$ | –                 | –       | 0.115                   | UI p-p | –              |
| Duty cycle distortion      | $D_{CD}$    | –                 | –       | 0.035                   | UI p-p | –              |
| Total jitter               | $T_J$       | –                 | –       | See Note <sup>(1)</sup> | UI p-p | <sup>(1)</sup> |

Notes: 1. The total jitter ( $T_J$ ) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A.

2. For recommended operating conditions, see [Table 3-2](#).

### 3.19.13 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC- coupled operation is supported.

#### 3.19.13.1 1000Base-KX DC electrical characteristics

##### 3.19.13.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SDn\_TXn\_P and SDn\_TXn\_N).

**Table 3-116.** 1000Base-KX Transmitter DC Specifications

| Parameter                   | Symbols          | Min | Typical | Max  | Units | Notes          |
|-----------------------------|------------------|-----|---------|------|-------|----------------|
| Output differential voltage | $V_{TX-DIFFP-P}$ | 800 | –       | 1600 | mV    | <sup>(1)</sup> |
| Differential resistance     | $T_{RD}$         | 80  | 100     | 120  | ohm   | –              |

Notes: 1. SRDSxLNmTECRO[AMP\_RED]=00\_0000.

2. For recommended operating conditions, see [Table 3-2](#).

## 3.19.13.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

**Table 3-117.** 1000Base-KX Receiver DC Specifications

| Parameter                  | Symbols          | Min | Typical | Max  | Units | Notes |
|----------------------------|------------------|-----|---------|------|-------|-------|
| Input differential voltage | $V_{RX-DIFFp-p}$ | —   | —       | 1600 | mV    | (1)   |
| Differential resistance    | $T_{RDIN}$       | 80  | -       | 120  | ohm   | —     |

Note: 1. For recommended operating conditions, see [Table 3-2](#).

## 3.19.13.2 1000Base-KX AC electrical characteristics

### 3.19.13.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

**Table 3-118.** 1000Base-KX Transmitter AC Specifications

| Parameter  | Symbols          | Min         | Typical | Max         | Units  | Notes |
|--|------------------|-------------|---------|-------------|--------|-------|
| Baud Rate  | $T_{BAUD}$       | 1.25-100ppm | 1.25    | 1.25+100ppm | Gb/s   | —     |
| Uncorrelated High Probability Jitter/Random Jitter | $T_{UHPJ}T_{RJ}$ | —           | —       | 0.15        | UI p-p | —     |
| Deterministic Jitter                               | $T_{DJ}$         | —           | —       | 0.10        | UI p-p | —     |
| Total Jitter                                       | $T_{TJ}$         | —           | —       | 0.25        | UI p-p | (1)   |

Notes: 1. Total jitter is specified at a BER of  $10^{-12}$ .

2. For recommended operating conditions, see [Table 3-2](#).

### 3.19.13.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

**Table 3-119.** 1000Base-KX Receiver AC Specifications

| Parameter                  | Symbols      | Min         | Typical | Max          | Units  | Notes |
|----------------------------|--------------|-------------|---------|--------------|--------|-------|
| Receiver Baud Rate         | $R_{BAUD}$   | 1.25-100ppm | 1.25    | 1.25+100ppm  | Gb/s   | —     |
| Random Jitter              | $R_{RJ}$     | —           | —       | 0.15         | UI p-p | (1)   |
| Sinusoidal Jitter, maximum | $R_{SJ-max}$ | —           | —       | 0.10         | UI p-p | (2)   |
| Total Jitter               | $R_{TJ}$     | —           | —       | See Note (3) | UI p-p | (2)   |

Notes: 1. Random jitter is specified at a BER of  $10^{-12}$ .

2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.

3. Per IEEE 802.3ap-clause 70.

4. The AC specifications do not include Refclk jitter.

5. For recommended operating conditions, see [Table 3-2](#).

## 4. HARDWARE DESIGN CONSIDERATIONS

### 4.1 System clocking

This section describes the PLL configuration of the chip.

#### 4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are two selectable core cluster PLLs which generate a clock for each core cluster from the externally supplied SYSCLK input.
  - Core cluster 1 (cores 0-3) can select from cluster group A PLL 1 or 2 (CGA1 or 2 PLL)
  - The frequency ratio between each of the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Core cluster to SYSCLK PLL ratio. The frequency for each core cluster is selected using the configuration bits as described in [Table 4-5](#).
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- Cluster group A generates an asynchronous clock for eSDHC SDR mode from cluster group A PLL1 or cluster group A PLL 2. Described in eSDHC SDR mode clock select.
- Cluster group A generates an asynchronous clock for FMan from the platform PLL, cluster group A PLL1 or cluster group A PLL 2. Described in Frame Manager (FM) clock select.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in DDR controller PLL ratios.
- Each of the two SerDes blocks has 2 PLLs which generate a core clock from their respective externally supplied SDn\_REF\_CLKn\_P/SDn\_REF\_CLKn\_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.

#### 4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

**Table 4-1.** Processor, platform, and memory clocking specifications

| Characteristic                   | Maximum processor core frequency |      |                         |      |                         |      | Unit | Notes     |
|----------------------------------|----------------------------------|------|-------------------------|------|-------------------------|------|------|-----------|
|                                  | 1200 MHz                         |      | 1533 MHz                |      | 1800 MHz                |      |      |           |
|                                  | Min                              | Max  | Min                     | Max  | Min                     | Max  |      |           |
| Core cluster group PLL frequency | 1000                             | 1200 | 1000                    | 1533 | 1000                    | 1800 | MHz  | (1)(2)    |
| Core cluster frequency           | 250                              | 1200 | 250                     | 1533 | 250                     | 1800 | MHz  | (2)       |
| Platform clock frequency         | 400                              | 533  | 400                     | 600  | 400                     | 600  | MHz  | (1)(7)    |
| Memory bus clock frequency       | 533                              | 800  | 533                     | 933  | 533                     | 1066 | MHz  | (1)(3)(4) |
| IFC clock frequency              | –                                | 100  | –                       | 100  | –                       | 100  | MHz  | (5)       |
| FMan                             | see note <sup>(6)</sup>          | 600  | see note <sup>(6)</sup> | 700  | see note <sup>(6)</sup> | 700  | MHz  | (6)       |

Notes: 1. **Caution:** The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The core cluster can run at cluster group PLL/1, PLL/2, or PLL/4. For the PLL/1 case, the minimum frequency is 1000 MHz. With a minimum cluster group PLL frequency of 1000 MHz, this results in a minimum allowable core cluster frequency of 250 MHz for PLL/4.
3. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3/3L memory bus clock frequency is limited to min = 533 MHz.
4. The memory bus clock speed is dictated by its own PLL.
5. The integrated flash controller (IFC) clock speed on IFC\_CLK[0:1] is determined by half of the platform clock divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.
6. The FMan minimum frequency is 132 MHz for SGMII (1.25G), 330 MHz for SGMII (2.5G), 300 MHz for XAUI, 391 MHz for HiGig, 469 MHz for HiGig2, and 359 MHz for XFI.
7. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

## 4.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

**Table 4-2.** Memory bus clocking specifications

| Characteristic             | Min | Max  | Unit | Notes     |
|----------------------------|-----|------|------|-----------|
| Memory bus clock frequency | 533 | 1066 | MHz  | (1)(2)(3) |

- Notes:
1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings.
  2. The memory bus clock refers to the chip's memory controllers' Dn\_MCK[0:3] and Dn\_MCK[0:3]\_B output clocks, running at half of the DDR data rate.
  3. The memory bus clock speed is dictated by its own PLL. See [DDR controller PLL ratios](#).

### 4.1.3 SerDes PLL ratio

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SDn\_REF\_CLKn\_P/SDn\_REF\_CLKn\_N inputs is determined by a set of RCW Configuration fields-SRDS\_PRTCL\_Sn, SRDS\_PLL\_REF\_CLK\_SEL\_Sn, and SRDS\_DIV\_\*\_Sn-as shown in this table.

**Table 4-3.** Valid SerDes RCW encodings and reference clocks

| SerDes protocol (given lane)                        | Valid reference clock frequency | Legal setting for SRDS_PRTCL_Sn | Legal setting for SRDS_PLL_REF_CLK_SEL_Sn | Legal setting for SRDS_DIV_*_Sn | Notes |
|---|---------------------------------|---------------------------------|---|---------------------------------|-------|
| High-speed serial and debug interfaces              |                                 |                                 |   |                                 |       |
| PCI Express 2.5 GT/s<br>(doesn't negotiate upwards) | 100 MHz                         | Any PCIe                        | 0b0: 100 MHz                              | 2b10: 2.5 G                     | (1)   |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | (1)   |
| PCI Express 5 GT/s<br>(can negotiate up to 5 GT/s)  | 100 MHz                         | Any PCIe                        | 0b0: 100 MHz                              | 2b01: 5.0 G                     | (1)   |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | (1)   |
| PCI Express 8 GT/s<br>(can negotiate up to 8 GT/s)  | 100 MHz                         | Any PCIe                        | 0b0: 100 MHz                              | 2b00: 8.0 G                     | (1)   |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | (1)   |
| Serial RapidIO 2.5 GBaud                            | 100 MHz                         | SRIO @ 2.5/5 GBaud              | 0b0: 100 MHz                              | 0b1: 2.5 G                      | —     |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | —     |
| Serial RapidIO 3.125 GBaud                          | 125 MHz                         | SRIO @ 3.125 GBaud              | 0b0: 125 MHz                              | Don't care                      | —     |
|   | 156.25 MHz                      |                                 | 0b1: 156.25 MHz                           |                                 | —     |
| Serial RapidIO 5 GBaud                              | 100 MHz                         | SRIO @ 2.5/5 GBaud              | 0b0: 100 MHz                              | 0b0: 5.0 G                      | —     |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              | —                               |       |
| SATA (1.5 or 3 Gbps)                                | 100 MHz                         | Any SATA                        | 0b0: 100 MHz                              | Don't care                      | (2)   |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 |       |
| Debug (2.5 GBaud)                                   | 100 MHz                         | Aurora @ 2.5/5 GBaud            | 0b0: 100 MHz                              | 0b1: 2.5 G                      | —     |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | —     |
| Debug (5 GBaud)                                     | 100 MHz                         | Aurora @ 2.5/5 GBaud            | 0b0: 100 MHz                              | 0b0: 5.0 G                      | —     |
|   | 125 MHz                         |                                 | 0b1: 125 MHz                              |                                 | —     |
| Networking interfaces                               |                                 |                                 |   |                                 |       |
| SGMII (1.25 GBaud)                                  | 100 MHz                         | SGMII @ 1.25 GBaud              | 0b0: 100 MHz                              | Don't care                      | —     |
|   | 125 MHz                         | 1000Base-KX @ 1.25 GBaud        | 0b1: 125 MHz                              |                                 | —     |
| 2.5x SGMII (3.125 GBaud)                            | 125 MHz                         | SGMII @ 3.125 GBaud             | 0b0: 125 MHz                              | Don't care                      | —     |
|   | 156.25 MHz                      |                                 | 0b1: 156.25 MHz                           |                                 | —     |
| XAUI (3.125 GBaud)                                  | 125 MHz                         | XAUI @ 3.125 GBaud              | 0b0: 125 MHz                              | Don't care                      | —     |
|   | 156.25 MHz                      |                                 | 0b1: 156.25 MHz                           |                                 | —     |
| HiGig or HiGig2 (3.125 GBaud)                       | 125 MHz                         | HiGig @ 3.125 GBaud             | 0b0: 125 MHz                              | Don't care                      | —     |
|   | 156.25 MHz                      |                                 | 0b1: 156.25 MHz                           |                                 | —     |
| HiGig or HiGig2 (3.75 GBaud)                        | 125 MHz                         | HiGig @ 3.75 GBaud              | 0b0: 125 MHz                              | Don't care                      | —     |
|   | 156.25 MHz                      |                                 | 0b1: 156.25 MHz                           |                                 | —     |
| XFI (10.3125 GBaud)                                 | 156.25 MHz                      | XFI @ 10.3125 GBaud             | 0b0: 156.25 MHz                           | Don't care                      | —     |
| 10GBase-KR (10.3125GBaud)                           | 156.25 MHz                      | 10GBase-KR @ 10.3125 GBaud      | 0b0: 156.25 MHz                           | Don't care                      | —     |

- Notes:
1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interfaces such as sRIO, SATA, or debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.
  2. SerDes lanes configured as SATA initially operate at 3.0 Gbps. 1.5 Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.

## 4.1.4 Frequency options

This section discusses interface frequency options.

### 4.1.4.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

**Table 4-4.** SYSCLK and platform frequency options

| Platform: SYSCLK ratio | SYSCLK (MHz)                            |        |        |
|------------------------|---|--------|--------|
|                        | 66.67                                   | 100.00 | 133.33 |
|                        | Platform frequency (MHz) <sup>(1)</sup> |        |        |
| 3:1                    |   |        | 400    |
| 4:1                    |   | 400    | 533    |
| 5:1                    |   | 500    |        |
| 6:1                    | 400                                     | 600    |        |
| 7:1                    | 466                                     |        |        |
| 8:1                    | 533                                     |        |        |
| 9:1                    | 600                                     |        |        |

Note: 1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).

### 4.1.4.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

**Figure 4-1.** Gen 1 PEX minimum platform frequency

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{16}$$

**Figure 4-2.** Gen 2 PEX minimum platform frequency

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{8}$$

**Figure 4-3.** Gen 3 PEX minimum platform frequency

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{4}$$

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use. For instance, if two x4 PCIe Gen3 ports are in use, 527 MHz platform frequency is needed to support by using Gen 3 equation ( $527 \times 4 / 4$ , not  $527 \times 4 \times 2 / 4$ ).

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to 525 MHz.

## 4.2 Power supply design

### 4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the  $V_{ID}$  efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. The  $V_{DD}$  supply should be separated from the Serdes 1.0V supply  $SnV_{DD}$ . It is required in order to control the  $V_{DD}$  supply only.

#### NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating  $V_{DD}$  at initial start-up of 1.025V. It is highly recommended to select a regulator with a  $V_{out}$  range of at least 0.9V to 1.1V, with a resolution of 12.5mV or better, when implementing a  $V_{ID}$  solution.

The table below lists the valid  $V_{ID}$  efuse values that will be programmed at the factory for this chip.

**Table 4-5.** Fuse Status Register (DCFG\_CCSR\_FUSESR)

| Binary value of DA_V / DA_ALT_V | $V_{DD}$ voltage |
|---------------------------------|------------------|
| 00000                           | 1.0250 V         |
| 00001                           | 0.9875 V         |
| 00010                           | 0.9750 V         |
| 10000                           | 1.0000 V         |
| 10001                           | 1.0125 V         |
| 10010                           | 1.0250 V         |

For additional information on  $V_{ID}$ , please refer to the chip reference manual.

#### 4.2.1.1 Options for system design

There are several widely-accepted options available to the system designer for obtaining the benefits of a  $V_{ID}$  solution. The most common option is to use the  $V_{ID}$  solution to drive a system's controllable voltage-regulators through a sideband interface such as a simple parallel bus or PMBus interface. PMBus is similar to I2C but with extensions to improve robustness and address shortcomings of I2C; the PMBus specification can be found at [www.pmbus.org](http://www.pmbus.org). The simple parallel bus is supported by the chip through GPIO pins and the PMBus interface is supported by an I<sup>2</sup>C interface. Other  $V_{ID}$  solutions may be to access an FPGA/ASIC or separate power management chip through the IFC, SPI, or other chip-specific interface, where the other device then manages the voltage regulator. The method chosen for implementing the chip-specific voltage in the system is decided by the user.



## 4.2.1.1.1 Example 1: Regulators supporting parallel bus configuration

In this example, a user builds a  $V_{ID}$  solution using controllable regulators with a parallel bus. In this implementation, the user chooses to utilize any subset of the available GPIO pins on the chip except those noted below.

### NOTE

GPIO pins that are muxed on an interface used by the application for loading RCW information are not available for  $V_{ID}$  use.

It is recommended that all GPIO pins used for  $V_{ID}$  are located in the same 32-bit GPIO IP block so that all bits can be accessed with a single read or write.

1. The GPIO pins are released to high-impedance at POR. Because GPIO pins default to being inputs, they do not begin automatically driving after POR, and only work as outputs under software control.
2. The board is responsible for a default voltage regulator setting that is "safe" for the system to boot. To achieve this, the user puts pull-up and/or pull-down resistors on the GPIO pins as needed for that specific system. For the case where the regulator's interface operates at a different voltage than  $OV_{DD}$ , the chip's GPIO module can be operated in an open drain configuration.
3. There is no direct connection between the Fuse Status Register (FUSESR) and the chip's pins. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software determines the proper value for the parallel interface and writes it to the GPIO block data (GPDAT) register. It then changes the GPIO direction (GPDIR) register from input to output to drive the new value on the device pins, thus overriding the board configuration default value. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
4. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task if desired.

## 4.2.1.1.2 Example 2: Regulators supporting PMBus configuration

In this example, a user builds a  $V_{ID}$  solution using controllable regulators with a PMBus interface. For the case where the regulator's interface operates at a different voltage than DVDD, the chip's I<sup>2</sup>C module can be operated in an open-drain configuration.

In this implementation, the user chooses to utilize any I<sup>2</sup>C interface available on the chip. These regulators have a means for setting a safe, default, operating value either through strapping pins or through a default, non-volatile store.

### NOTE

If I<sup>2</sup>C1 controller is selected, it is important that its calling address is different than the 7-bit value of 0x50h used by the pre-boot loader (PBL) for RCW and pre-boot initialization.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR register and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the I<sup>2</sup>C interface connected to the regulator's PMBus interface. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

#### 4.2.1.1.3 Example 3: Regulators supporting FPGA/ASIC or separate power management device configuration

In this example, a user builds a  $V_{ID}$  solution using controllable regulators that are managed by a FPGA/ASIC or a separate power-management device. In this implementation, the user chooses to utilize the IFC, eSPI or any other available chip interface to connect to the power-management device.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the IFC, eSPI, or any other interface that is used to connect to the FPGA/ASIC or separate power-management device that manages the regulator. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

### 4.2.2 Core and platform supply voltage filtering

The  $V_{DD}$  supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, TELEDYNE e2v recommends that these bulk capacitors should be chosen to maintain the positive transient power surges to less than  $V_{ID} + 50$  mV (negative transient undershoot should comply with specification of  $V_{ID} - 30$  mV) for current steps of up to 10 A with a slew rate of 12 A/us.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see [Decoupling recommendations](#) for further decoupling recommendations.

### 4.2.3 PLL power supply filtering

Each of the PLLs described in [System clocking](#) is provided with power through independent power supply pins ( $AV_{DD\_PLAT}$ ,  $AV_{DD\_CGAn}$ ,  $AV_{DD\_CGBn}$  and  $AV_{DD\_Dn}$  and  $AV_{DD\_SDn\_PLLn}$ ).  $AV_{DD\_PLAT}$ ,  $AV_{DD\_CGAn}$ ,  $AV_{DD\_CGBn}$  and  $AV_{DD\_Dn}$  voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme.  $AV_{DD\_SDn\_PLLn}$  voltages must be derived directly from the  $XnV_{DD}$  source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in [Figure 4-4](#), one for each of the  $AV_{DD}$  pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific  $AV_{DD}$  pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit. Where:

- $R = 5\Omega \pm 5\%$
- $C1 = 10 \mu F \pm 10\%$ , 0603, X5R, with  $ESL \leq 0.5$  nH
- $C2 = 1.0 \mu F \pm 10\%$ , 0402, X5R, with  $ESL \leq 0.5$  nH

## NOTE

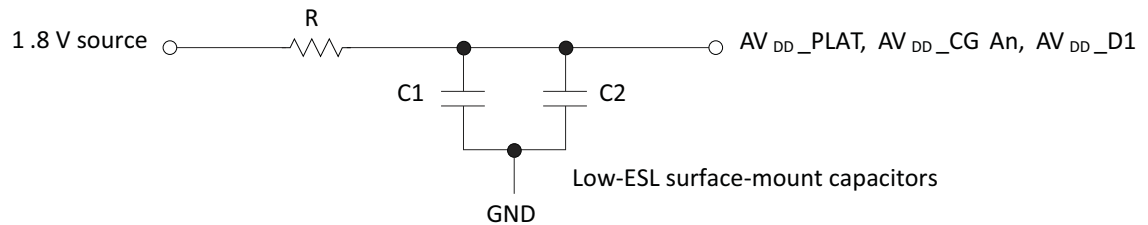
A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R,  $ESL \leq 0.5$  nH).

## NOTE

Voltage for  $AV_{DD}$  is defined at the input of the PLL supply filter and not the pin of  $AV_{DD}$ .

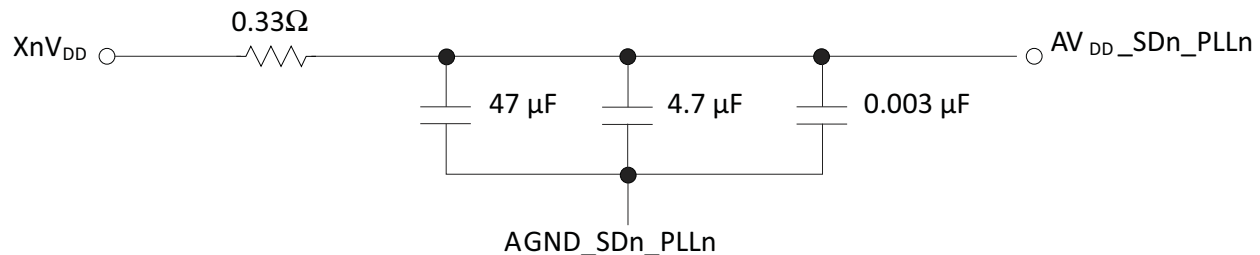
Low-ESL surface-mount capacitors

**Figure 4-4.** PLL power supply filter circuit



The  $AV_{DD\_SDn\_PLLn}$  signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following [Figure 4-5](#). For maximum effectiveness, the filter circuit is placed as closely as possible to the  $AV_{DD\_SDn\_PLLn}$  balls to ensure it filters out as much noise as possible. The ground connection should be near the  $AV_{DD\_SDn\_PLLn}$  balls. The 0.003- $\mu$ F capacitors closest to the balls, followed by a 4.7- $\mu$ F and 47- $\mu$ F capacitor, and finally the 0.33 $\Omega$  resistor to the board supply plane. The capacitors are connected from  $AV_{DD\_SDn\_PLLn}$  to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

**Figure 4-5.** SerDes PLL power supply filter circuit



Note the following:

- $AV_{DD\_SDn\_PLLn}$  should be a filtered version of  $XnV_{DD}$ .
- Signals on the SerDes interface are fed from the  $XnV_{DD}$  power plane.
- Voltage for  $AV_{DD\_SDn\_PLLn}$  is defined at the PLL supply filter and not the pin of  $AV_{DD\_SDn\_PLLn}$ .
- A 47- $\mu$ F 0805 XR5 or XR7, 4.7- $\mu$ F 0603, and 0.003- $\mu$ F 0402 capacitor are recommended. The size and material type are important. A 0.33 $\Omega \pm 1\%$  resistor is recommended.
- There needs to be dedicated analog ground,  $AGND\_SDn\_PLLn$  for each  $AV_{DD\_SDn\_PLLn}$  pin up to the physical local of the filters themselves.

#### 4.2.4 SnVDD power supply filtering

For initial system bring-up, the linear regulator option is highly recommended.

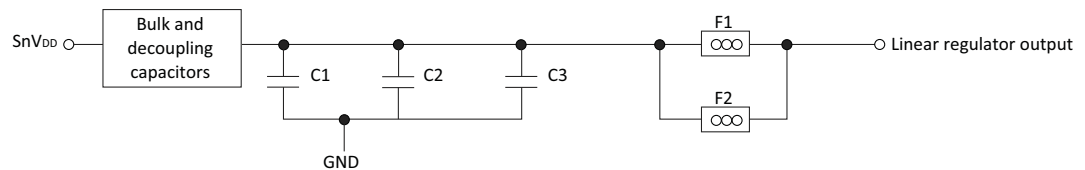
An example solution for  $SnV_{DD}$  filtering, where  $SnV_{DD}$  is sourced from a linear regulator, is illustrated in Figure 4-6. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- $C1 = 0.003 \mu F \pm 10\%$ , X5R, with  $ESL \leq 0.5 \text{ nH}$
- $C2$  and  $C3 = 2.2 \mu F \pm 10\%$ , X5R, with  $ESL \leq 0.5 \text{ nH}$
- $F1$  and  $F2 = 120\Omega$  at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Note the following:

**Figure 4-6.**  $SnV_{DD}$  power supply filter circuit



- Please refer to [Power-on ramp rate](#), for maximum  $SnV_{DD}$  power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500 MHz is the noise goal.

#### 4.2.5 XnVDD power supply filtering

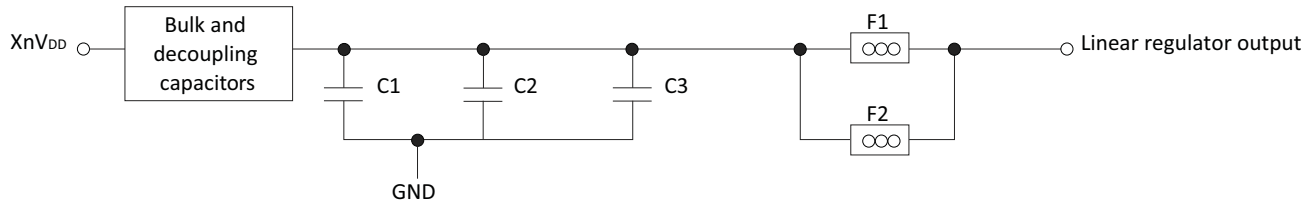
$XnV_{DD}$  may be supplied by a linear regulator or sourced by a filtered  $G1V_{DD}$ . Systems may design in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended.

An example solution for  $XnV_{DD}$  filtering, where  $XnV_{DD}$  is sourced from a linear regulator, is illustrated in Figure 4-7. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- $C1 = 0.003 \mu F \pm 10\%$ , X5R, with  $ESL \leq 0.5 \text{ nH}$
- $C2$  and  $C3 = 2.2 \mu F \pm 10\%$ , X5R, with  $ESL \leq 0.5 \text{ nH}$
- $F1$  and  $F2 = 120\Omega$  at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

**Figure 4-7.**  $XnV_{DD}$  power supply filter circuit



Note the following:

- See [Section 3.5 "Power-on ramp rate" on page 52](#) for maximum  $XnV_{DD}$  power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10 mVp-p, 50 kHz - 500 MHz is the noise goal.

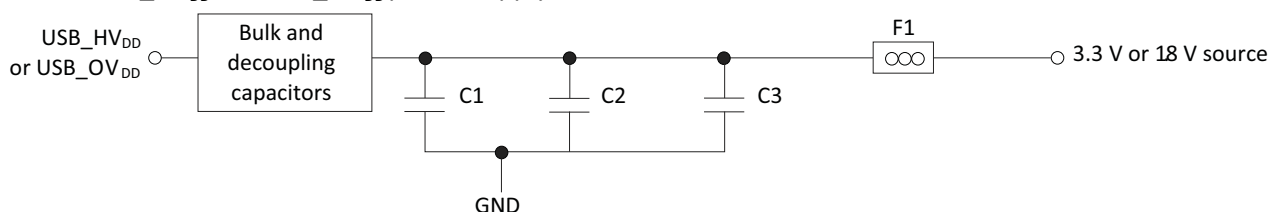
## 4.2.6 USB\_HV<sub>DD</sub> and USB\_OV<sub>DD</sub> power supply filtering

USB\_HV<sub>DD</sub> and USB\_OV<sub>DD</sub> must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB\_HV<sub>DD</sub> and USB\_OV<sub>DD</sub> filtering, where USB\_HV<sub>DD</sub> and USB\_OV<sub>DD</sub> are sourced from a 3.3 V and 1.8 V voltage source, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003  $\mu\text{F} \pm 10\%$ , X5R, with ESL  $\leq 0.5$  nH
- C2 and C3 = 2.2  $\mu\text{F} \pm 10\%$ , X5R, with ESL  $\leq 0.5$  nH
- F1 = 120 $\Omega$  at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

**Figure 4-8.** USB\_HV<sub>DD</sub> and USB\_OV<sub>DD</sub> power supply filter circuit



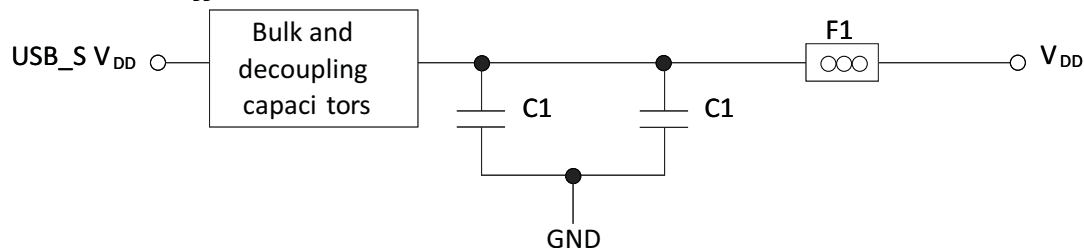
## 4.2.7 USB\_SV<sub>DD</sub> power supply filtering

USB\_SV<sub>DD</sub> must be sourced by a filtered V<sub>DD</sub> using a star connection. An example solution for USB\_SV<sub>DD</sub> filtering, where USB\_SV<sub>DD</sub> is sourced from V<sub>DD</sub>, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 2.2  $\mu\text{F} \pm 20\%$ , X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
- F1 = 120 $\Omega$  at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

**Figure 4-9.** USB\_SV<sub>DD</sub> power supply filter circuit



### 4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each  $V_{DD}$ ,  $OV_{DD}$ ,  $DV_{DD}$ ,  $G1V_{DD}$ , and  $LV_{DD}$  pin of the device. These decoupling capacitors should receive their power from separate  $V_{DD}$ ,  $OV_{DD}$ ,  $DV_{DD}$ ,  $G1V_{DD}$ ,  $LV_{DD}$ , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1  $\mu\text{F}$ . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in [Core and platform supply voltage filtering](#), it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the  $V_{DD}$  and other planes (for example,  $OV_{DD}$ ,  $DV_{DD}$ ,  $G1V_{DD}$ , and  $LV_{DD}$ ), to enable quick recharging of the smaller chip capacitors.

### 4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power ( $SnV_{DD}$  and  $XnV_{DD}$ ) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

#### NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least  $1 \times 0.1\text{-}\mu\text{F}$  SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor for example a 10- $\mu\text{F}$ , low ESR SMT tantalum or ceramic and a higher bulk capacitor for example a 100  $\mu\text{F}$  - 300- $\mu\text{F}$  low ESR SMT tantalum or ceramic capacitor.

### 4.5 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to  $V_{DD}$ ,  $OV_{DD}$ ,  $DV_{DD}$ ,  $G1V_{DD}$ , and  $LV_{DD}$  as required. All unused active high inputs should be connected to GND. All NC (no- connect) signals must remain unconnected. Power and ground connections must be made to all external  $V_{DD}$ ,  $OV_{DD}$ ,  $DV_{DD}$ ,  $G1V_{DD}$ ,  $LV_{DD}$  and GND pins of the device.
- The TEST\_SEL\_B pin must be pulled high.
- The chip has temperature diodes on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as on Semiconductor, NCT72). Even if a temperature diode monitoring device is not utilized on production systems, being able to access these pins for debug or problem analysis can be valuable. Therefore, it is suggested to connect these pins to test points connected to ground through low value resistors, which can be removed if a temperature monitoring device is ever to be connected. The chip temperature diode specifications are as follows:
  - Operating range: 10 - 230  $\mu\text{A}$
  - Ideality factor over 13.5 - 220  $\mu\text{A}$ : Temperature range 25°C – 105°C  $n = 1.006833 \pm 0.008$

## 4.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 4-11](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST\_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST\_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST\_B during the power-on reset flow. Simply tying TRST\_B to PORESET\_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET\_B or TRST\_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 4-11](#) allows the COP port to independently assert PORESET\_B or TRST\_B, while ensuring that the target can drive PORESET\_B as well.

The COP interface has a standard header, shown in [Figure 4-10](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

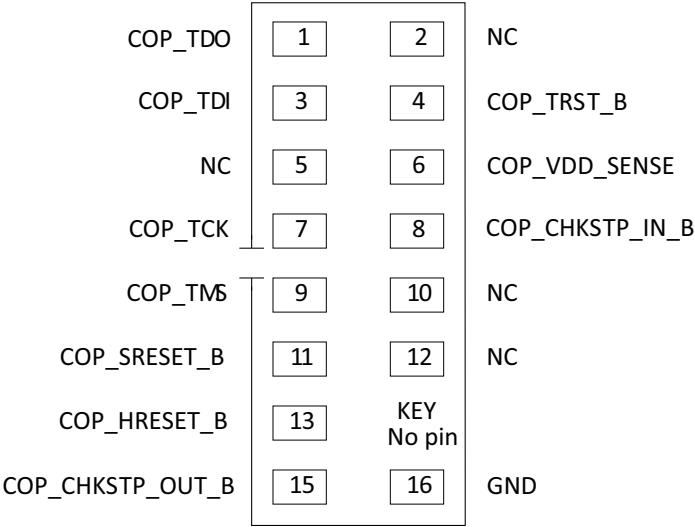
There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 4-10](#) is common to all known emulators.

### 4.5.1.1 Termination of unused signals

If the JTAG interface and COP header will not be used, TELEDYNE e2v recommends the following connections:

- TRST\_B should be tied to PORESET\_B through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal (PORESET\_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. TELEDYNE e2v recommends that the COP header be designed into the system as shown in [Figure 4-11](#). If this is not possible, the isolation resistor will allow future access to TRST\_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

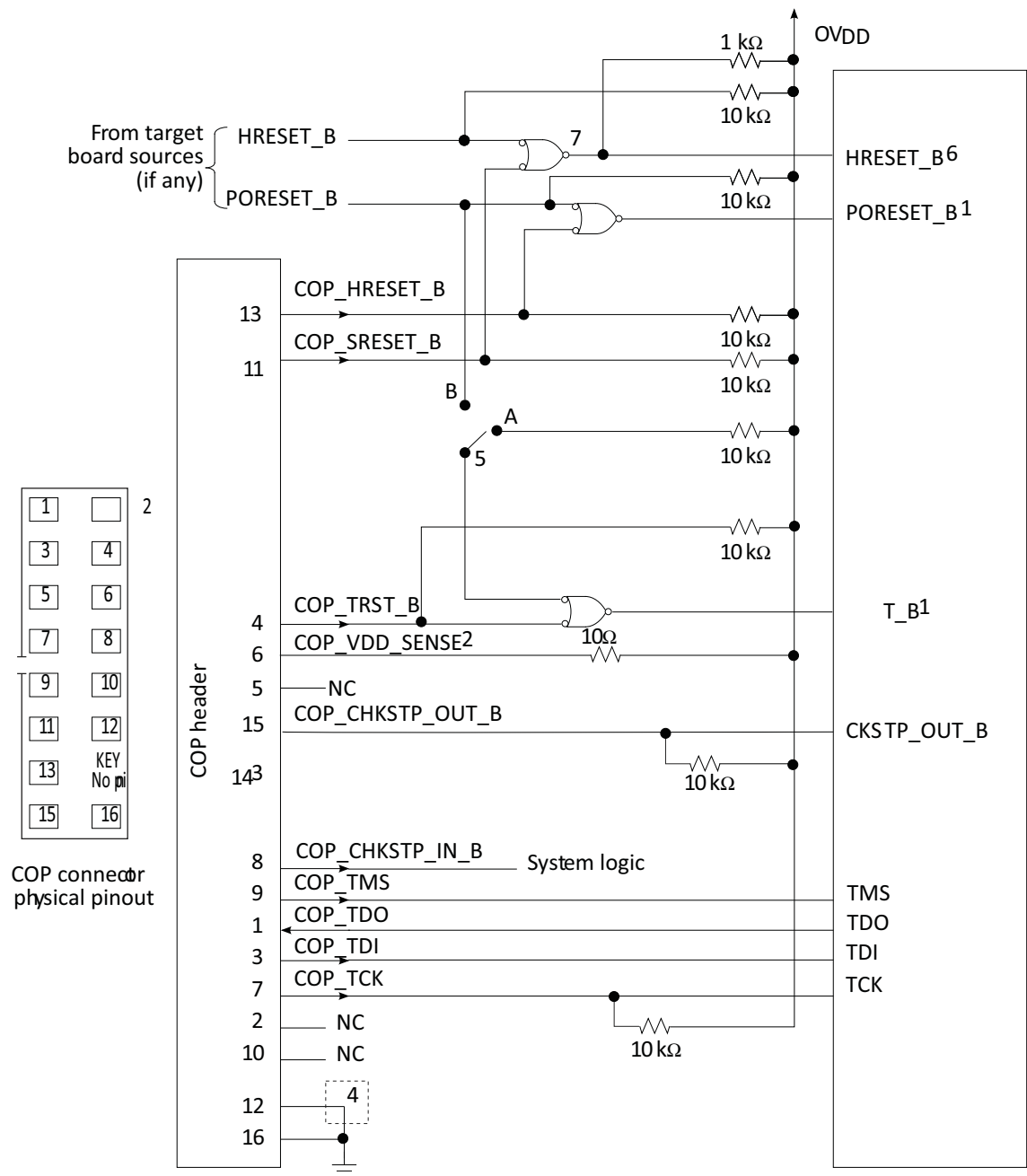
Figure 4-10. Legacy COP Connector Physical Pinout



- Notes:
- 1. The COP port and target board should be able to independently assert PORESET\_B and TRST\_B to the processor in order to fully control the processor as shown here.
  - 2. Populate this with a 10Ω resistor for short-circuit/current-limiting protection.
  - 3. The KEY location (pin 14) is not physically present on the COP header.
  - 4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
  - 5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST\_B line. If BSDL testing is not being performed, this switch should be closed to position B.
  - 6. Asserting HRESET\_B causes a hard reset on the device
  - 7. This is an open-drain output gate.



**Figure 4-11.** Legacy JTAG Interface Connection



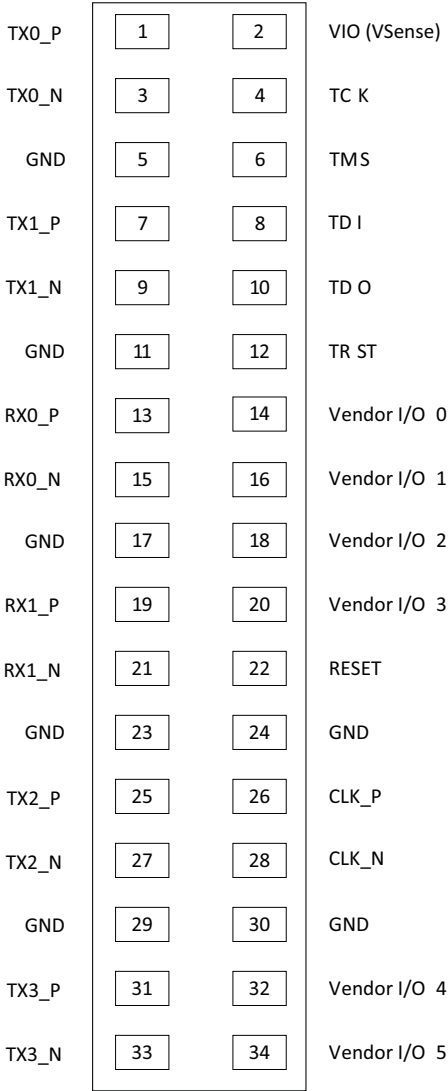
4.5.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in the figures below. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TELEDYNE e2v recommends that the Aurora 34 pin duplex connector be designed into the system as shown in [Figure 4-14](#) or the 70 pin duplex connector be designed into the system as shown in [Figure 4-15](#).

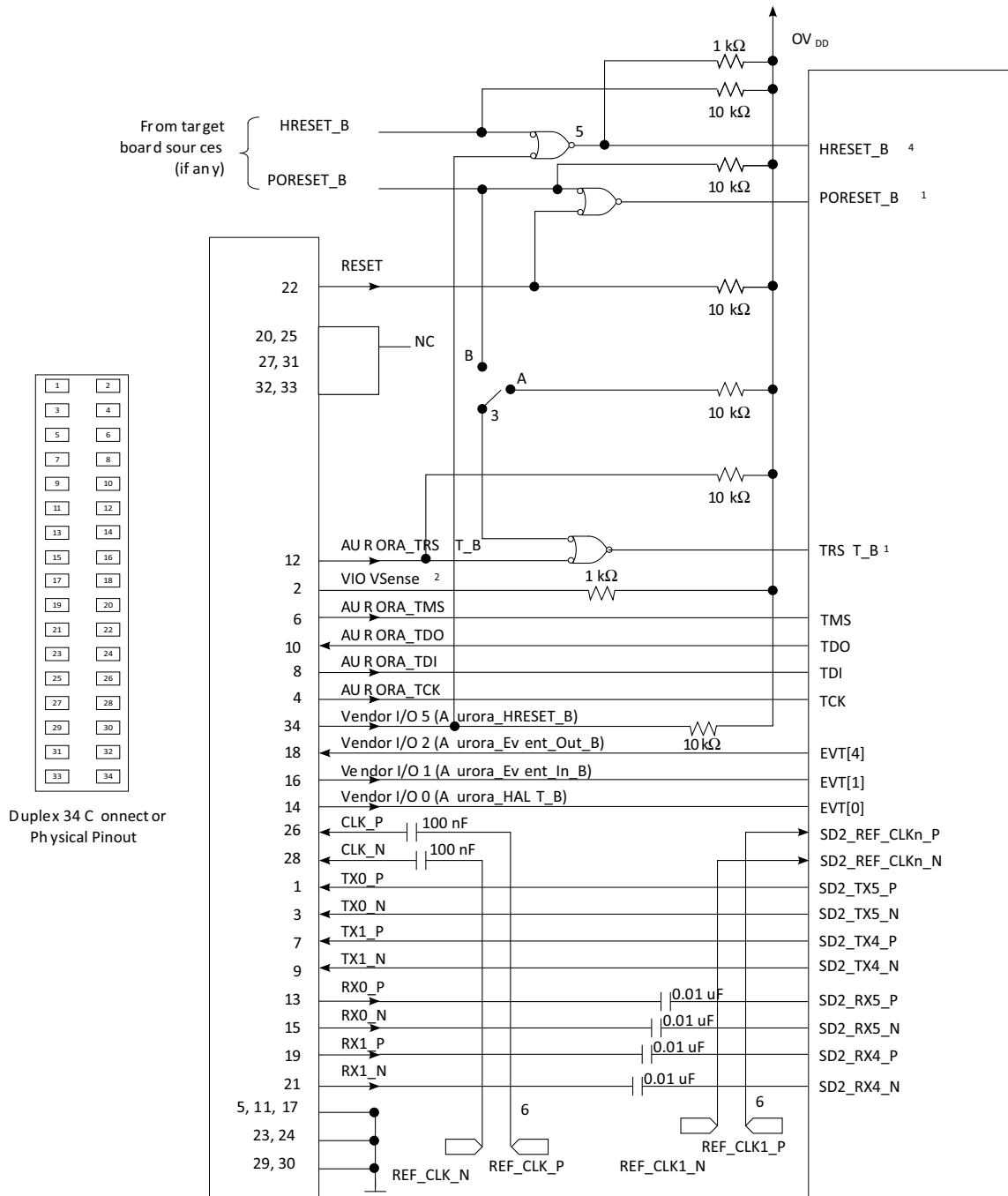
If the Aurora interface will not be used, TELEDYNE e2v recommends the legacy COP header be designed into the system as described in "Termination of unused signals" in the chip reference manual.

Figure 4-12. Aurora 34 pin connector duplex pinout



**Figure 4-13.** Aurora 70 pin connector duplex pinout

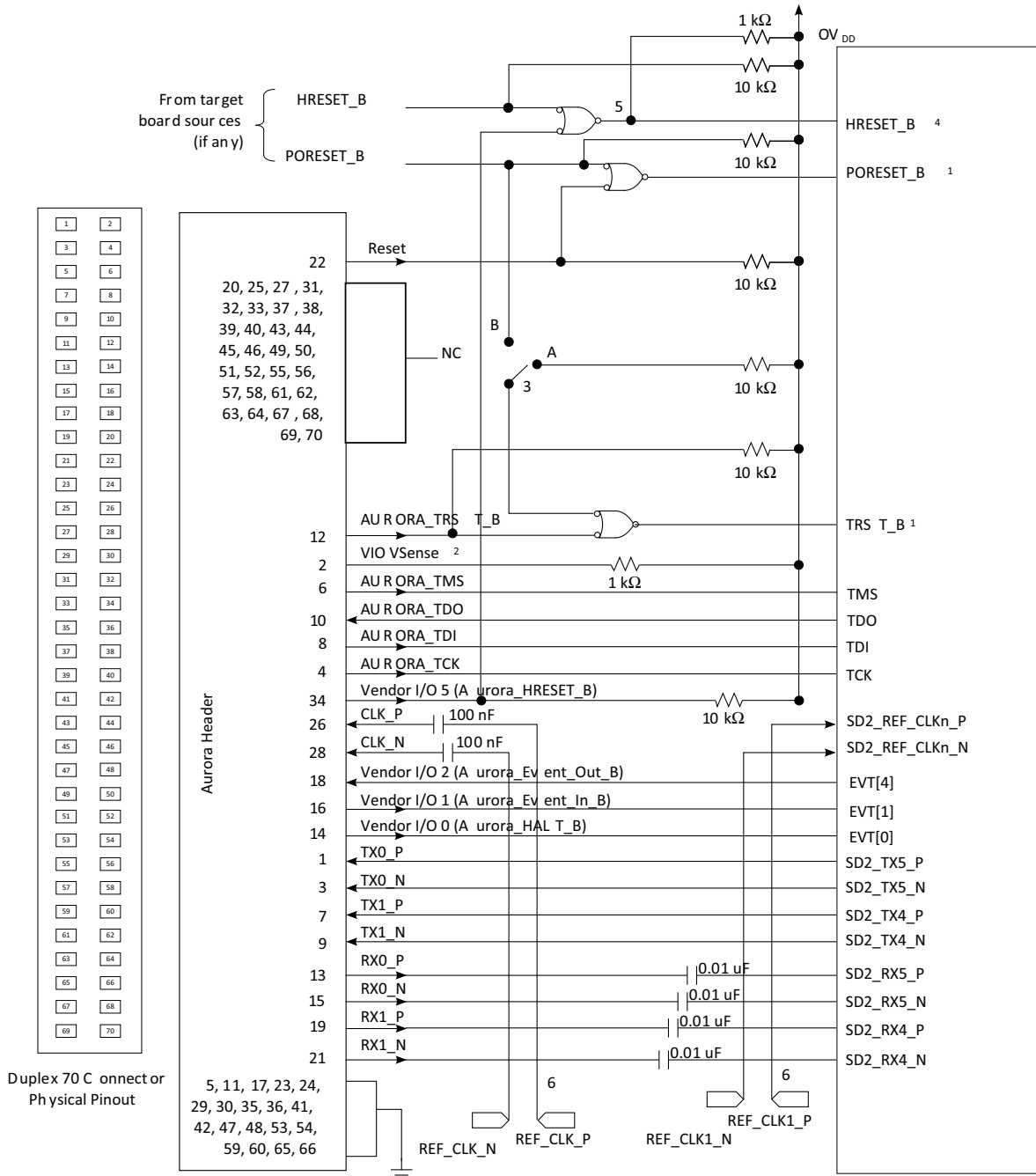
|       |    |    |              |
|-------|----|----|--------------|
| TX0_P | 1  | 2  | VIO (VSense) |
| TX0_N | 3  | 4  | TCK          |
| GND   | 5  | 6  | TMS          |
| TX1_P | 7  | 8  | TDI          |
| TX1_N | 9  | 10 | TDO          |
| GND   | 11 | 12 | TR ST        |
| RX0_P | 13 | 14 | Vendor I/O 0 |
| RX0_N | 15 | 16 | Vendor I/O 1 |
| GND   | 17 | 18 | Vendor I/O 2 |
| RX1_P | 19 | 20 | Vendor I/O 3 |
| RX1_N | 21 | 22 | RESET        |
| GND   | 23 | 24 | GND          |
| TX2_P | 25 | 26 | CLK_ P       |
| TX2_N | 27 | 28 | CLK_ N       |
| GND   | 29 | 30 | GND          |
| TX3_P | 31 | 32 | Vendor I/O 4 |
| TX3_N | 33 | 34 | Vendor I/O 5 |
| GND   | 35 | 36 | GND          |
| RX2_P | 37 | 38 | N/C          |
| RX2_N | 39 | 40 | N/C          |
| GND   | 41 | 42 | GND          |
| RX3_P | 43 | 44 | N/C          |
| RX3_N | 45 | 46 | N/C          |
| GND   | 47 | 48 | GND          |
| TX4_P | 49 | 50 | N/C          |
| TX4_N | 51 | 52 | N/C          |
| GND   | 53 | 54 | GND          |
| TX5_P | 55 | 56 | N/C          |
| TX5_N | 57 | 58 | N/C          |
| GND   | 59 | 60 | GND          |
| TX6_P | 61 | 62 | N/C          |
| TX6_N | 63 | 64 | N/C          |
| GND   | 65 | 66 | GND          |
| TX7_P | 67 | 68 | N/C          |
| TX7_N | 69 | 70 | N/C          |

**Figure 4-14.** Aurora 34 pin connector duplex interface connection

- Notes:
1. The Aurora port and target board should be able to independently assert PORESET\_B and TRST\_B to the processor in order to fully control the processor as shown here.
  2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
  3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST\_B line. If BSDL testing is not being performed, this switch should be closed to position B.
  4. Asserting HRESET\_B causes a hard reset on the device

- This is an open-drain output gate.
- REF\_CLK\_P/REF\_CLK\_N and REF\_CLK1\_P/REFCLK1\_N are buffered clocks from the same common source.

**Figure 4-15.** Aurora 70 pin connector duplex interface connection



- Notes:
- The Aurora port and target board should be able to independently assert PORESET\_B and TRST\_B to the processor in order to fully control the processor as shown here.
  - Populate this with a 1 k $\Omega$  resistor for short-circuit/current-limiting protection.

3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST\_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HREST\_B causes a hard reset on the device
5. This is an open-drain output gate.
6. REF\_CLK\_P/REF\_CLK\_N and REF\_CLK1\_P/REFCLK1\_N are buffered clocks from the same common source.

### 4.5.3 Guidelines for high-speed interface termination

#### 4.5.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that  $SnV_{DD}$ ,  $XnV_{DD}$  and  $AVDD\_SDn\_PLLn$  must remain powered.

For  $AVDD\_SDn\_PLLn$ , it must be connected to  $XnV_{DD}$  through a zero ohm resistor (instead of filter circuit shown in [Figure 4-5](#)).

The following pins must be left unconnected:

- $SDn\_TX[7:0]_P$
- $SDn\_TX[7:0]_N$

The following pins must be connected to SnGND:

- $SDn\_RX[7:0]_P$
- $SDn\_RX[7:0]_N$
- $SDn\_REF\_CLK1\_P$ ,  $SDn\_REF\_CLK2\_P$
- $SDn\_REF\_CLK1\_N$ ,  $SDn\_REF\_CLK2\_N$

The following pins must be left unconnected:

- $SDn\_IMP\_CAL\_RX$
- $SDn\_IMP\_CAL\_TX$

It is possible to independently disable each SerDes module by disabling all PLLs associated with it.

SerDes n = 1:2 is disabled as follows:

- $SRDS\_PLL\_PD\_Sn = 2'b11$  (both PLLs configured as powered down)
- $SRDS\_PLL\_REF\_CLK\_SEL\_Sn = 2'b00$
- $SRDS\_PRTCL\_Sn = 2$  (no other values permitted when both PLLs are powered down)

#### 4.5.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both  $SnVDD$  and  $XnVDD$  must remain powered.

If any of the PLLs are un-used, the corresponding  $AVDD\_SDn\_PLLn$  must be connected to  $XnVDD$  through a zero ohm resistor (instead of filter circuit shown in [Figure 4-5](#)).

The following unused pins must be left unconnected:

- $SDn\_TX[n]_P$
- $SDn\_TX[n]_N$

The following unused pins must be connected to SnGND:

- SDn\_RX[n]\_P
- SDn\_RX[n]\_N
- SD1\_REF\_CLK[1:2]\_P, SD1\_REF\_CLK[1:2]\_N (If entire SerDes 1 unused)
- SD2\_REF\_CLK[1:2]\_P, SD2\_REF\_CLK[1:2]\_N (If entire SerDes 2 unused)

In the RCW configuration field SRDS\_PLL\_PD\_Sn, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

After POR, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDSxPLLnRSTCTL).

Unused lanes must be powered down by clearing the RRST and TRST fields and setting the RX\_PD and TX\_PD fields in the corresponding lane's general control register (SRDSxLNmGCR0).

## 4.5.4 USB controller connections

This section details the hardware connections required for the USB controllers.

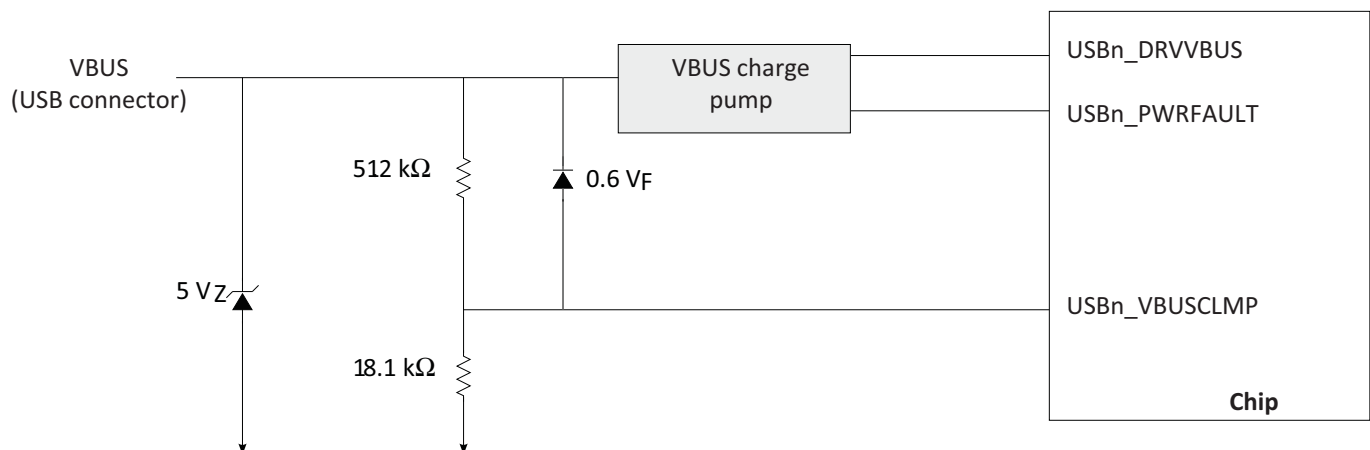
### 4.5.4.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.

- The zener diode must have a value of 5 V-5.25 V.
- The 0.6 V diode requires an  $I_F = 10$  mA,  $I_R < 500$  nA and  $V_{F(Max)} = 0.8$  V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

**Figure 4-16.** Divider network at VBUS



## 4.6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

**Table 4-6.** Package thermal characteristics<sup>(1)</sup> (Rev 1.1)

| Rating                                  | Board                   | Symbol             | Value | Unit | Notes  |
|---|-------------------------|--------------------|-------|------|--------|
| Junction to ambient, natural convection | Single-layer board (1s) | $R_{\theta JA}$    | 20    | °C/W | (2)(3) |
| Junction to ambient, natural convection | Four-layer board (2s2p) | $R_{\theta JA}$    | 13    | °C/W | (2)(4) |
| Junction to ambient (at 200 ft./min.)   | Single-layer board (1s) | $R_{\theta JMA}$   | 14    | °C/W | (2)(3) |
| Junction to ambient (at 200 ft./min.)   | Four-layer board (2s2p) | $R_{\theta JMA}$   | 10    | °C/W | (2)(3) |
| Junction to board                       | —                       | —                  | 4     | °C/W | (4)    |
| Junction to case top                    | —                       | $R_{\theta JCTOP}$ | 0.6   | °C/W | (5)    |
| Junction to lid top                     | —                       | $R_{\theta JCLID}$ | 0.25  | °C/W | (6)    |

Notes: 1. See [Thermal management information](#) for additional details.

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.
- Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

## 4.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local TELEDYNE e2v sales office.

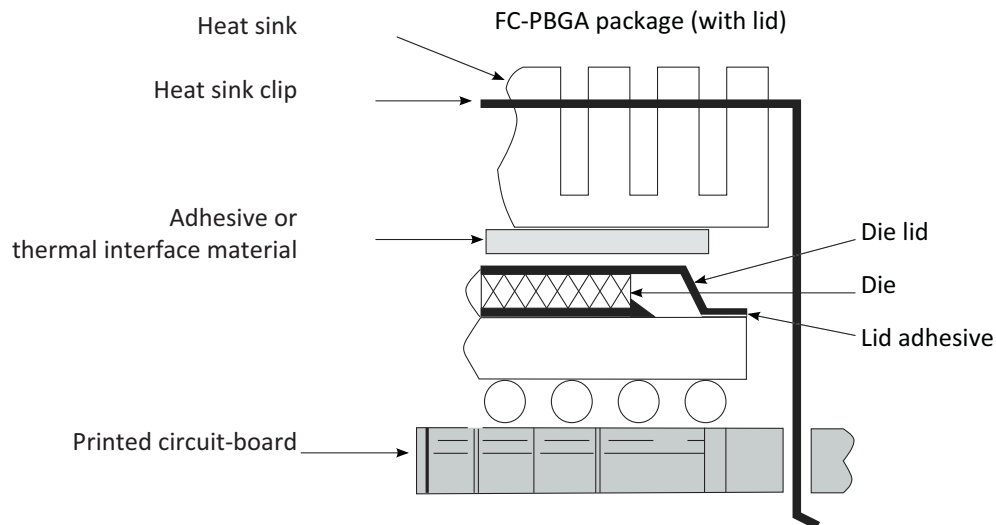
## 4.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in [Figure 4-17](#). The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 18 pounds force (45 Newton).



**Figure 4-17.** Package exploded, cross-sectional view-FC-PBGA (with lid) - Rev 1.1



The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

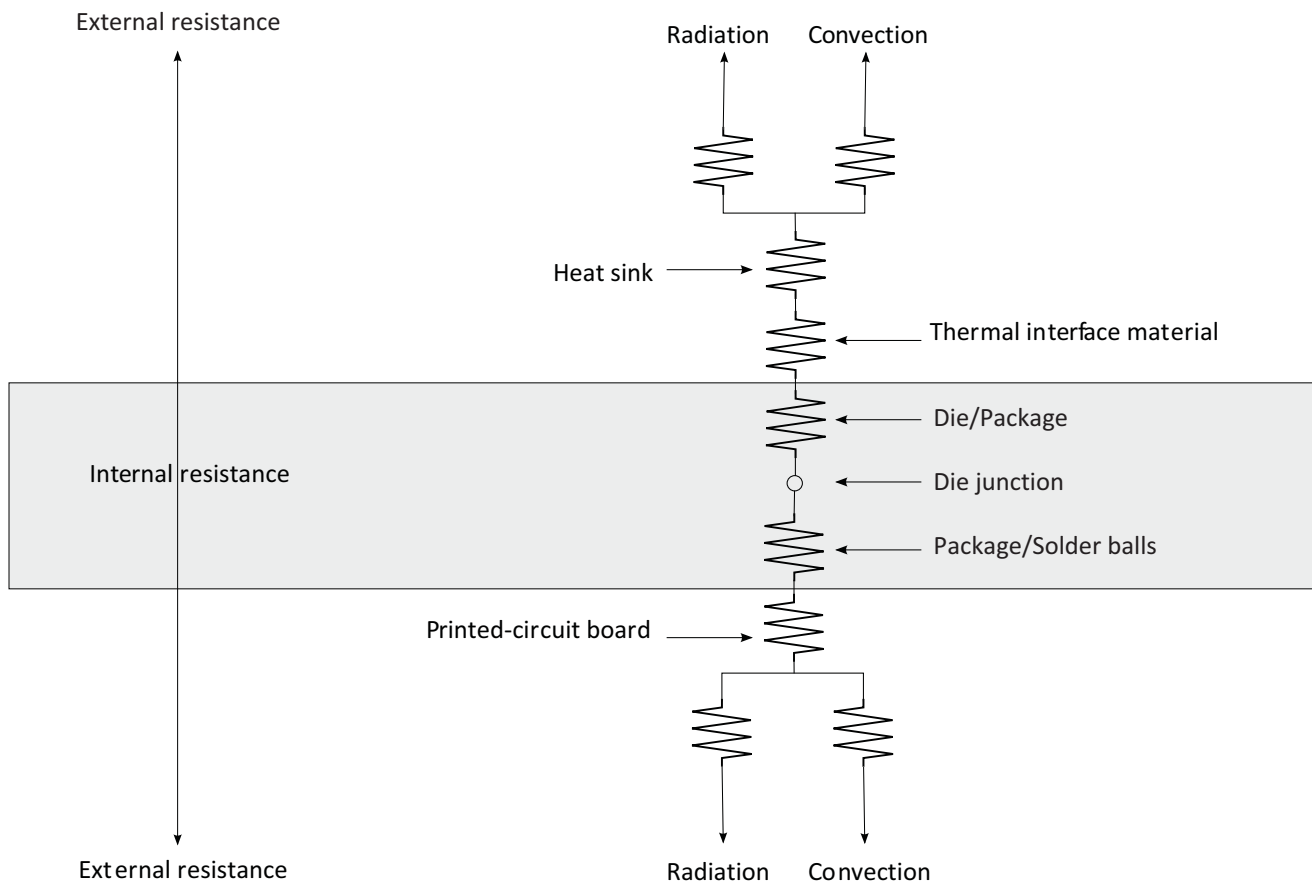
For additional information regarding thermal management of lid-less flip-chip packages, refer to application note AN4871 "Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages".

## 4.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

**Figure 4-18.** Package with heat sink mounted to a printed-circuit board

(Note the internal versus external package resistance)

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

#### 4.8.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see [Figure 4-17](#)).

The system board designer can choose among several types of commercially-available thermal interface materials.

## 5. PACKAGE INFORMATION

### 5.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 25 mm × 25 mm, 896 flip-chip, plastic-ball, grid array (FC-PBGA).

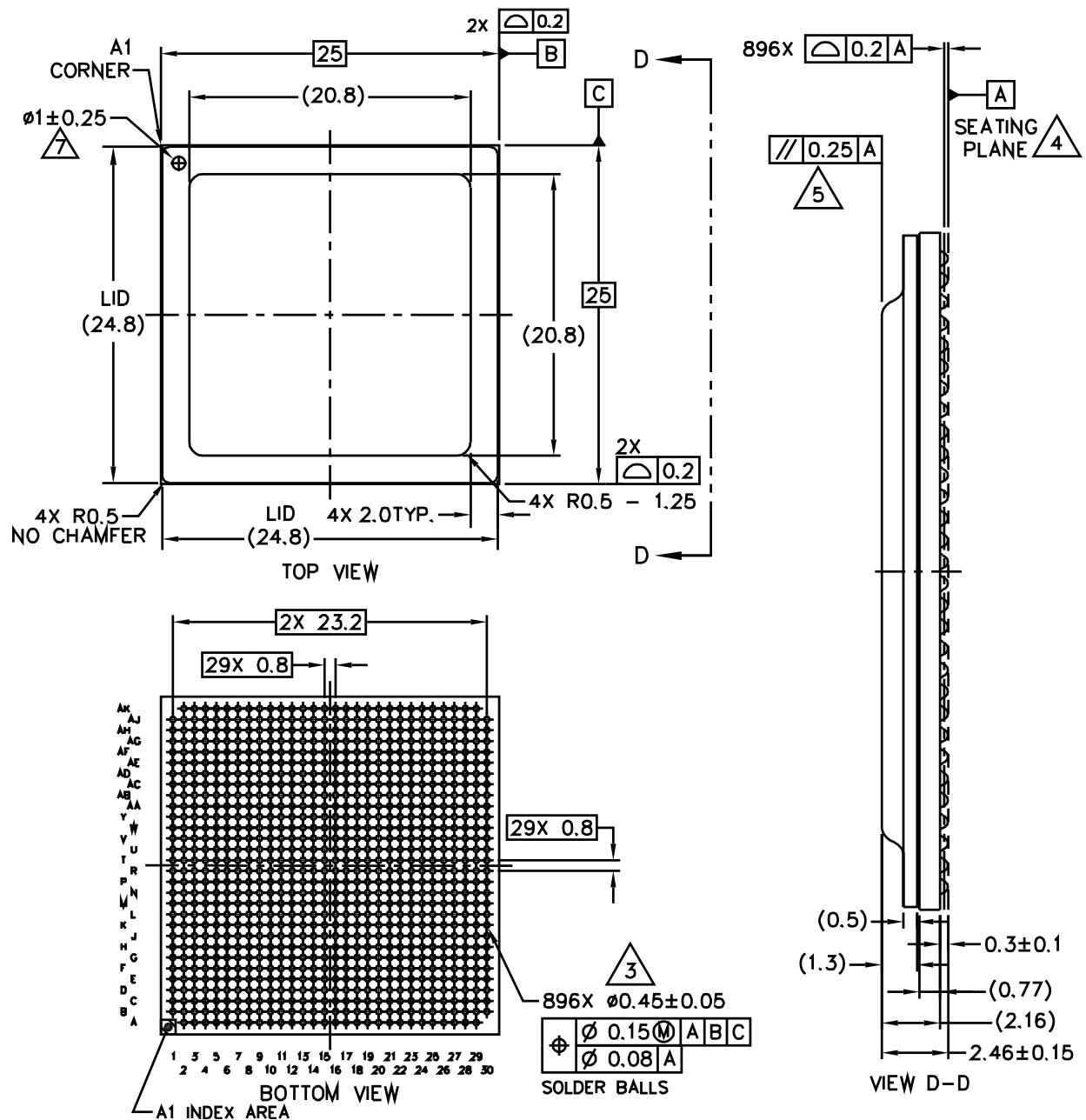
Rev 1.1:

- Package outline - 25 mm × 25 mm
- Interconnects - 896
- Ball pitch - 0.8 mm
- Ball diameter (typical) - 0.45 mm
- Solder balls - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height - 2.31 mm (minimum), 2.46 mm (typical), 2.61 (maximum)

## 5.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip for Rev 1.1 silicon.

**Figure 5-1.** Mechanical dimensions of the FC-PBGA, with lid



- Notes:
1. All dimensions are in millimeters.
  2. Dimensions and tolerances per ASME Y14.5M-1994.
  3. Maximum solder ball diameter measured parallel to datum A.
  4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
  5. Parallelism measurement shall exclude any effect of mark on top surface of package.

## 6. SECURITY FUSE PROCESSOR

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the PROG\_SFP pin per Power sequencing. PROG\_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of eight fuse programming cycles. All other times PROG\_SFP should be connected to GND. The sequencing requirements for raising and lowering PROG\_SFP are shown in [Figure 3-2](#). To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per [Table 3-2](#).

### NOTE

Users not implementing the QorIQ platform's Trust Architecture features should connect PROG\_SFP to GND.

Changed "two fuse programming cycles" to "eight fuse programming cycles" in Security fuse processor

## 7. ORDERING INFORMATION

Please contact your local TELEDYNE e2v sales office or regional marketing team for ordering information.

This table provides the TELEDYNE e2v QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your TELEDYNE e2v Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Contact your local TELEDYNE e2v sales office or regional marketing team for order information.

**Table 7-1.** Ordering Information

| Generation   | Platform | Number of virtual cores | Derivatives | Temperature range                         | Encryption                             | Package Type   | CPU Speed                                    | DDR Data Rate                                  | Low power                         | Product Revision |
|--------------|----------|-------------------------|-------------|---|--|--|--|--|-----------------------------------|------------------|
| T(X) = 28 nm | 2        | 08 = 8 virtual cores    | 0-9         | A : -40/105<br>F : -40/125<br>M : -55/125 | E = SEC present<br>N = SEC not present | 3 = FCPBGA<br>C4 Pb-free<br>/C5 Leaded<br>8 = FCPBGA<br>C4/C5 Pbfree | M = 1200 MHz<br>P = 1533 MHz<br>T = 1800 MHz | Q = 1600 MT/s<br>T = 1866 MT/s<br>1 = 2133MT/s | L = low power<br>blank = standard | B = Rev 1.1      |

Notes: 1. For availability of the different versions, contact your local TELEDYNE e2v sales office.  
 2. The letter x in the part number designates a "Prototype" product that has not been qualified by TELEDYNE e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

## 8. Definitions

### 8.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. TELEDYNE e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TELEDYNE e2v for any damages resulting from such improper use or sale.

## 9. Revision History

This table provides revision history for this document.

**Table 9-1.** Revision History

| Rev. No | Date    | Substantive Change(s)   |
|---------|---------|---|
| 1170D   | 10/2018 | <p><a href="#">Table 3-2, "Recommended operating conditions," on page 40</a></p> <ul style="list-style-type: none"> <li>- Updated temperature range name</li> </ul>   |
| 1170C   | 05/2018 | <ul style="list-style-type: none"> <li>. Changed <math>XV_{DD}</math> to <math>SV_{DD}</math> in <a href="#">Figure 3-1</a></li> <li>. Updated the row "AC Input Swing Limits at 1.8 V <math>OV_{DD}</math>" in <a href="#">Table 3-12</a></li> <li>. Updated the row "Input capacitance" in <a href="#">Table 3-14</a></li> <li>. Removed the table "PLL lock times" from the section <a href="#">Section 3.7 "RESET initialization" on page 56</a></li> <li>. Added <a href="#">Table 3-47</a> and <a href="#">Figure 3-18</a></li> <li>. Updated the row "Input current (<math>OVIN = 0</math> V or <math>OVIN = OVDD</math>)" in <a href="#">Table 3-50</a></li> <li>. Updated note 5 in <a href="#">Table 4-1</a></li> <li>. Changed "two fuse programming cycles" to "eight fuse programming cycles" in <a href="#">Section 6. "Security fuse processor" on page 154</a></li> <li>. Updated <a href="#">Table 7-1, "Ordering Information," on page 154</a></li> </ul>   |
| 1170B   | 11/2016 | <ul style="list-style-type: none"> <li>. In the pin list table: <ul style="list-style-type: none"> <li>Revealed alternate pin SDHC_CLK_SYNC_IN on primary pin IRQ[10].</li> <li>Revealed alternate pin SDHC_CLK_SYNC_OUT on primary pin SPI_CS_B[3].</li> </ul> </li> <li>. In <a href="#">Section 3.2 "Power sequencing" on page 43</a>, added a note for the frequency requirements when using Trust Architecture Security Monitor battery-backed features and changed the stable value from 75 ms to 400 ms.</li> <li>. In <a href="#">Table 3-5</a> and <a href="#">Table 3-6</a>, added the 1533 MHz and 1200 MHz low-power numbers and added footnote 9.</li> <li>. In <a href="#">Section 3.9.2 "eSPI AC timing specifications" on page 63</a>, added a note for the master mode internal clock diagram that SPICLK appears on the interface only after CS assertion.</li> <li>. In <a href="#">Section 3.11.2.2 "RGMIIC AC timing specifications" on page 66</a>, added a note to footnote 9 that MAC10 is not impacted by erratum A-005177 and meets industry specifications.</li> <li>. Throughout the document, removed Rev 1.0 information and the preliminary data disclaimers.</li> <li>. In <a href="#">Table 3-2</a>, added table footnote 8.</li> <li>. Updated <a href="#">Table 3-3</a>, "Output driver capability."</li> <li>. In <a href="#">Table 3-5</a> and <a href="#">Table 3-6</a>, added the 2133 MT/s (low-power version) numbers and re-ordered the rows from largest to smallest MHz power number.</li> <li>. In <a href="#">Table 3-7</a>: Added rows for DDR I/O 2133 MT/s and USB_SVDD.</li> <li>. Updated the SerDes 1.35 V parameter to "4x 5 G-baud".</li> <li>. In <a href="#">Table 3-9</a>, updated the PH10 core frequencies.</li> <li>. In <a href="#">Table 3-18</a>, added the maximum rise/fall of PORESET_B and changed the HRESET_B max from 1 to 10.</li> <li>. In <a href="#">Section 3.8 "DDR3 and DDR3L SDRAM controller" on page 56</a>, added to the NOTE that DDR3L is not supported at a DDR data rate of 2133 MT/s.</li> <li>. In the tables of <a href="#">Section 3.8.1 "DDR3 and DDR3L SDRAM interface DC electrical characteristics" on page 57</a>, changed "<math>Dn\_MVREF</math>" to "<math>MVREFn</math>".</li> <li>. In <a href="#">Table 3-19</a>, updated the I/O leakage current min/max from -100/100 to -50/50.</li> <li>. In <a href="#">Table 3-22</a> and <a href="#">Table 3-23</a>, added the 2133 MT/s data rates and added notes that only DDR3 supports 2133 MT/s.</li> <li>. In <a href="#">Table 3-31</a>, added "10 Mbps" to note 9 as an option for RGMIIC if the device cannot cope with a wide skew.</li> <li>. Added <a href="#">Table 3-32</a>, "Ethernet management interface 1 DC electrical characteristics (<math>LVDD = 1.8</math> V)."</li> <li>. In <a href="#">Table 3-36</a>, removed "x2" from "(Frame Manager x2)" in table footnote 4.</li> <li>. In <a href="#">Table 3-38</a>, changed the input current min and max to -50 and 50.</li> <li>. In <a href="#">Table 3-70</a>, updated the unit interval minimum from 199.40 to 199.94.</li> <li>. In note 2 of <a href="#">Table 3-102</a> and in the final paragraph of SGMII and SGMII 2.5x receiver AC timing Specification, changed the figure reference from <a href="#">Figure 3-36</a> to <a href="#">Figure 3-37</a>.</li> </ul> |

**Table 9-1.** Revision History (Continued)

| Rev. No | Date    | Substantive Change(s)  |
|---------|---------|--|
|         |         | <p>. In <a href="#">Table 4-1</a>, updated the 1800 MHz memory bus clock frequency maximum from 933 to 1066 and, in table footnote 6, changed the XFI minimum frequency from 359 MHz to 300 MHz.</p> <p>. In <a href="#">Table 4-2</a>, changed the maximum frequency from 933 MHz to 1066 MHz.</p> <p>. Removed the following sections:</p> <p>"Platform to SYSCLK PLL ratio"</p> <p>"Core cluster to SYSCLK PLL ratio"</p> <p>"Core complex PLL select"</p> <p>"DDR controller PLL ratios"</p> <p>"Frame Manager clock select"</p> <p>"eSDHC SDR mode clock select"</p> <p>. In <a href="#">Section 4.5 "Connection recommendations" on page 139</a>, changed the example from "Analog Devices, ADT7461A" to "Semiconductor, NCT72" and added the chip temperature diode specifications.</p> <p>. In <a href="#">Section 4.8 "Thermal management information" on page 149</a>, updated the recommended spring force maximum from 10 pounds to 18 pounds.</p> <p>. Updated <a href="#">Section 5.2 "Mechanical dimensions of the FC-PBGA" on page 153</a>, to include package parameters.</p> |
| 1170A   | 01/2016 | Initial revision   |

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