PRELIMINARY DATASHEET

OVERVIEW

EV12AD500A is a dual S-band capable 12bit ADC intended for various applications that is built using a true single core architecture providing high spectral purity.
With a 3dB input bandwidth of 5.2GHz it allows for digitization in S-band without frequency conversion. Wideband communication and radar systems will also be able to operate this ADC with reduced dynamic range at frequencies beyond 5GHz without frequency down-conversion.
This device outputs data either in LVDS format with low latency or high speed serial link using the ESIstream (Efficient Serial Interface) protocol.
It proposes a multiple ADC chained synchronization feature. Along with the serial interface, it helps designing large array of synchronous ADC in active antenna array or MIMO systems.
Dual channel crosstalk isolation exhibits figure in excess of 80dB and Noise Power Ratio performance beyond 50dB in the first Nyquist zone.
This device comes in a flip chip CBGA255 package in HiTCE® substrate with High Temperature Coefficient of Expansion.

APPLICATIONS

- Wideband communication system
- Phased-array/MIMO communication system
- Phased-array/MIMO radar system
- Instrumentation

FEATURES

Dual channel 12 bits 1.5GSps ADC

- Single core architecture ADC
- Differential analog input voltage: 1Vppd
- Full Power Input bandwidth (-3dB): 5.2GHz
- Differential clock input
- Power consumption: 2.3W / channel
- Power supplies: Single Rail 3.4V or Dual rail 3.4V/2.5V
- Output interface: LVDS DEMUX 1:1 or serial ESIstream
- Package: CBGA255 14x14mm / 0.8mm pitch
- SPI configuration
- Multiple ADC chained synchronization
- Test mode: ramp, flash, PRBS
- Control bit: parity, in-range, trigger, timestamp
- Clock input up to 3GHz

PERFORMANCE @ 1.5GSps

- 5.2GHz analog input bandwidth (-3dB)

- 50 dB NPR over 1st Nyquist
- 48 dB NPR over 2nd Nyquist
- 46 dB NPR over 3rd Nyquist

- 70 dBFS SFDR at 100MHz, -1dBFS
- 70 dBFS SFDR at 1900MHz, -8dBFS
- 60 dBFS SFDR at 3730MHz, -12dBFS
- 54 dBFS SFDR at 5300MHz, -12dBFS

- Latency < 7.5ns in LVDS output
- Latency < 17ns in serial output

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1 Bloc Diagrams

1.1 DEMUX 1:1

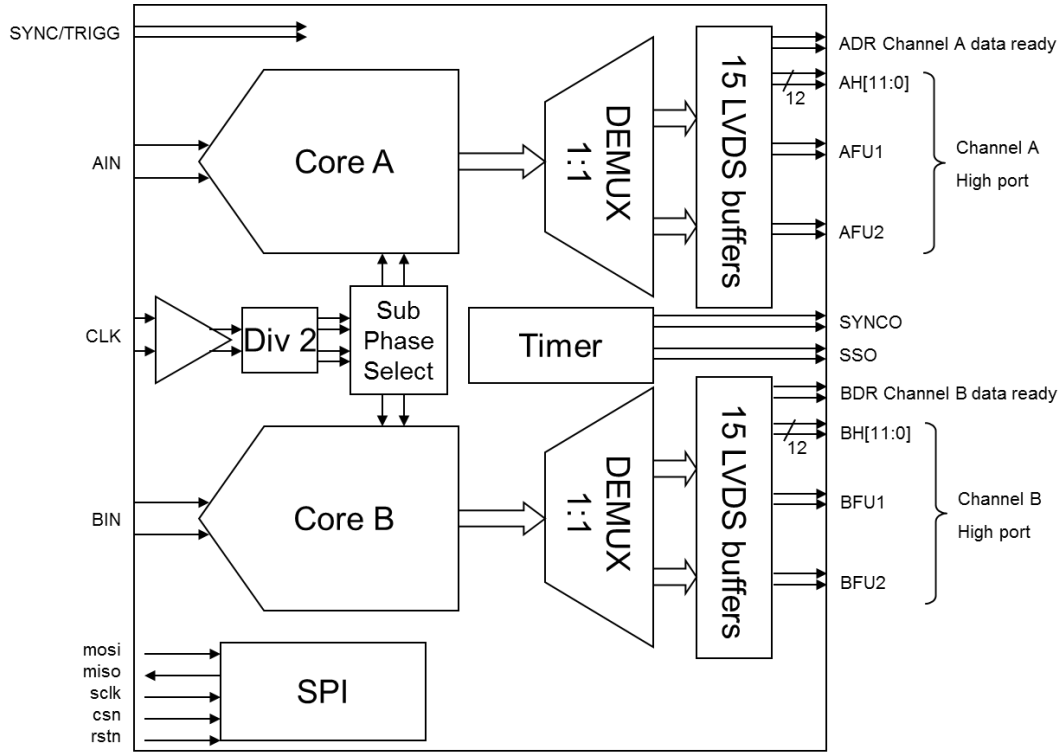


Figure 1: Bloc diagram in DEMUX 1:1 output mode

1.2 High speed serial interface

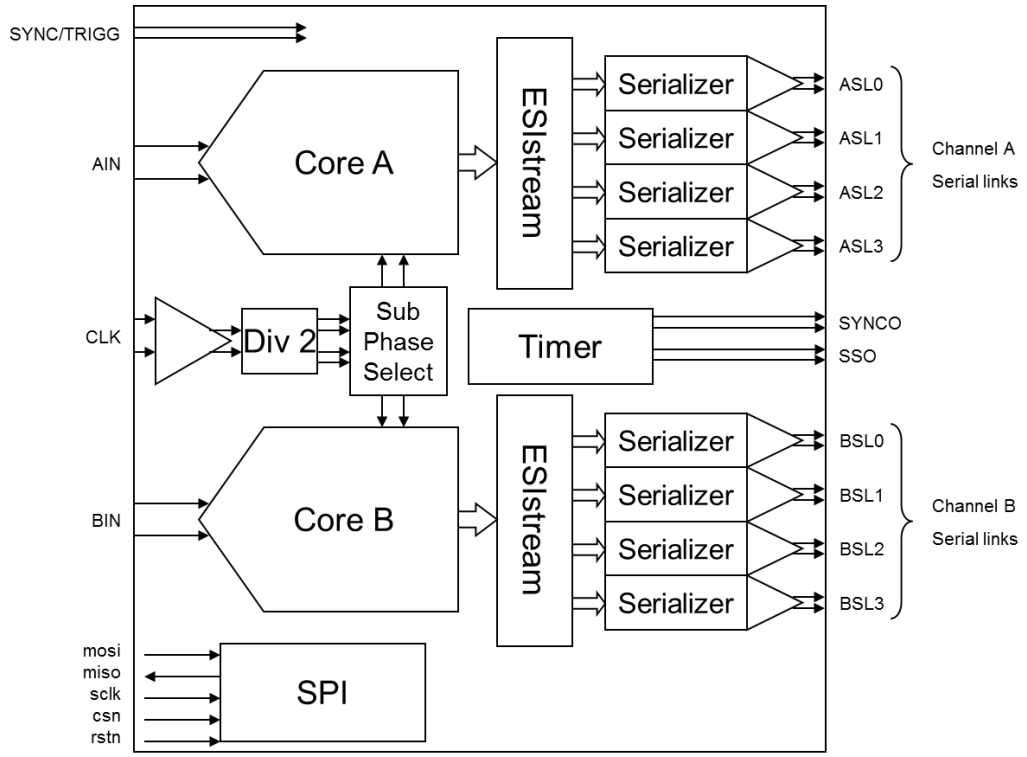


Figure 2: Bloc diagram in serial ESIstream output mode

2 Description

The EV12AD500A is a dual 12 bit 1.5GSps ADC featuring low latency LVDS 1:1 parallel output and a high speed serial output option based on the ESIstream (Efficient Serial Interface) protocol.

The two channels can operate in phase or in opposition, thus allowing synchronous or interleaved sampling. Each channel is composed of a true single core ADC sampling at up to 1.5GSps. Based on an innovative architecture without interleaving, it provides high spectral purity. It offers an analog input bandwidth up to 5.2GHz with 2 selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. It also features a novel synchronization method to ease the synchronization of a large number of ADCs. This device is clocked at twice the sampling rate of each channel, thus at 3GHz at full speed where the channels sample at 1.5GSps. It is controlled through an SPI interface. All sensitive areas of the device have been protected to increase robustness. This includes, but is not limited to, clock circuitry and SPI registers. A supplementary feature is also provided to increase this robustness of the ADC and prevent potential external influence.

The EV12AD500A is available in a HiTCE255 package using flip-chip assembly and operates over the temperature range -40°C < Tc; Tj < +110°C.

3 Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Exposure to maximum ratings may affect device reliability.

Table 1: Absolute maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
VCCA analog supply voltage	V_{CCA}	AGND – 0.3	3.8	V
VCCIOxx output supply voltage		GNDIO – 0.3	3.8	V
VCCD digital supply voltage	V_{CCD}	DGND – 0.3	3.8	V
Analog input swing	|AIN - AINN|, |BIN - BINN|		4.8	Vppd
Analog input voltage	AIN, AINN, BIN, BINN	AGND - 0.3	3.6	V
Clock input swing	[CLK - CLKN|		4	Vppd
Clock input voltage	CLK, CLKN	AGND - 0.3	3.75	V
SYNC input voltage	SYNC, SYNCN	AGND - 0.3	VCCA + 0.3	V
SYNC input swing	|SYNC - SYNCN|		4	Vppd
SPI input voltage	RSTN, SCLK, CSN, MOSI	DGND - 0.3	VCCD + 0.3	V
VDIODEA input voltage	DIODEA	-0.9	0.3	V

Notes: Inputs have been designed to allow for “cold sparing”. This means that all inputs of the ADC can receive an input signal while VCCA and VCCD are either floating or to GND, as long as they are below the maximum ratings specified above (considering typical value for VCCA, VCCD and VCCIOxx)

Table 2: Absolute maximum ratings (ESD and temperature)

Parameter		Symbol	Value	Unit
In serial interface output mode	Electrostatic discharge (HBM)	ESD HBM	1000	V
	ESD classification		Class 1C	
In LVDS DMUX 1:1 output mode	Electrostatic discharge (HBM)		750	V
	ESD classification		Class 1B	
Storage temperature range		Tstg	-65 to +150	°C

Notes: All integrated circuits have to be handled with appropriate care to avoid damage due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure

3.2 Recommended conditions of use

Table 3: Recommended conditions of use

Parameter	Symbol	Value	Unit
VCCA analog supply voltage	V_{CCA}	3.4	V
VCCIOS1 output supply voltage	V_{CCIOS1}	2.5	V
VCCIOH1 output supply voltage	V_{CCIOH1}	3.4 or 2.5	V
VCCIOx2 output supply voltage	V_{CCIOx2}	3.4	V
VCCD digital supply voltage	V_{CCD}	3.4 or 2.5	V
External clock frequency	Fc	≤ 3	GHz
Differential analog input full scale swing	$\lvert AIN_P - AIN_N \rvert$, $\lvert BIN_P - BIN_N \rvert$	1.0	Vppd
Differential analog input full scale power	P_A, P_B	1	dBm
Differential clock input power	P_{CLK}	1	dBm
SPI input voltage	V_{IL}	0	V
	V_{IH}	VCCD	V

Notes: Vccioh1= 2.5V and V_{CCD} =2.5V can be used to reduce power consumption. Refer to Table 18 in section Output selection for more information

Table 4: Recommended temperature conditions of use

Parameter	Symbol	Value	Unit
Operating temperature range (for performances)	Tc; Tj	-40 < Tc ; Tj < +110	°C
Operating temperature range for long term reliability	Tc; Tj	TBD	°C

Notes: Tj refers to the hot spot junction temperature on the die
Qualification pending

3.3 Explanation of test levels

Table 5: Explanation of test levels

Test level	Comments
1	100% production tested at Tamb = +25°C (1)
2	100% production tested at Tamb = +25°C, and sample tested at specified temperatures (1)
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is guaranteed by design
6	100% tested over specified temperature range

Notes: Only MIN and MAX values are guaranteed.
1. Unless otherwise specified

3.4 Electrical characteristics for supplies, inputs and outputs

Unless otherwise specified:
- Typical values are given for typical supplies in dual-rail configuration (Refer to Table 18 in section Output selection for more information) at Tamb = +25°C
- Minimum and maximum values are given over corresponding temperature range for typical power supplies
- Values are given with SDA disabled

Table 6: Electrical characteristics for supplies, inputs and outputs

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
Resolution				12		bit	
POWER REQUIREMENTS							
Power supply voltage							
• Analog		V_{CCA}	3.25	3.4	3.55	V	
• Output		V_{CCIOS1}	2.35	2.5	2.65	V	
		V_{CCIOH1} 3.4V	3.25	3.4	3.55	V	
		V_{CCIOH1} 2.5V	2.35	2.5	2.65	V	(1)
		V_{CCIOx2}	3.3	3.4	3.55	V	
• Digital		V_{CCD} 3.4V	3.3	3.4	3.55	V	
		V_{CCD} 2.5V	2.35	2.5	2.65	V	
Power supply current in DMUX 1:1							
• Analog, VCCA = 3.4V		I_{CCA}		1090		mA	
• Output 2							
Full swing, VCCIOH2 = 3.4V		I_{CCO2}		62		mA	
Reduced swing, VCCIOH2 = 3.4V		I_{CCO2}		62		mA	
• Output 1							(2)
Full swing, VCCIOH1 = 3.4V		I_{CCO1}		145		mA	
Full swing, VCCIOH1 = 2.5V		I_{CCO1}		100		mA	
Reduced swing, VCCIOH1 = 3.4V		I_{CCO1}		103		mA	
• Digital							
VCCD = 3.4V		I_{CCD}		93		mA	
VCCD = 2.5V		I_{CCD}		88		mA	
Power supply current in serial ESIstream							
• Analog, VCCA = 3.4V		I_{CCA}		1118		mA	
• Output 1, VCCIOS1 = 2.5V		I_{CCO1}		71		mA	(2)
• Output 2, VCCIOS2 = 3.4V		I_{CCO2}		85		mA	
• Digital, VCCD = 2.5V		I_{CCD}		235		mA	
Power supply current in standby mode							
• Analog		I_{CCA}		348		mA	
• Output (DMUX 1:1)		I_{CCO}		164		mA	(2)
• Output (Serial ESIstream)		I_{CCO}		34		mA	
• Digital		I_{CCD}		156		mA	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
Power dissipation (VCCA = VCCD = VCCIOxx = 3.4V) • DEMUX1:1 - Full swing - Reduced swing		P_D		 4.77 4.62		 W W	(2)
Power dissipation (VCCA = VCCIOx2 = 3.4V, VCCD = VCCIOx1 = 2.5V) • DEMUX1:1, Reduced swing • Serial ESIstream		P_D		 4.41 4.85		 W W	(2)
ANALOG INPUTS							
Analog input coupling			AC or DC				(3)
Analog input common mode voltage		V_{INCM}		2.4		V	(4)
Analog differential input full scale voltage		$\|AIN_P - AIN_N\|$, $\|BIN_P - BIN_N\|$			1	Vppd	
Analog differential input full scale power (100Ω differential termination)		P_{IN}			1	dBm	
Analog input leakage current		I_{IN}		40		µA	
Analog input resistance • Without trimming • With trimming		R_{IN}	 80 95	 100 100	 120 105	 Ω Ω	(5)
Crosstalk between analog inputs		Xtalk		80		dB	(6)
CLOCK INPUTS							
Clock common mode voltage		V_{CCM}	2.40	2.57	2.75	V	
Clock differential input power (100Ω differential termination)		P_{CLK}	-3	1	7	dBm	
Clock input capacitance (including die and package)		C_{CLK}		1		pf	
Clock differential input resistance		R_{CLK}	80	100	120	Ω	
Clock slew rate		SR_{CLK}	8	12		GV/s	
Clock jitter (3GHz sine wave) Integrated from 10MHz to 10GHz		Jitter			100	fs_{rms}	
Intrinsic clock jitter - SDA off		Intrinsic jitter		135		fs_{rms}	
- SDA on				200			(7)
Clock duty cycle		Duty cycle	45	50	55	%	
SYNCTRIG INPUTS							
SYNCTRIG common mode voltage		V_{ICM}	1.125	1.25	1.8	V	
SYNCTRIG differential swing		$V_{IH} - V_{IL}$	100	350	450	mVp	
SYNCTRIG input capacitance		C_{SYNC}		1		pf	
SYNCTRIG input resistance		R_{SYNC}	80	100	120	Ω	
SYNCTRIG slew rate		SR_{SYNC}	500			MV/s	
SPI INPUTS (RSTN, SCLK, CSN, MOSI)							
CMOS Schmitt trigger low level threshold		V_{IL}			$0.35V_{CCD}$	V	
CMOS Schmitt trigger high level threshold		V_{IH}	$0.65V_{CCD}$			V	
CMOS Schmitt trigger hysteresis		V_{tH}	$0.1V_{CCD}$			V	
CMOS low level input current		I_{IL}			300	nA	
CMOS high level input current		I_{IH}			1000	nA	

Parameter		Test level	Symbol	Value			Unit	Note
				Min	Typ	Max		
SPI OUTPUT (MISO)								
CMOS low level output voltage			V_{OL}			$0.2V_{CCD}$	V	
CMOS high level output voltage			V_{OH}	$0.8V_{CCD}$			V	
LVDS OUTPUT								
Full swing	- Common mode voltage		VO_{CM}	1.125	1.35	1.45	V	
	- Swing		V_{OH} - V_{OL}	250	350	450	mVp	
	- Logic low		V_{OL}			1.125	V	
	- Logic high		V_{OH}	1.375			V	
Reduced swing	- Common mode voltage		VO_{CM}	1.1	1.35	1.4	V	
	- Swing		V_{OH} - V_{OL}	165	290	300	mVp	
	- Logic low		V_{OL}			1.125	V	
	- Logic high		V_{OH}	1.5			V	
CML OUTPUT (Serial ESIstream)								
Full swing	- Common mode voltage		VO_{CM}		V_{CCIOS1}-0,2		V	
	- Swing		V_{OH} - V_{OL}		400		mVp	
	- Logic low		V_{OL}		V_{CCIOS1}		V	
	- Logic high		V_{OH}		V_{CCIOS1}-0,4		V	
Reduced swing	- Common mode voltage		VO_{CM}		V_{CCIOS1}-0,1		V	
	- Swing		V_{OH} - V_{OL}		200		mVp	
	- Logic low		V_{OL}		V_{CCIOS1}		V	
	- Logic high		V_{OH}		V_{CCIOS1}-0,1		V	

Notes: 1. Refer to Table 18 in section Output selection for more information on power supplies management
2. Enabling SDA increases power consumption by 80mW (23mA on VCCA)
3. The DC analog common mode voltage is provided by the CMIREF output of the ADC
4. See section Input common mode trimming for more information on the range available
5. For optimal performance, in terms of VSWR, the input impedance must be 50Ω ± 5% and the analog input impedance must be digitally trimmed to cope with process deviation. Refer to section Input impedance trimming for more information
6. The crosstalk specified is measured by inputting a 2400MHz tone at -3dBFS on one core and checking the spur level on the other core at this frequency

3.5 Converter characteristics

Unless otherwise specified:

- Typical values are given for typical supplies in dual-rail configuration (Refer to Table 18 in section Output selection for more information) at Tamb = +25°CBoth cores comply with the below specification when the OTP have been loaded
- Minimum and maximum values are given over corresponding temperature range for typical power supplies
- Values are specified at Fs = 1.5GSps for the serial mode and Fs = 1.3GSps for LVDS DMUX1:1 mode
- Values are given with SDA disabled

Table 7: Static characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
DC accuracy / Fs = 1.5GSps, Fin = 100MHz, -1dBFS							
Gain variation		Go	-1.5	0	1.5	dB	(1)
Gain variation versus temperature		G(T)	-0.5	0	0.5	dB	
DC offset			-0.25	0	0.25	LSB	(2)
Differential Non Linearity		DNL	TBD		TBD	LSB	
DNL rms		DNLrms		TBD	TBD	LSB	
Integral Non Linearity		INL	TBD		TBD	LSB	
INL rms		INLrms		0.6	TBD	LSB	

Notes: 1. This value corresponds to the maximum deviation from part to part
2. After DC offset calibration

Table 8: Dynamic characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
ANALOG INPUT							
Full power input bandwidth							
• Nominal bandwidth (NBW)				3.7		GHz	(1)
• Extended bandwidth (EBW)				5.2		GHz	
Gain flatness (+/- 0.5dB)							
• Nominal bandwidth (NBW)				850		MHz	
• Extended bandwidth (EBW)				900		MHz	
Input voltage standing wave ratio							
• Up to 2.4GHz		VSWR		1:1.35			
• Up to 5GHz				1:1.6			
DYNAMIC PERFORMANCE							
Noise Power Ratio at (600MHz noise bandwidth, 5MHz notch							
• 1st Nyquist zone				50		dB	
• 2nd Nyquist zone		NPR		48		dB	(2)
• 3rd Nyquist zone				46		dB	
• 4th Nyquist zone				TBD		dB	
Spurious Free Dynamic Range							
Fin = 100MHz, NBW							
• -1 dBFS				74		dBc	
• -3 dBFS				71		dBc	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
• -8 dBFS				66		dBc	
• -12 dBFS				66		dBc	
Fin = 1480MHz, NBW							
• -1 dBFS				61		dBc	
• -3 dBFS				63		dBc	
• -8 dBFS				64		dBc	
• -12 dBFS				68		dBc	
Fin = 1900MHz, NBW		SFDR					(3)
• -8 dBFS				62		dBc	
• -12 dBFS				67		dBc	
Fin = 2980MHz, EBW							
• -8 dBFS				50		dBc	
• -12 dBFS				55		dBc	
Fin = 3730MHz, EBW							
• -8 dBFS				45		dBc	
• -12 dBFS				49		dBc	
Fin = 5300MHz, out-of-band							
• -8 dBFS				TBD		dBc	
• -12 dBFS				TBD		dBc	
Fin = 1480MHz / -1dBFS, NBW							
• Over 50MHz band				TBD		dBc	
• Over 200MHz band				TBD		dBc	
3rd order intermodulation products Fin = 1425MHz +/- 5MHz / -7dBFS		IMD		TBD		dBc	(3)
Total harmonic distortion							
Output level -1dBFS							
• Fin = 100MHz, NBW				68		dBFS	
• Fin = 1480MHz, NBW				60		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW		THD		69		dBFS	(3)
• Fin = 1480MHz, NBW				67		dBFS	
• Fin = 1900MHz, NBW				65		dBFS	
• Fin = 2980MHz, EBW				58		dBFS	
• Fin = 3730MHz, EBW				52		dBFS	
• Fin = 5300MHz, out-of-band				TBD		dBFS	
Signal to Noise Ratio							
Output level -1dBFS							
• Fin = 100MHz, NBW				59		dBFS	
• Fin = 1480MHz, NBW				55		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW				60		dBFS	
• Fin = 1480MHz, NBW		SNR		59		dBFS	
• Fin = 1900MHz, NBW				57		dBFS	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
• Fin = 2980MHz, EBW				55		dBFS	
• Fin = 3730MHz, EBW				54		dBFS	
• Fin = 5300MHz, out-of-band				TBD		dBFS	
Signal to Noise And Distortion							
Output level -1dBFS							
• Fin = 100MHz, NBW				58		dBFS	
• Fin = 1480MHz, NBW				54		dBFS	
Output level -8dBFS							
• Fin = 100MHz, NBW		SINAD		59		dBFS	
• Fin = 1480MHz, NBW				58		dBFS	
• Fin = 1900MHz, NBW				57		dBFS	
• Fin = 2980MHz, EBW				53		dBFS	
• Fin = 3730MHz, EBW				50		dBFS	
• Fin = 5300MHz, out-of-band				TBD		dBFS	
Effective Number Of Bits							
Output level -1dBFS							
• Fin = 100MHz, NBW				9.2		bit	
• Fin = 1480MHz, NBW				8.5		bit	
Output level -8dBFS							
• Fin = 100MHz, NBW				9.5		bit	
• Fin = 1480MHz, NBW		ENOB		9.3		bit	
• Fin = 1900MHz, NBW				9.1		bit	
• Fin = 2980MHz, EBW				8.6		bit	
• Fin = 3730MHz, EBW				8.0		bit	
• Fin = 5300MHz, out-of-band				TBD		bit	
Noise Spectral density at -1dBFS							
• 1st Nyquist zone, NBW				-147		dBm/Hz	
• 2nd Nyquist zone, NBW				-144		dBm/Hz	
• 3rd Nyquist zone, EBW				-142		dBm/Hz	
• 4th Nyquist zone, EBW		NSD		-138		dBm/Hz	
Noise Spectral density at -8dBFS							
• 1st Nyquist zone, NBW				-148		dBm/Hz	
• 2nd Nyquist zone, NBW				-147		dBm/Hz	
• 3rd Nyquist zone, EBW				-146		dBm/Hz	
• 4th Nyquist zone, EBW				-144		dBm/Hz	

Notes: 1. Optimal bandwidth selection depends on signal characteristic; the bandwidth selection allows optimizing noise and linearity trade-off. For signal below 2.0GHz, the bandwidth selection must be set to nominal, for large signal beyond 2GHz the bandwidth selection must be set to extended. The extended bandwidth degrades noise floor up to 1dB, but brings lower signal attenuation with high frequency input

2. Due to the high bandwidth of the ADC, generating high performance and high loading factor to input to the ADC is a challenge. The values indicated in this table indicate the NPR value obtained at optimum loading factor value

3. Linearity at high frequency is dominated by low order odd harmonics (especially H3) and H2. Phase difference on the differential inputs should be reduced as much as possible to optimize the 2nd harmonic level. Stepping back 3 or 6 dB on input signal gives significant improvement on SFDR figures

3.6 Transient and switching characteristics

Unless otherwise specified:
- Typical values are given for typical supplies in dual-rail configuration (Refer to Table 18 in section Output selection for more information) at Tamb = +25°CBoth cores comply with the below specification when the OTP have been loaded
- Minimum and maximum values are given over corresponding temperature range for typical power supplies
- Values are specified at Fs = 1.5GSps for the serial mode and Fs = 1.3GSps for LVDS DMUX1:1 mode
- Values are given with SDA disabled

Table 9: Transient characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
ADC Code Error Rate at 1.5GSps (3GHz CLK)		CER		10^{-12}			(1)
ADC Code Error Rate at 1.25GSps (2.5GHz CLK)		CER		10^{-15}			(2)
Overvoltage Recovery Time		ORT		666		ps	

Notes: 1. Output error amplitude > 128 LSB (3% of the full-scale). At Fs = 1.5 GSps, ambient temperature.
2. Output error amplitude > 64 LSB (1.5% of the full-scale). At Fs = 1.25 GSps, ambient temperature.

Table 10: Switching characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
External clock frequency		F_{CLK}	400		3200	MHz	(1)
Sampling frequency for performance							
• DEMUX 1:1		$F_{S1:1}$	200 (TBC)		1300 (TBC)	MSps	(1)
• Serial ESIstream		F_{SSI}	200 (TBC)		1500	MSps	
Sampling frequency for operation							
• DEMUX 1:1		$F_{S1:1}$	200		1500	MSps	(1)
• Serial ESIstream		F_{SSI}	200		1600	MSps	
Aperture delay (SDA disabled)		T_A		TBD			
Aperture delay tuning range (SDA enabled)		T_A		TBD		ps	
SPI clock frequency		F_{SCLK}			30	MHz	
SPI reset duration		T_{RSTN}	10			µs	
Settling time at power-up		T_{PU}		TBD		µs	
LVDS OUTPUT							
Rise time for data (20-80%)		T_R		TBD		ps	(1), (2)
Fall time for data (20-80%)		T_F		TBD		ps	(1), (2)
Rise time for data ready (20-80%)		T_R		TBD		ps	(1), (2)
Fall time for data ready (20-80%)		T_F		TBD		ps	(1), (2)
Output data pipeline delay (latency)							
• Port high		T_{PDH}		22		T_{CLK}	(3)
• Port low		T_{PDL}		20		T_{CLK}	
Output data propagation delay		T_{OD}		TBD		ns	(3)
Output data to data ready delay		T_{D1}		TBD		T_{CLK}	(3)
Output data ready to data delay		T_{D2}		TBD		T_{CLK}	(3)
Output data ready A to data ready B skew		T_{DRsk}		TBD		ps	

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
SYNC to data ready pipeline delay							
• DEMUX 1:1		T_{RDR}		26		T_{CLK}	(4)
• DEMUX 1:2		T_{RDR}		27		T_{CLK}	
SYNC pulse width		T_{SYNC}	16			T_{CLK}	
SYNC to SYNCO pipeline delay		T_{PS}		TBD		T_{CLK}	
SYNC to SYNCO propagation delay		T_{ODS}		TBD		ps	
SYNC signal valid timing		T_1 T_2		TBD TBD		ps ps	(5)
Trigger data pipeline delay							
• Port high		T_{PDH}		TBD		T_{CLK}	
• Port low		T_{PDL}		TBD		T_{CLK}	
TRIG propagation delay		T_{ODT}		TBD		ns	
CML OUTPUT (Serial ESIstream)							
Data rate		DR_{HSSL}	3.2	$2xF_{clk}$	6	Gbps	
Rise time for data (20-80%)		T_R		TBD		ps	(2)
Fall time for data (20-80%)		T_F		TBD		ps	(2)
Output data pipeline delay (latency)		T_{PDS}	48		52	T_{CLK}	(6)
Output data propagation delay		T_{ODS}		TBD		ps	(6)
SYNC to synchronization sequence		T_{SS}		TBD		ps	(7)

Notes: 1. Performances only guaranteed at 1.5GSps max in serial ESIstream mode and 1.3GSps max in DEMUX 1:1 mode
2. Simulated with 50Ω lines modeled by 2.5nH in parallel with 1pF
3. Refer to timing diagrams in Figure 3
4. Refer to timing diagram in Figure 5
5. Refer to timing diagram in Figure 7. T_1 and T_2 correspond to setup and hold times of the SYNCTRIG input seen at the package input.
6. Refer to timing diagram in Figure 4
7. Refer to timing diagram in Figure 6

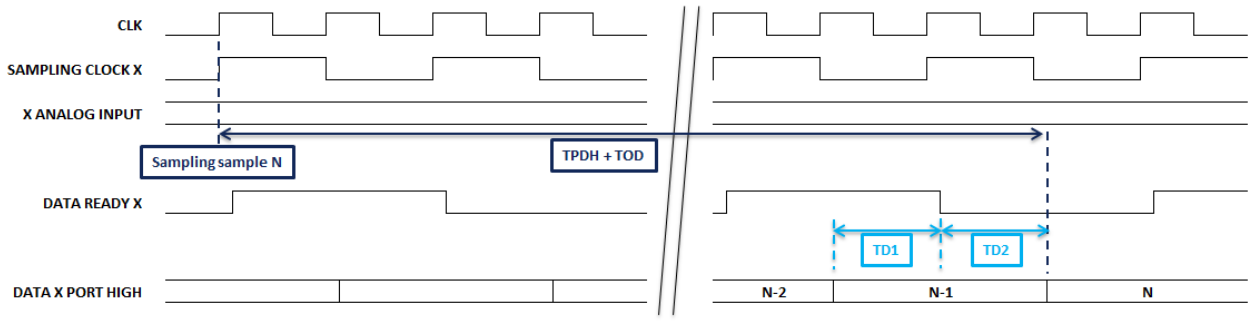


Figure 3: Timing diagram in DEMUX 1:1

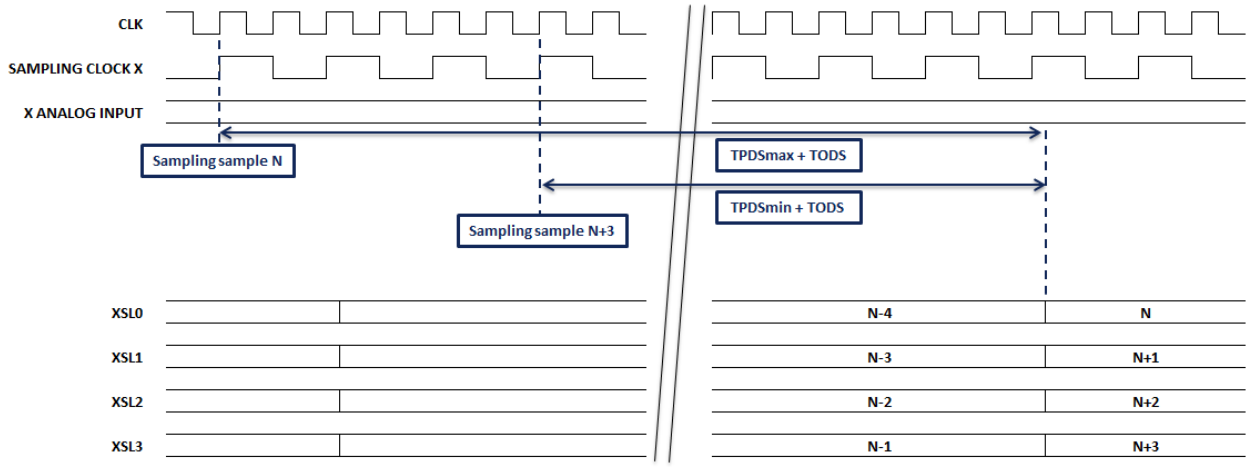


Figure 4: Timing diagram in serial ESIstream

For both figure 3 and 4, X represents either channel A or B. If channel A and B are interleaved, the internal sampling clocks of channel A and B are in opposition and their output data and data ready are delayed by 1 external CLK cycle.
For Figure 4, the output data XSLN are encoded through ESIstream (see section Serial ESIstream for more information).

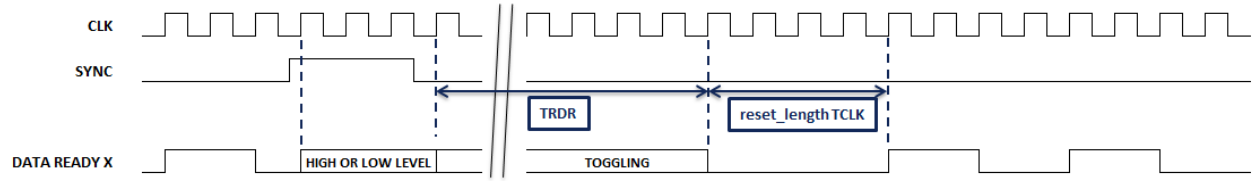


Figure 5: SYNC timing diagram in DEMUX 1:1

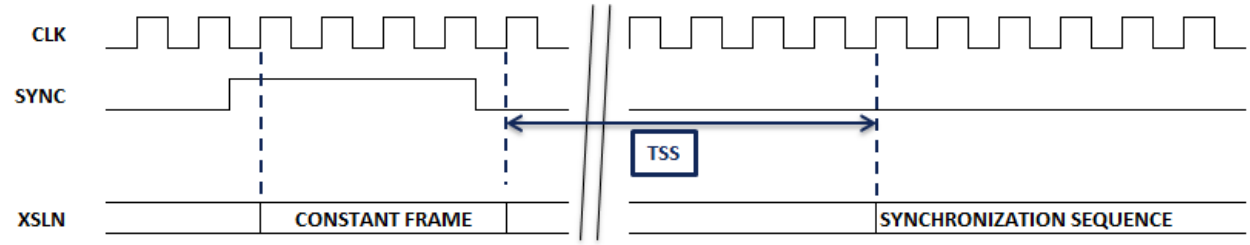


Figure 6: SYNC timing diagram in serial ESIstream

XSLN corresponds to any serial output (X = A or B and N = [0..3]).

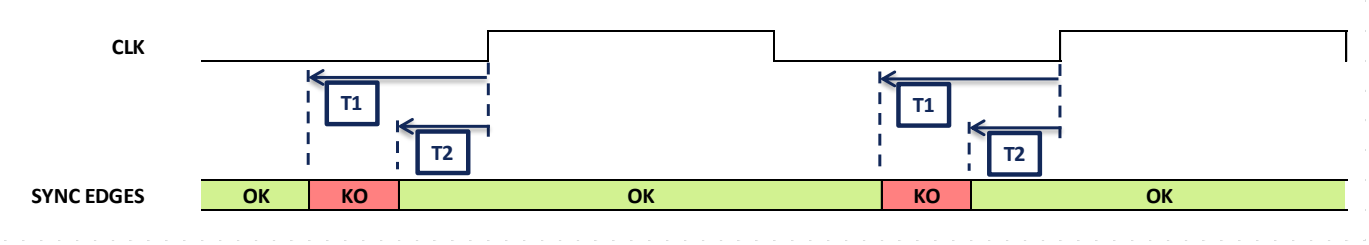


Figure 7: SYNC edges forbidden zone

Notes: The timing diagram assumes that bit ESEL in register SYNC control is at '0'. If ESEL = '1', T1 and T2 have to be referenced to the falling edge of CLK. See section SYNCTRIG input for more information.

Table 11: SPI switching characteristics

Parameter	Test level	Symbol	Value			Unit	Note
			Min	Typ	Max		
RSTN pulse length		T_{RSTN}	10			µs	
SCLK frequency		F_{SCLK}			30	MHz	
CSN to SCLK delay		$T_{CSN-SCLK}$	0.5			T_{SCLK}	(1)
MISO setup time		T_{setup}	3			ns	(1)
MISO hold time		T_{hold}	3			ns	(1)
MOSI output delay		T_{delay}			TBD	ns	(1)

Notes: 1. Refer to timing diagram in Figure 8.

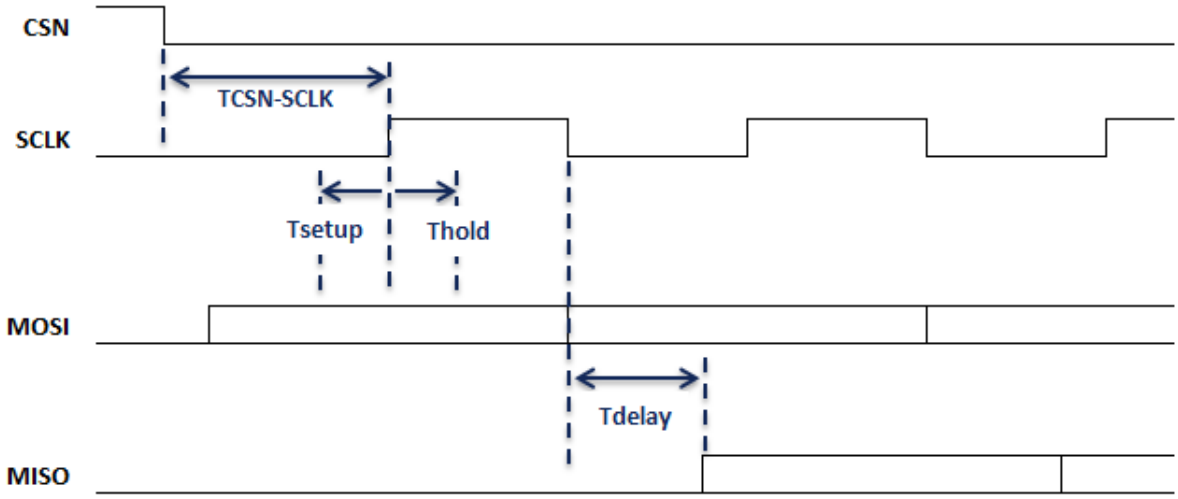


Figure 8: SPI timing diagram

3.7 Digital output coding

Table 12: ADC digital output coding table

Differential analog input	Voltage level	Binary MSB (bit 11).....LSB(bit 0)	In-range
> + 500.125 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	0
+ 500.125 mV + 500 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 1
+ 0.125 mV - 0.125 mV	Mid-scale + ½ LSB Mid-scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	1 1
- 500 mV -500.125 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	1 1
< - 500.125 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	0

3.8 Definition of terms

Table 13: Definition of terms

Abbreviation	Term	Definition
CER	*Code Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate.
DNL	*Differential non-linearity*	The Differential Non Linearity for an output code "i" is the difference between the measured step size of code "i" and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification higher than -1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
ENOB	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the input amplitude and FS is the full scale range of the ADC under test.
FPBW	*Full Power Input Bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at -1dBFS (Full scale – 1dB).
IMD	*Intermodulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
INL	*Integral non-linearity*	The Integral Non Linearity for an output code "i" is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
JITTER	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
LF	*Loading Factor*	The loading factor is 20log(1/k), where k is the rms value of the broadband signal. This parameter relates to the NPR measurement. The optimum loading factor for a 12bits converter is k = 5 corresponding to a loading factor of -14dBFS.
NPR	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
NSD	*Noise Spectral Density*	The NSD is the power spectral density magnitude of the ADC expressed in dBm/Hz.
ORT	*Overvoltage Recovery Time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
OTP	*One Time Programmable*	OTP are fuses used to set circuit default configuration and calibrations.
SFDR	*Spurious Free Dynamic Range*	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SINAD	*SIgnal to Noise And Distortion ratio*	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SNR	*Signal to Noise Ratio*	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the 25th first harmonics. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
T1, T2	*SYNC forbidden zone*	T1 and T2 represents setup and hold time on the SYNC input brought back to the input of the package.
TA	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (XAI, XAIN where X = A, B) is sampled.
TF	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between high level and low level.

Abbreviation	Term	Definition
THD	*Total Harmonic Distortion*	Ratio expressed in dB of the RMS sum up to 25th harmonic components, to the RMS input signal amplitude. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
TOD	*Digital data output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
TPD	*Pipeline delay / latency*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking into account TOD).
TR	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
TRDR	*Data ready reset delay*	Delay between the edge of the external clock after reset (SYNC, SYNCN) and the reset to digital zero transition of the data ready output signal (XDR, where X = A, B).
TS	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when an 80% Full Scale step function is applied to the differential analog input.
TSYNC	*SYNC duration*	External SYNC pulse width needed for SYNC function.
VSWR	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e. 99% power transmitted and 1% reflected).

4 Package description

Ceramic Ball Grid Array CBGA255
Body size: 14mmx14mm
Substrate type: HiTCE® High Temperature Coefficient Expansion
Pitch: 0.8mm
Pins count: 255

4.1 Package Drawings

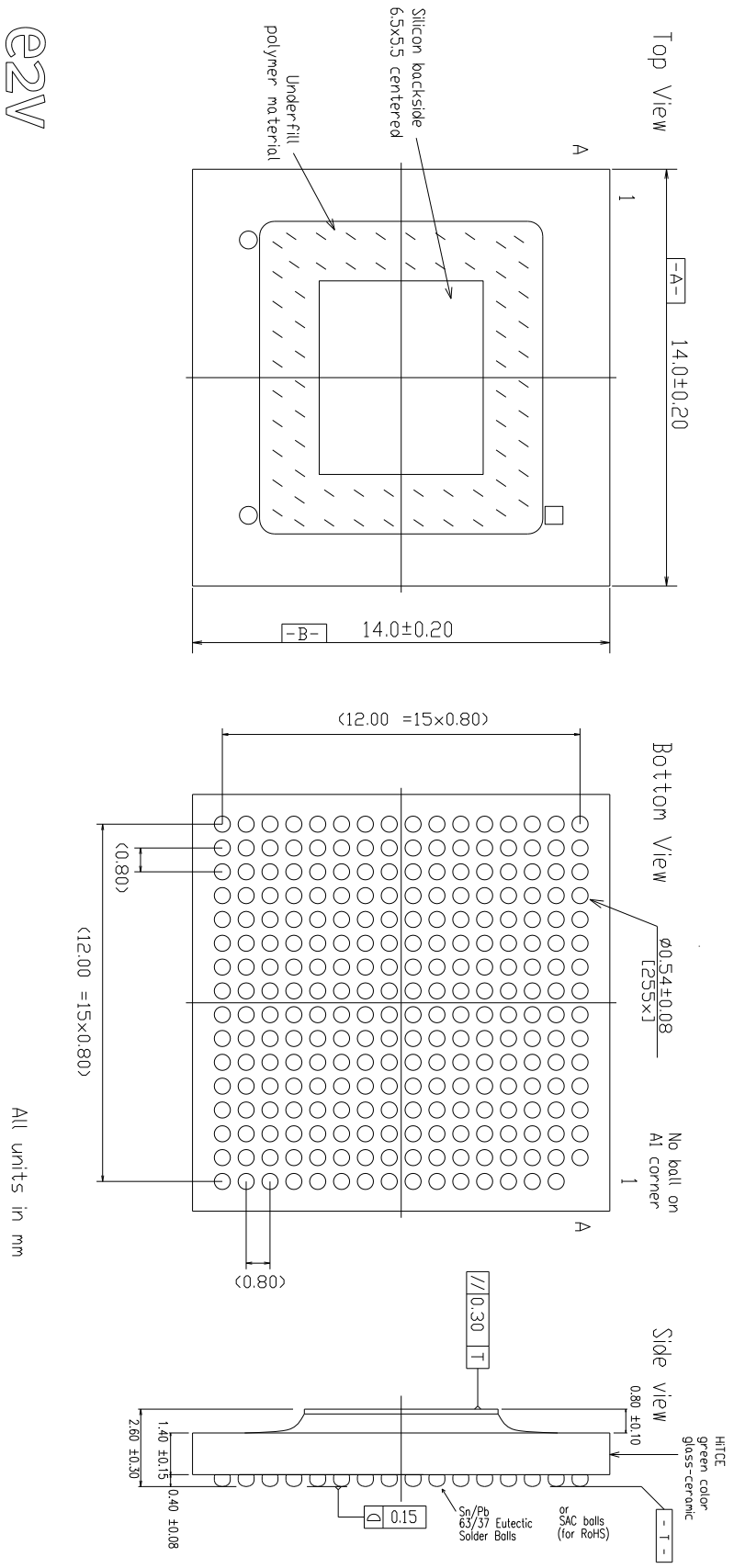


Figure 9: Package drawings

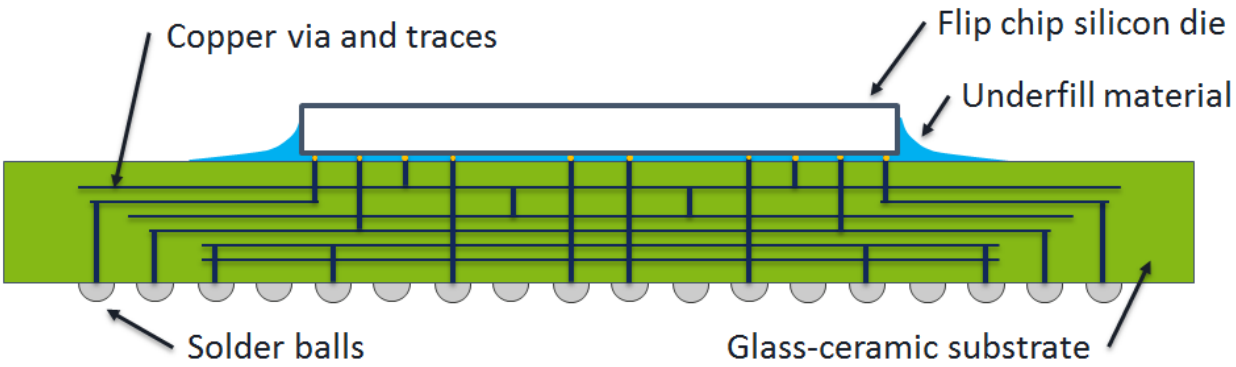


Figure 10: Package cross-section

4.2 Thermal characteristics

Table 14: Package thermal characteristic

Parameter	Symbol	Value		Unit
		In LVDS interface	In serial interface	
Thermal Resistance	$\Theta_{Junction\text{-}Bottom\ of\ balls}$	10.5	10	°C/Watt
Thermal Resistance	$\Theta_{Junction\text{-}top\ of\ die}$ (1)	3.3	3	°C/Watt
Thermal Resistance	$\Theta_{Junction\text{-}Ambient}$ (2)	TBD	TBD	°C/Watt
Delta Temp Hot Spot - Vdiode		+11,4	+11.4	°C

Notes: Thermal resistances are calculated from hot spot, not from average temperature

1. Infinite heat sink at top of die.
2. Typical Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 × 76.2 mm, 1.6 mm thickness

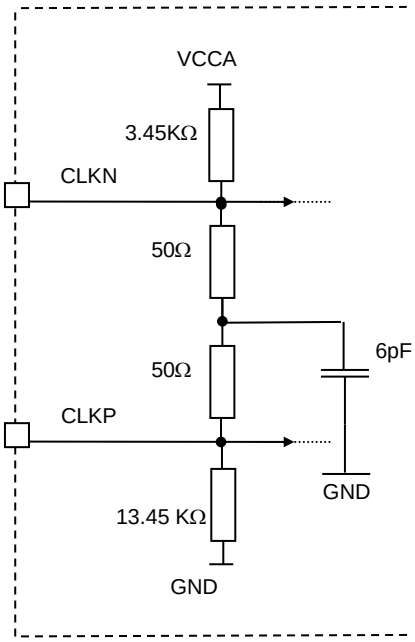
4.3 Pinout top view

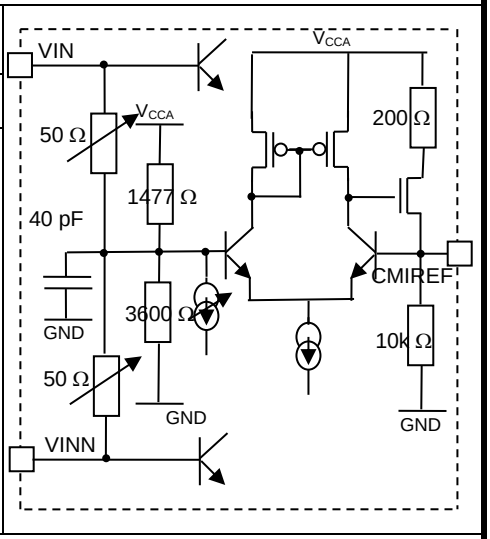
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		AGND	AGND	AGND	AINN	AINP	AGND	AGND	AGND	AGND	BINP	BINN	AGND	AGND	AGND	AGND	A
B	SYNCTRIGP	SYNCTRIGN	AGND	AGND	AGND	AGND	AGND	CLKN	CLKP	AGND	AGND	AGND	AGND	AGND	DIODE_C	DIODE_A	B
C	SSOP	SSON	AGND	AGND	CMIREFA	AGND	AGND	AGND	AGND	AGND	AGND	CMIREFB	AGND	AGND	SYNCON	SYNCOP	C
D	AH11P	AH11N	AFU1P	AFU1N	AGND	AGND	VCCA	AGND	AGND	VCCA	AGND	AGND	BFU1N	BFU1P	BH11N	BH11P	D
E	AH8P	AH8N	AH10P	AH10N	GNDIO	VCCIOH1A	AGND	VCCA	VCCA	AGND	VCCIOH1B	GNDIO	BH10N	BH10P	BH8N	BH8P	E
F	AH6P	AH6N	AH7P	AH7N	GNDIO	VCCIOH2A	VCCA	AGND	AGND	VCCA	VCCIOH2B	GNDIO	BH7N	BH7P	BH6N	BH6P	F
G	AH4P	AH4N	AH9P	AH9N	GNDIO	VCCIOH1A	VCCA	AGND	AGND	VCCA	VCCIOH1B	GNDIO	BH9N	BH9P	BH4N	BH4P	G
H	AH2P	AH2N	AH5P	AH5N	GNDIO	VCCIOH2A	VCCA	AGND	AGND	VCCA	VCCIOH2B	GNDIO	BH5N	BH5P	BH2N	BH2P	H
J	AH0P	AH0N	AH3P	AH3N	GNDIO	VCCIOH1A	VCCA	VCCD	GNDD	VCCA	VCCIOH1B	GNDIO	BH3N	BH3P	BH0N	BH0P	J
K	ADRP	ADRN	AH1P	AH1N	GNDIO	VCCIOS2A	VCCIOH2A	GNDD	VCCD	VCCIOH2B	VCCIOS2B	GNDIO	BH1N	BH1P	BDRN	BDRP	K
L	GNDIO	GNDIO	AFU2P	AFU2N	GNDIO	VCCIOS1A	VCCIOS2A	VCCIOS1A	VCCIOS1B	VCCIOS2B	VCCIOS1B	GNDIO	BFU2N	BFU2P	GNDIO	GNDIO	L
M	ASL3P	ASL3N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BSL3N	BSL3P	M
N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	MOSI	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	N
P	ASL2P	ASL2N	GNDIO	GNDIO	GNDIO	GNDIO	TESTA	SCLK	SCAN	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BSL2N	BSL2P	P
R	GNDIO	GNDIO	ASL1N	GNDIO	ASL0N	GNDIO	VCCFUSEC	CSN	MISO	RSTN	GNDIO	BSL0N	GNDIO	BSL1N	GNDIO	GNDIO	R
T	GNDIO	GNDIO	ASL1P	GNDIO	ASL0P	GNDIO	GNDIO	GNDIO	VCCFUSEB	VCCFUSEA	GNDIO	BSL0P	GNDIO	BSL1P	GNDIO	GNDIO	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

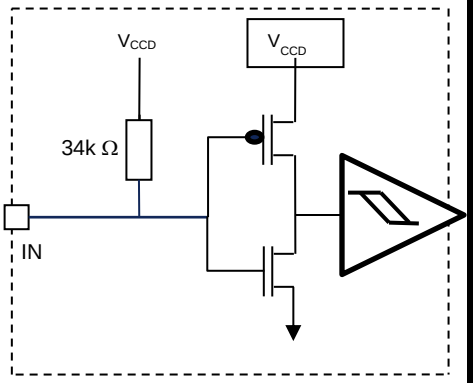
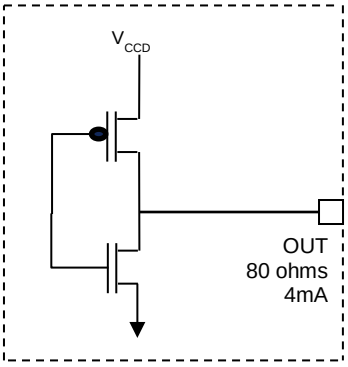
Figure 11: Pinout top view

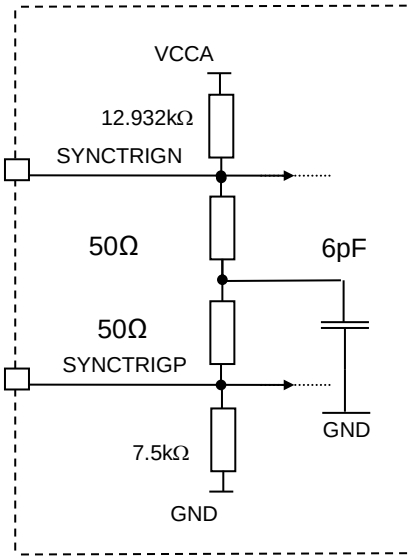
4.4 Pinout table

Table 15: Pinout table

Pin label	Pin number	Description	I/O	Simplified electrical schematics
Power supplies				
AGND	A2, A3, A4, A7, A8, A9, A10, A13, A14, A15, A16, B3, B4, B5, B6, B7, B10, B11, B12, B13, B14, C3, C4, C6, C7, C8, C9, C10, C11, C13, C14, D5, D6, D8, D9, D11, D12, E7, E10, F8, F9, G8, G9, H8, H9	Analog ground		
VCCA	D7, D10, E8, E9, F7, F10, G7, G10, H7, H10, J7, J10	Analog power supply		
GNDD	J9, K8	Digital ground		
VCCD	J8, K9	Digital power supply		
GNDIO	E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L1, L2, L5, L12, L15, L16, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, N1, N2, N3, N4, N5, N6, N7, N8, N10, N11, N12, N13, N14, N15, N16, P3, P4, P5, P6, P10, P11, P12, P13, P14, R1, R2, R4, R6, R11, R13, R15, R16, T1, T2, T4, T6, T7, T8, T11, T13, T15, T16	I/O ground		
VCCIOH1	E6, E11, G6, G11, J6, J11	Output power supply for LVDS port high		
VCCIOH2	F6, F11, H6, H11, K7, K10	Output power supply for LVDS port high		
VCCIOS1	L6, L8, L9, L11	Output power supply for serial ESIstream		
VCCIOS2	K6, K11, L7, L10	Output power supply for serial ESIstream		
Clock				
CLKP CLKN	B8, B9	Input clock signal	I	

Pin label	Pin number	Description	I/O	Simplified electrical schematics
Analog signals				
AINP AINN	A6, A5	Analog input for ADC A	I	
BINP BINN	A11, A12	Analog input for ADC B	I	
CMIREFA CMIREFB	C5, C12	Input signal common mode reference for A and B cores. In AC coupling operation this output must be left floating (not used) In DC coupling operation, these pins provide an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	
Digital output (LVDS) – Disabled in serial ESIstream				
AH0P, AH0N AH1P, AH1N AH2P, AH2N AH3P, AH3N AH4P, AH4N AH5P, AH5N AH6P, AH6N AH7P, AH7N AH8P, AH8N AH9P, AH9N AH10P, AH10N AH11P, AH11N	J1, J2 K3, K4 H1, H2 J3, J4 G1, G2 H3, H4 F1, F2 F3, F4 E1, E2 G3, G4 E3, E4 D1, D2	High port channel A output data AH0 is the LSB, AH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O	
AFU1P, AFU1N	D3, D4	Channel A control bit 1	O	
AFU2P, AFU2N	L3, L4	Channel A control bit 2	O	
ADRP, ADRN	K1, K2	Channel A data ready	O	
BH0P, BH0N BH1P, BH1N BH2P, BH2N BH3P, BH3N BH4P, BH4N BH5P, BH5N BH6P, BH6N BH7P, BH7N BH8P, BH8N BH9P, BH9N BH10P, BH10N BH11P, BH11N	J16, J15 K14, K13 H16, H15 J14, J13 G16, G15 H14, H13 F16, F15 F14, F13 E16, E15 G14, G13 E14, E13 D16, D15	High port channel B output data BH0 is the LSB, BH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O	
BFU1P, BFU1N	D14, D13	Channel B control bit 1	O	
BFU2P, BFU2N	L14, L13	Channel B control bit 2	O	
BDRP, BDRN	K16, K15	Channel B data ready	O	
Digital output (CML) – Disabled in parallel LVDS				
ASL0P, ASL0N	T5, R5	Channel A serial link output 0	O	
ASL1P, ASL1N	T3, R3	Channel A serial link output 1	O	
ASL2P, ASL2N	P1, P2	Channel A serial link output 2	O	

Pin label	Pin number	Description	I/O	Simplified electrical schematics
ASL3P, ASL3N	M1, M2	Channel A serial link output 3	O	
BSL0P, BSL0N	T12, R12	Channel B serial link output 0	O	
BSL1P, BSL1N	T14, T14	Channel B serial link output 1	O	
BSL2P, BSL2N	P16, P15	Channel B serial link output 2	O	
BSL3P, BSL3N	M16, M15	Channel B serial link output 3	O	
Digital output (LVDS)				
SSOP, SSON	C1,C2	Slow Synchronization Output clock	O	
SYNCOP, SYNCON	C16, C15	Synchronization output signal	O	
SPI digital I/0 (CMOS)				
CSN	R8	Chip Select signal (active low) Internal pull-up	I	
SCLK	P8	SPI clock Internal pull-up	I	
MOSI	N9	SPI Master Out Slave In Internal pull-up	I	
RSTN	R10	SPI asynchronous reset (active low) Internal pull-up	I	
MISO	R9	SPI Master In Slave Out	O	
DIGITAL INPUT (LVDS)				

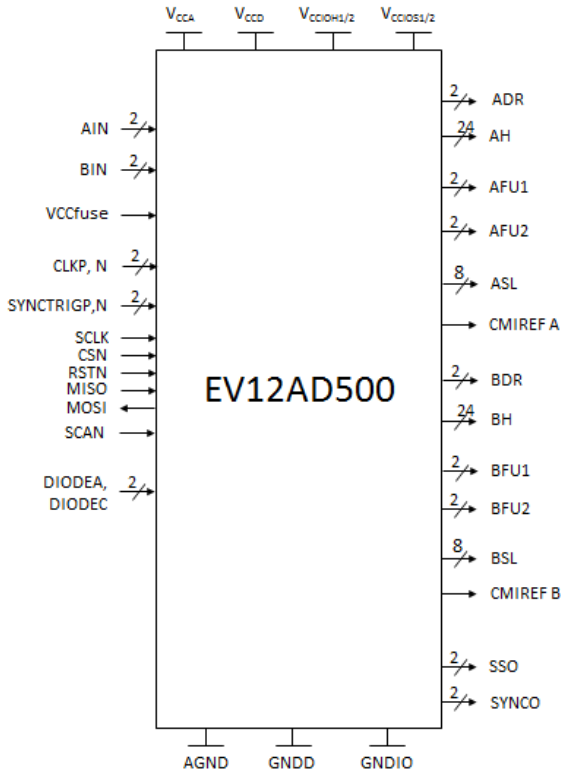
Pin label	Pin number	Description	I/O	Simplified electrical schematics
SYNCTRIGP SYNCTRIGN	B1, B2	Differential input synchronization or trigger signal (LVDS) Active high signal	I	
Miscellaneous				
scan	P9	RESERVED PIN **Must be pulled-down with 10kΩ**		
TESTA	P7	RESERVED PIN **Should be left unconnected**		
VCCFuseA, VCCFuseB, VCCFuseC	T10 T9 R7	RESERVED PIN **Should be left unconnected**		
DiodeA, DiodeC	B16 B15	Junction temperature monitoring diode anode and cathode	I	

5 Theory of operation

5.1 Overview

Table 16: Functional description

Name	Function
V_{CCA}	Analog power supply
V_{CCD}	Digital power supply
AGND	Analog ground
GNDD	Digital ground
$V_{CCIOH1/2}$ $V_{CCIOS1/2}$	Output buffers power supplies
GNDIO	Ground for output buffers
AINP, AINN	Analog input for ADC core A
BINP, BINN	Analog input for ADC core B
CLKP,CLKN	Differential clock input
[AH0P:AH11P] [AH0N:AH11N]	High port channel A output data (inactive in serial ESIstream)
AFU1P, AFU1N	Channel A control bit 1
AFU2P, AFU2N	Channel A control bit 2
ADRP, ADRN	Channel A data ready
[BH0P:BH11P] [BH0N:BH11N]	High port channel B output data (inactive in serial ESIstream)
BFU1, BFU1N	Channel B control bit 1
BFU2, BFU2N	Channel B control bit 2
BDRP, BDRN	Channel B data ready
[ASL0P:ASL3P] [ASL0N:ASL3N]	Channel A serial output data (inactive in LVDS DEMUX 1:1)
[BSL0P:BSL3P] [BSL0N:BSL3N]	Channel B serial output data (inactive in LVDS DEMUX 1:1)



CSN	SPI chip select input (active low)	SYNCTRIGP, SYNCTRIGN	Differential input synchronization or trigger signal (LVDS)
RSTN	SPI asynchronous reset input (active low)		
SCLK	SPI input clock	SYNCOP, SYNCON	Synchronization output signal
MOSI	SPI Master Out Slave In	SSOP, SSON	Slow Synchronization Output clock
MISO	SPI Master In Slave Out	CMIRefA CMIRefB	Output voltage for input common mode reference of ADC A and B
DIODEA, DIODEC	Diode anode and cathode inputs for die junction temperature monitoring	TESTA	RESERVED PIN Should be left unconnected
SCAN	RESERVED PIN Must be pulled-down with 10kΩ	VCCfuse	RESERVED PIN Should be left unconnected

5.2 Digital Reset and start up procedure

RSTN is an asynchronous active low global reset for the SPI and OTP (One Time Programmable Registers). It is mandatory to put RSTN at low level during a minimum of 10µs at power-up of the device. It sets all SPI registers to their default values.
The SPI interface can be used or not; if it is not used, the OTP value and default SPI configurations will be automatically loaded (see section Using the SPI interface and Without using the SPI interface for more information).

5.2.1 Using the SPI interface

Figure 11 presents the reset and synchronization to realize after power-up when the SPI interface is used (see section Serial Peripheral Interface for more information on the SPI interface).

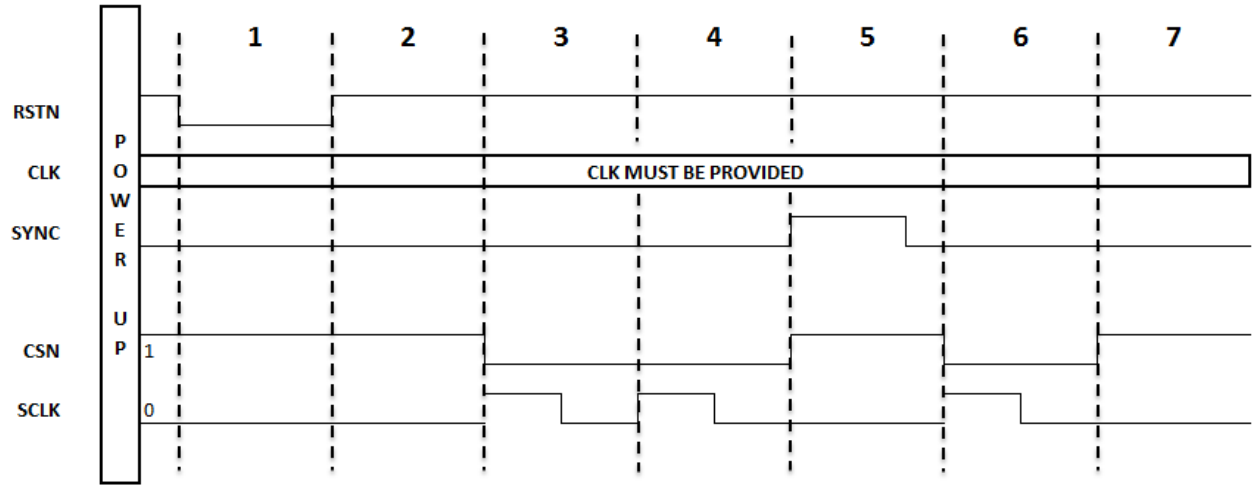


Figure 12: Start-up sequence when using the SPI interface

1. It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least 10µs. During the RSTN pulse, CSN must be held high and SCLK held low. The CLK must be provided before the RSTN pulse. The CLK can start before or after the power-up;
2. The fuses need 1ms to wake up;
3. The SPI instruction WRITE @0x7E 0x0001 must be sent to the ADC. The OTP are loaded into the SPI registers at this point. There must be at least 1ms between the RSTN pulse and this SPI instruction;
4. The ADC is configured through the SPI interface;
5. A pulse is applied onto the SYNCTRIG input to reset the internal clocks (SYNC signal in Figure 12). At this stage the bit 7 of register chip control must be at '0' (trigger mode disabled) – see section SYNCTRIG input;
6. The ADC can be configured in trigger mode enable and the EXTRA_SEE_PROTECT register can be activated – see section Extra SEE protect;
7. Normal operation of the ADC.

5.2.2 Without using the SPI interface

The figure below presents the reset and synchronization to realize after power-up of the device when the SPI interface is not used. In this case, the configuration of the ADC cannot be changed and corresponds to the SPI default values (refer to Register mapping and default configuration). Due to the internal pull-up of the SPI inputs, this is the default mode when the SPI inputs are floating.

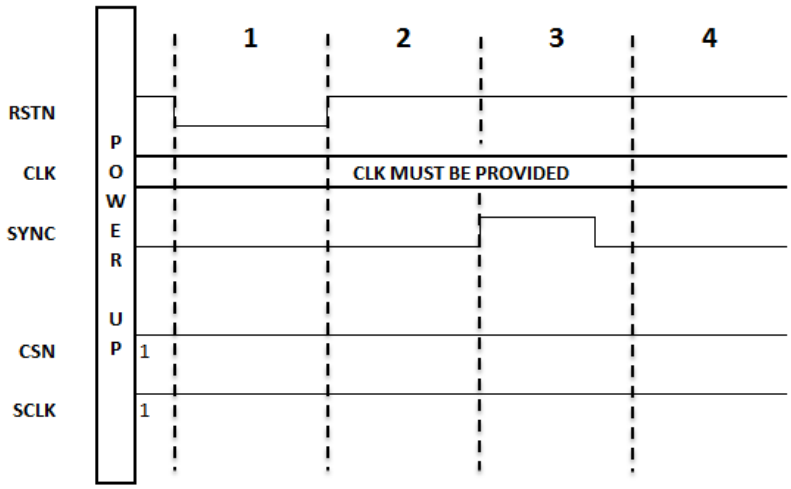


Figure 13: Start-up sequence when the SPI interface is not used

1. It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least 10µs. During the RSTN pulse, CSN must be held high and SCLK held high. The CLK must be provided before the RSTN pulse. It can start either before or after the power-up;
2. The fuses need 1ms to wake up;
3. A pulse is applied onto the SYNCTRIG input to reset the internal clocks (SYNC signal in Figure 13) ;
4. Normal operation of the ADC.

Refer to section Register mapping and default configuration for more information on the ADC configuration when the SPI interface is not used.

5.3 Serial Peripheral Interface

5.3.1 SPI Characteristics

The SPI interface uses the 5 following input/output signals:
- RSTN: asynchronous reset active low;
- SCLK: SPI clock;
- CSN: chip select active low;
- MISO: Master In Slave Out;
- MOSI: Master Out Slave In.

And is a standard SPI with:
- 8 address bits from the MSB A[7] to A [0], with A[7] being the R/W bit;
- 16 data bits from the MSB D[15] to D[0]

The MOSI sequence should start (A[7] bit) with ‘0’ for a read procedure and ‘1’ for a write procedure.

The following diagrams (Figure 13 and 14) show a write and read procedure address and data sequencing. For more information on the timing between signals refer to Figure 7.

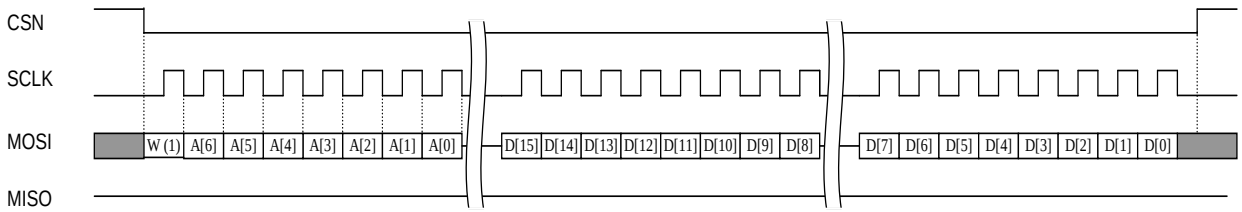


Figure 14: SPI write procedure

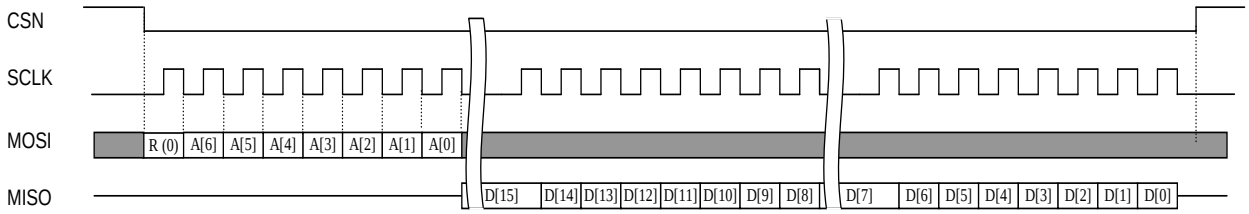


Figure 15: SPI read procedure

5.3.2 Register mapping and default configuration

Table 17: Register mapping

Address	Register	Access	Bit	Default value	Description	Refer to section
0x01	CHIP_ID	R	[15..0]		Chip ID	
0x02	S_N	R	[15..0]		Chip serial number	
0x04	CHIP_CTRL	W/R	[15..10]	0x00	Reserved	
			9	0b1	Serial output swing adjust 1: reduced swing 0: full swing	
			8	0b0	SSO and SYNCO swing adjust 1: full swing 0: reduced swing	5.9
			7	0b0	Trigger enable 1: enabled 0: disabled	5.5.1; 5.6.2
			6	0b0	LVDS swing adjust 1: full swing 0: reduced swing	5.5.2
			5	0b1	Bandwidth selection 1: nominal 0: extended	5.7.2
			4	0b1	Reserved	
			3	0b0	Temperature calibration selection 1: Cold temperature 0: Hot temperature	5.10
			2	0b0	Reserved	
			1	0b0	Reserved	

Address	Register	Access	Bit	Default value	Description	Refer to section
			0	0b1	Clock interleaved 1: enabled 0: disabled	5.12.1
0x1E	A_CMIREF	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input common mode trimming for channel A	5.7.3
0x1F	A_RIN	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input impedance trimming for channel A	5.7.1
0x20	A_SDA_CTRL	W/R	[15..13]	0x0	Reserved	
			12	0b1	SDA control for channel A 0: enabled 1: disabled	5.13
			[11..10]	0b00	Reserved	
			[9..0]	0x000	SDA value for channel A	5.13
0x21	A_GAIN_CAL	W/R	[15..10]	0x00	Reserved	
			[9..0]	0x0200	Interleaving gain calibration for channel A	5.12.2
0x22	A_PHASE_CAL	W/R	[15..8]	0x00	Reserved	
			[7..0]	0x80	Interleaving phase calibration for channel A	5.12.2
0x23	A_OFFSET_CAL	W/R	[15..9]	0x00	Reserved	
			[8..0]	0x0100	Interleaving offset calibration for channel A	5.12.2
0x3D	B_CMIREF	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input common mode trimming for channel B	5.7.3
0x3E	B_RIN	W/R	[15..5]	0x000	Reserved	
			[4..0]	0x10	Input impedance trimming for channel B	5.7.1
0x3F	B_SDA_CTRL	W/R	[15..13]	0x00	Reserved	
			12	0b1	SDA control for channel B 0: enabled 1: disabled	5.13
			[11..10]	0b00	Reserved	
			[9..0]	0x000	SDA value for channel B	5.13
0x40	B_GAIN_CAL	W/R	[15..10]	0x00	Reserved	
			[9..0]	0x0200	Interleaving gain calibration for channel B	5.12.2
0x41	B_PHASE_CAL	W/R	[15..8]	0x00	Reserved	
			[7..0]	0x80	Interleaving phase calibration for channel B	5.12.2
0x42	B_OFFSET_CAL	W/R	[15..9]	0x00	Reserved	
			[8..0]	0x0100	Interleaving offset calibration for channel B	5.12.2
			[15..14]	0b00	Reserved	
			13	0b0	Serial link 3 standby 1: enabled 0: disabled	5.14
			12	0b0	Serial link 2 standby 1: enabled 0: disabled	5.14

Address	Register	Access	Bit	Default value	Description	Refer to section
0x62	STDBY	W/R	11	0b0	Serial link 1 standby 1: enabled 0: disabled	5.14
			10	0b0	Serial link 0 standby 1: enabled 0: disabled	5.14
			[9..6]	0x0	Reserved	
			5	0b0	Channel B analog standby 1: enabled 0: disabled	5.14
			4	0b0	Channel A analog standby 1: enabled 0: disabled	5.14
			[3..2]	0b00	Reserved	
			1	0b0	Channel B full standby 1: enabled 0: disabled	5.14
			0	0b0	Channel A full standby 1: enabled 0: disabled	5.14
0x63	LVDS_PRBS_CTRL	W/R	[15..2]	0x0000	Reserved	
			[1..0]	0b00	PRBS on LVDS output 00: data only 01: data xor PRBS 11: PRBS only	5.5.3
0x64	CTRL_BIT_CFG	W/R	[15..4]	0x000	Reserved	
			[3..2]	0b00	XFU2 selection: 00: In-range 01: Parity bit 10: Trigger	5.5.1
			[1..0]	0b00	**If OUT_SEL = '1' (LVDS DEMUX 1:1)** XFU1 selection: 00: in-range 01: parity bit 10: trigger **If OUT_SEL = '0' (Serial interface)** ***Bit 1 – CB2 selection:*** 0: timestamp 1: trigger ***Bit 0 - CB1 selection:*** 0: in-range 1: parity	5.5.1 5.6.2
0x66	TEST_MODE	W/R	[15..5]	0x000	Reserved	
			4	0b0	Ramp 1: enabled 0: disabled	5.5.4

Address	Register	Access	Bit	Default value	Description	Refer to section
			3	0b0	Flash 1: enabled 0: disabled	5.5.4
			[2..1]	0b00	Reserved	
			0	0b0	Test mode 1: enabled 0: disabled	5.5.4
0x67	FLASH_RST_LENGTH	W/R	[15..12]	0x0	Reserved	
			[11..6]	0x10	Number of clock cycle when data ready is driven low after a SYNC	5.8
			[5..0]	0x18	Flash pattern length	5.5.4
0x68	OUT_SEL	W/R	[15..1]	0x0000	Reserved	
			1	0b0	Output selection 0: LVDS DEMUX 1:1 1: Serial interface	
			0	0b0	Reserved	5.4
0x69	A_CALC_CRC	R	[15..0]		CRC value for channel A	5.11.2
0x6A	B_CALC_CRC	R	[15..0]		CRC value for channel B	5.11.2
0x74	SYNC_CTRL	W/R	[15..1]	0x0000	Reserved	
			0	0b0	Edge selection for SYNC recovery 1: Clock falling edge 0: Clock rising edge	5.8
0x76	A_CAL_CRC2	R	16		CRC channel A hot temperature calibration	5.11.2
0x77	A_CAL_CRC1	R	16		CRC channel A cold temperature calibration set 1	5.11.2
0x78	B_CAL_CRC2	R	16		CRC channel B hot temperature calibration set 2	5.11.2
0x79	B_CAL_CRC1	R	16		CRC channel B cold temperature calibration set 1	5.11.2
0x7E	LOAD_CAL	W	[15..1]	0x0000	Reserved	
			0		Load calibration when written 1	5.10
0x7F	EXTRA_SEE_PROTECT	W/R	[15..0]	0x0000	Reserved	
			0	0	SE protect 1: enabled 0: disabled	5.11.1

5.4 Output selection

The output of the ADC can be configured either as a LVDS DEMUX 1:1 or serial interface using the ESIstream protocol through the SPI register OUT_SEL at address 0x68:

OUT_SEL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
														OUT_SEL	

Setting OUT_SEL to "0" configures the output in DEMUX 1:1, which is the default configuration. Setting it to "1" configures the output in serial interface.

When in DEMUX 1:1, the serial interface output should be grounded.
When in serial interface, the LVDS output should be grounded.

Depending on the output mode of interest, the supplies should be configured as follows:

Table 18: Power supplies configuration

		Single rail	Dual rail	
		DMUX 1:1	DMUX 1:1	Serial
Analog supply	VCCA	3.4V	3.4V	
	AGND	GND	GND	
Digital supply	VCCD	3.4V	2.5V	
	DGND	GND	GND	
I/O Supplies	VCCIOH1	3.4V	2.5V	GND
	VCCIOH2	3.4V	3.4V	GND
	VCCIOS1	GND	GND	2.5V
	VCCIOS2	GND	GND	3.4V
	GNDIO	GND	GND	

Note: In dual-rail configuration, the power consumption is reduced
Single-rail configuration is not available in serial interface

5.5 DEMUX 1:1

5.5.1 Control bit XFU1 and XFU2

Three different control bits can be output on XFU1 and XFU2 in DEMUX 1:1: in-range, parity or trigger. The configuration of the control bits is done through the register LVDS_CFG selection at address 0x64:

LVDS_CFG															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
												XFU2_SEL		XFU1_SEL	

XFU1 and XFU2 control bits are set for both channels. All control bits are output at the same time as the sample they control.

5.5.1.1 IN-RANGE

The in-range control bit output '1' when the ADC input is not saturated and '0' when it is. To set XFUn as the in-range, XFUn_SEL must be set to "00".

5.5.1.2 PARITY BIT

The parity bit is a XOR between the 12 bits of the sample. To set XFUn as the parity, XFUn_SEL must be set to "01".

5.5.1.3 TRIGGER

The trigger bit is a copy of the SYNCTRIG input with the same pipeline delay as the sampled data (refer to timing diagram in Figure 15 below) To set XFUn as the trigger, XFUn_SEL must be set to “10” and TREN in register CHIP_CTRL at 0x04 set to ‘1’.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								TREN							

Note: When TREN is set to ‘1’, the SYNCTRIG input is used as a trigger input, when at ’0’ it is used as a SYNC input. See section SYNCTRIG input for more information

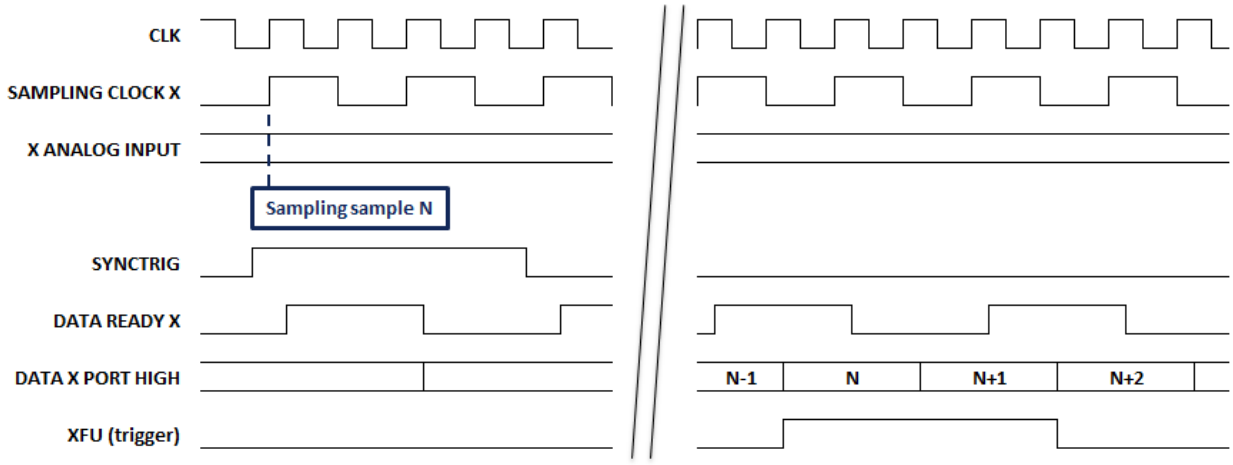


Figure 16: Trigger mode timing diagram

5.5.2 Swing adjust

By default the swing of the data output is reduced to optimize power consumption. When working with long traces length and/or limiting FPGA/ASIC a full swing option is available through SPI to increase the output swing.

It is configured through register CHIP_CTRL at 0x04:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
									LSSA						

When LSSA is at ‘0’, the output swing of LVDS data and data ready are reduced which is the default configuration as well. When set to ‘1’ LVDS output data and data ready are in full swing configuration.

5.5.3 PRBS on data output

A PRBS (Pseudo Random Bit Sequence) can be generated for the LVDS output. It can either be disabled, scrambling the data or output alone. The implemented PRBS sequence is based on the sequence X7 + X6 + 1. The same sequence is output on all bits of the LVDS ports (12 bits of data and the XFU1 and XFU2 bits).
It is configured through the LVDS_PRBS_CTRL register at address 0x63

LVDS_PRBS_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
														PRBS_ctrl	

PRBS_ctrl = “00” by default and the PRBS is disabled; the output data corresponds to the ADC samples plus control bit. Setting PRBS_ctrl to “01” configures the LVDS output in scrambling mode. In that case, the output corresponds to the ADC samples plus control bit XOR the PRBS value. The PRBS value is the same on all output.
Setting PRBS_ctrl to “11” configures the LVDS output so that the PRBS alone is output. The PRBS value is the same on all output.

5.5.4 Test mode

The test modes are only available in LVDS DEMUX 1:1 output configuration.

5.5.4.1 Enabling test mode

Two test modes on the ADC output are offered to help validate the interface with the ADC: flash and ramp patterns. The test modes are enabled through the TEST_MODE register at address 0x66:

TEST_MODE															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
												RPEN	FLEN		TMEN

To enable any test mode, it is necessary to put TMEN at '1' (test mode is disabled by default). Then to activate ramp pattern mode, RPEN must be set to '1' and to activate a flash pattern output, FLEN must be set to '1'. If both RPEN and FLEN are set to '1', the output is in normal operation and none of the test modes is output. Refer to the 2 following sections for more information on the test modes.

5.5.4.2 Ramp test mode

In ramp test mode, the data output on the LVDS is a 12 bit ramp on both channels XH (and XL in DEMUX 1:2). The same value is output on both ports in DEMUX 1:2. The 2 control bits XFU1 and XFU2 are toggling. The ramp value is reset to 0x000 when a pulse is sent on the SYNCTRIG input in SYNC mode (See section SYNCTRIG input for more information). See the timing diagram below for more information (X represents channel A or B).

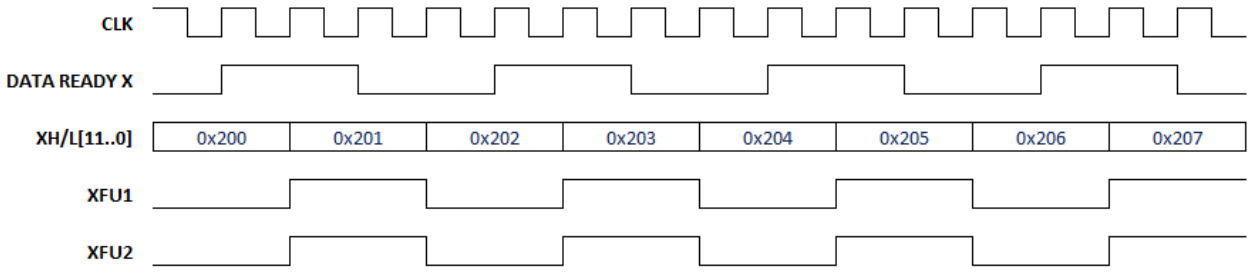


Figure 17: Ramp test mode timing diagram

5.5.4.3 Flash test mode

The flash mode is useful to align the interface between FPGA and ADC. The flashing pattern consists of one data at 0xFFF followed by [flash_length-1] data at 0x000. The control bit XFU1 and XFU2 follows the same sequence. The flash_length value can be configured through the FLASH_RST_LENGTH register at address 0x67. Its default value is 24.

FLASH_RST_LENGTH															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
										Flash_length					

See below the timing diagram for the LVDS output when in flashing mode. It is the same for both channels and all ports used (X represents channel A or B).

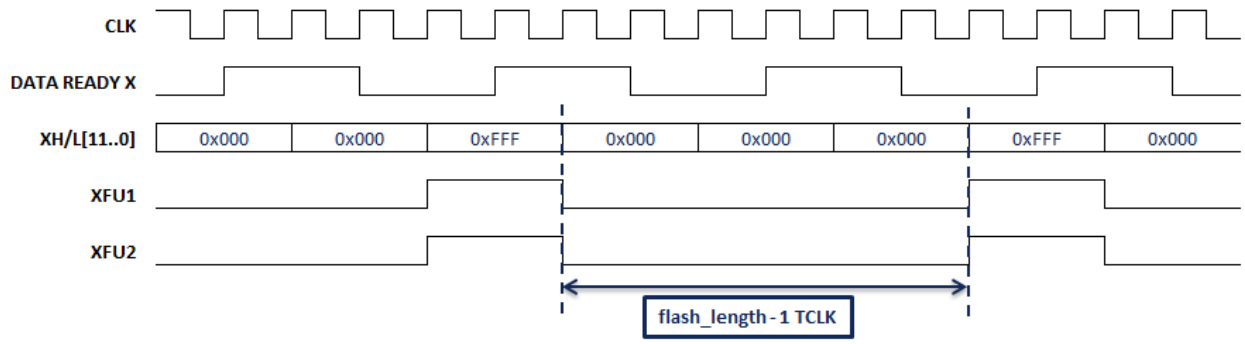


Figure 18: Flashing test mode timing diagram

5.6 High speed serial interface

The EV12AD500 offer a high speed serial interface to output the data; it has 8 high speed serial lanes (4 per core) running at twice the external clock frequency (for example at F_{CLK} = 3GHz, the serial links run at 6Gbps). It uses the protocol ESIstream to optimize efficiency, simplicity and latency.

More information on the ESIstream protocol can be found on www.esistream.com.

The ESIstream protocol is a 14b/16b encoding based on 14 scrambled bits along with 2 overhead bits: clock bit and disparity bit. Applied onto the EV12AD500, the 16 bits frames are as follows:

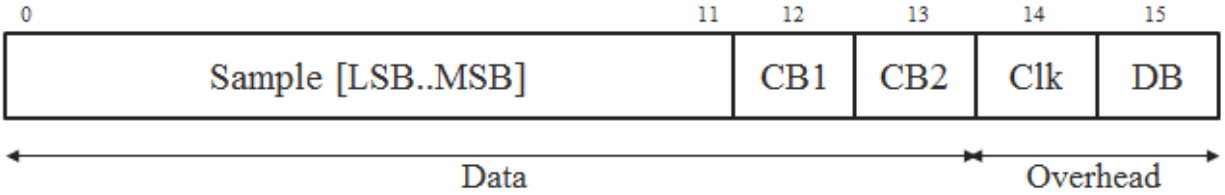


Figure 19: ESIstream frame with EV12AD500

DB being the disparity bit, CLK the clock bit, CB1 and CB2 the control bit of the ADC (Refer to section Control bit CB1 and CB2) and bit 11 to 0 contains the ADC sample. Bit 13 to 0 are scrambled using an LSFR (Linear Feedback Shift Register) that generate the PRBS (Pseudo-Random Binary Sequence). The frames are transmitted LSB first.

5.6.1 ESIstream protocol

5.6.1.1 Scrambling

Applying scrambling ensures a statistical DC balanced transmission. It also statistically ensures that there are transitions in the transmission. It is necessary to comply with these constraints otherwise the CDR (Clock and Data Recovery) may lose its lock and the data would be corrupted.

The scrambling technique used in ESIstream is an additive scrambling to avoid error propagation in case of a single bit error. It is based on Fibonacci architecture using the following polynomial: X17+X3+1. It has a run length of 2^{17} - 1. Instead of using a shift of one bit per operation, it uses shifts of 14 bits per operation to adapt to the size of the data being scrambled.
The equations to use to generate this PRBS are as follow:

$$LFSR_{n+1}(0) = LFSR_n(14)$$
$$LFSR_{n+1}(1) = LFSR_n(15)$$
$$LFSR_{n+1}(2) = LFSR_n(16)$$
$$LFSR_{n+1}(3) = LFSR_n(0) \text{ xor } LFSR_n(3)$$
$$LFSR_{n+1}(4) = LFSR_n(1) \text{ xor } LFSR_n(4)$$
$$LFSR_{n+1}(5) = LFSR_n(2) \text{ xor } LFSR_n(5)$$
$$LFSR_{n+1}(6) = LFSR_n(3) \text{ xor } LFSR_n(6)$$
$$LFSR_{n+1}(7) = LFSR_n(4) \text{ xor } LFSR_n(7)$$
$$LFSR_{n+1}(8) = LFSR_n(5) \text{ xor } LFSR_n(8)$$
$$LFSR_{n+1}(9) = LFSR_n(6) \text{ xor } LFSR_n(9)$$
$$LFSR_{n+1}(10) = LFSR_n(7) \text{ xor } LFSR_n(10)$$
$$LFSR_{n+1}(11) = LFSR_n(8) \text{ xor } LFSR_n(11)$$
$$LFSR_{n+1}(12) = LFSR_n(9) \text{ xor } LFSR_n(12)$$
$$LFSR_{n+1}(13) = LFSR_n(10) \text{ xor } LFSR_n(13)$$
$$LFSR_{n+1}(14) = LFSR_n(11) \text{ xor } LFSR_n(14)$$
$$LFSR_{n+1}(15) = LFSR_n(12) \text{ xor } LFSR_n(15)$$
$$LFSR_{n+1}(16) = LFSR_n(13) \text{ xor } LFSR_n(16)$$

The PRBS is applied to the data as follow; the 14 LSB of the PRBS are the bits used to scramble the data.

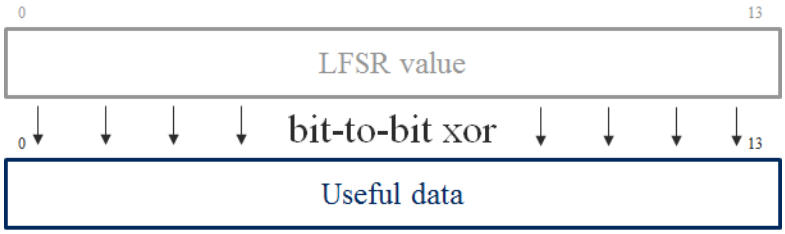


Figure 20: LFSR operation

This particular LFSR was chosen because it reduces the number of necessary gates to be implemented.

5.6.1.2 Encoding

After scrambling, the 14 bits of data are encoded into a 16 bits frame. One of the added bits is the clk bit; it toggles at every frame. The last bit encoding these 15 bits is the disparity bit. Its objective is to ensure deterministically the advantages brought statistically by the scrambling process.

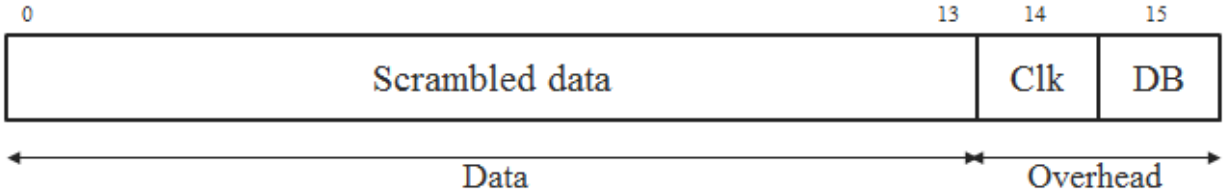


Figure 21: Frame format after encoding

Even with scrambling, large running disparity can still occur with very low probability and could produce excessive eye shifts. These eye shifts could be balanced by a more complicated equalization stage in the receiver if the running disparity was still limited. However, a PRBS does not bind the running disparity deterministically, thus the data could be corrupted on the reception end and it could eventually cause the CDR to lose its lock. To prevent this, the disparity bit is implemented.

The running disparity of the transmission is constantly monitored by the transmitter on each link.
For each frame, its disparity is calculated, 2 cases can occur on the running disparity:

a. The running disparity of the transmission **does not** increase above +/- 15 (+15 and -15 included). In this case, the disparity bit is set to '0' and the 15 bits of data (scrambled data + clk bit) are transmitted as such.
b. The running disparity of the transmission **does** increase above +/-15 (+15 and -15 excluded). In this case, the 15 bits of data (scrambled data + clk bit) are inverted and the disparity bit is set to '1'.

The running disparity is updated with the disparity of the frame.

This disparity bit ensures that the longest possible series of '1' or '0' transmitted is of 48 bits (the clk bit reduces this value effectively to 32). It also ensures that the running disparity does not exceed +/- 15 (included) which satisfies the DC balance condition.

In normal operating mode, the receiver will check the disparity bit first. If it is high then it will invert the received data and descramble them. Otherwise it will directly descramble them.

5.6.1.3 Synchronization

The link must be synchronized to align the frames between the transmitter and the receiver and to synchronize the reception scrambler with the transmission scrambler. The synchronization is controlled through the SYNC signal sent by the receiver (FPGA/ASIC) to the transmitter (EV12AD500).

The synchronization works in 2 steps and starts when the ADC receives a SYNCTRIG pulse in SYNC mode (refer to section SYNCTRIG input).

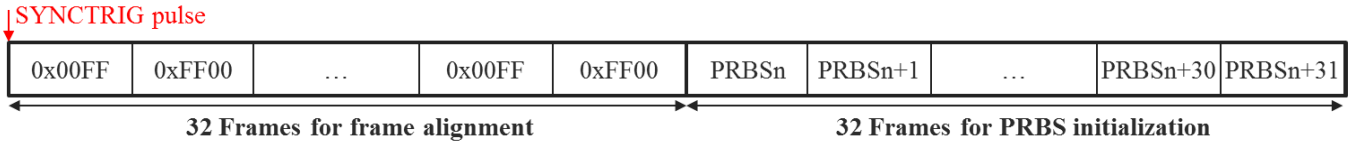


Figure 22: Synchronization sequence

When the ADC sees the SYNCTRIG pulse, it will send an alignment pattern which is 32 frames alternating between 0xFF00 and 0x00FF. The sequence bypasses the scrambling and disparity processing (the sequence is DC balanced). This alignment pattern should be used by the receiver to align its data on the transmitter output data.
After these 32 frames, the transmitter starts sending 32 additional frames containing the scrambling PRBS alone. These frames contain 14 bits of the PRBS plus the clk bit and the disparity bit. They go through the disparity processing, as the PRBS value will start to impact the running disparity of the transmission.

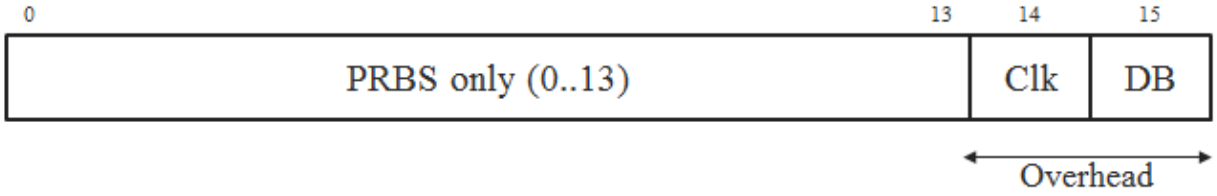


Figure 23: Frame sent for PRBS initialization

The receiver will detect the transition from the alignment pattern to the PRBS alone (passive detection). It will determine the initial value it has to start its PRBS with after receiving 2 frames of the PRBS. These 2 frames contain 28 bits of the PRBS sequence; the receiver needs 17 bits to determine its initial value. The transmitter (EV12AD500) PRBS sequence is reset upon reception of a SYNCTRIG pulse in SYNC mode.

After these 2 steps, the synchronization of the link is complete.

During normal operation, the synchronization of the serial links can be monitored through the clk bit. In case the receiver does not detect that the clk bit is toggling properly, then it can state that the link is not synchronous or has lost its synchronization and restart the synchronization process. Another option is to use the timestamp control bit of the ADC to monitor the interface synchronization (refer to section Control bit CB1 and CB2).

5.6.2 Control bit CB1 and CB2

The control bits CB1 and CB2 are controlled through the CTRL_BIT_CFG register at address 0x64:

CTRL_BIT_CFG															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
														CB2_SEL	CB1_SEL

CB1 can either be the in-range control bit when CB1_SEL is at ’0’ which is the default value or the parity bit when at ‘1’.
CB2 can either be the timestamp bit when CB2_SEL is at ‘0’ which is the default value or the trigger bit when at ‘1’.

5.6.2.1 IN-RANGE

The in-range control bit output ‘1’ when the ADC input is not saturated and ‘0’ when it is.

5.6.2.2 PARITY BIT

The parity bit is a XOR between the 12 bits of the sample.

5.6.2.3 TIMESTAMP

The timestamp control bit is a PRBS sequence that is updated with every frame. It is the same sequence for all links and is reset upon receiving a SYNCTRIG pulse. The PRBS sequence is based on an LFSR of Gallois architecture with the polynomial X7+X6+1. It can be used to identify the samples order and/or check the synchronization of the serial interface.

5.6.2.4 TRIGGER

The trigger bit is a copy of the SYNCTRIG input with the same pipeline delay as the sampled data (refer to timing diagram in Figure 24 below). To set CB2 as the trigger, CB2_SEL must be set to ‘1’ and TREN in register CHIP_CTRL at 0x04 set to ‘1’.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								TREN							

Note: When TREN is set to '1', the SYNCTRIG input is used as a trigger input, when at '0' it is used as a SYNC input. See section SYNCTRIG input for more information

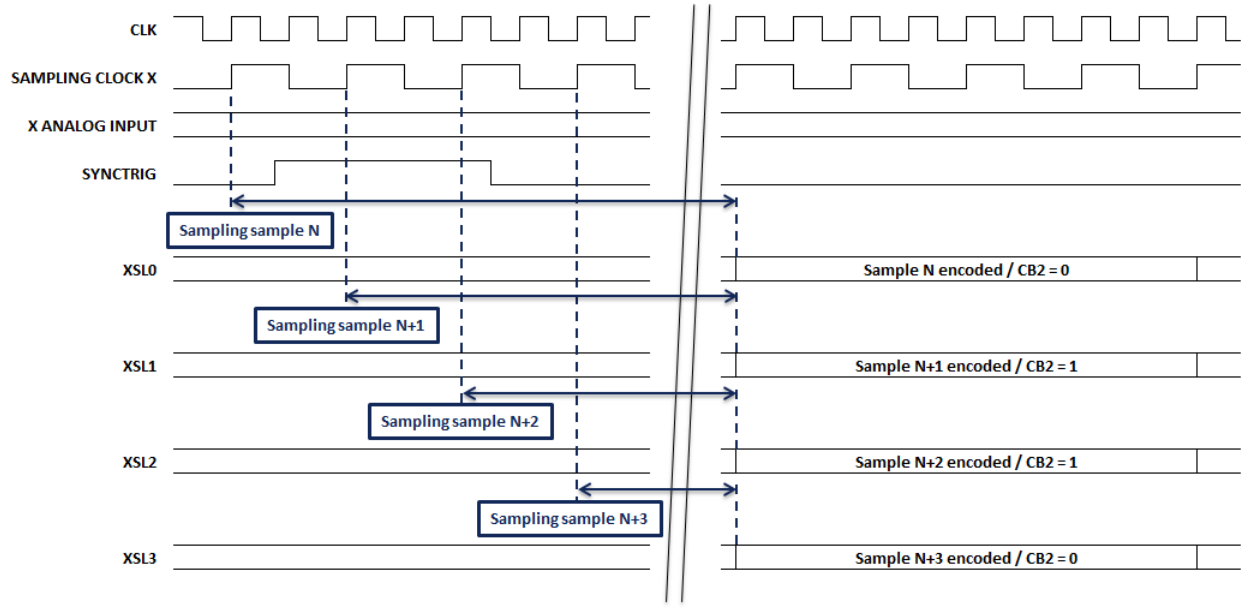


Figure 24: Trigger mode timing diagram in serial interface

5.6.3 Swing adjust

By default the swing of the serial outputs is reduced to optimize power consumption. When working with long traces length and/or limiting FPGA/ASIC a full swing option is available through SPI to increase the output swing and thus the reception eye diagram.

It is configured through register CHIP_CTRL at 0x04:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						SLSA									

When SLSA is at '1', the serial outputs swing are reduced which is the default configuration as well. When set to '0' the serial outputs swings are in full swing configuration.

5.7 Input configuration

5.7.1 Input impedance trimming

Impedance matching is important to maximize power transmission and avoid reflexion. The DC impedance of each channel can be trimmed digitally and individually to 100Ω through register X_RIN at address 0x1F for channel A and 0x3E for channel B:

X_RIN															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
										RIN_TRIM					

The default value is 0x10. Trimming the input impedance allows to achieve a 100Ω +/-2.4Ω precision.

5.7.2 Input bandwidth selection

The ADC has a tunable bandwidth selectable through SPI with register CHIP_CTRL at 0x04:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
										BW					

When selecting nominal bandwidth (default configuration BW = '1'), the noise performance will be improved as the noise is cut earlier. On the other hand, when working with high input frequency, it is optimal to use the extended bandwidth mode (BW = '0') to avoid losing input power due to the bandwidth.

5.7.3 Input common mode trimming

The ADC can work with DC coupling analog inputs. Its input common mode (CMIREF) for each channel can be trimmed individually. It can also be used to optimize linearity performance. It is controlled through the register X_CMIREF at address 0x1E for channel A and 0x3D for channel B:

X_CMIREF															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
											CMIN_TRIM				

The default value is 0x10. Each increment of the value adds 11mV; each decrement reduces the common mode by 11mV. The 32 possible steps thus allow 340mV range.

5.8 SYNCTRIG input

The SYNCTRIG input is an LVDS signal. The SYNCTRIG input can be used in 2 different modes controlled through bit7 of SPI register CHIP_CTRL at address 0x04:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								TREN							

The default mode when TREN = '0' is the SYNC mode. When enabled to '1', the SYNCTRIG input is used in trigger mode (see section Control bit XFU1 and XFU2 and Control bit CB1 and CB2 for more information).

The SYNC signal is mandatory in order to have deterministic timing for the 2 cores synchronization and for multiple ADCs time alignment. Thus it is necessary to send a SYNC pulse after power-up so that the ADC timing circuitry starts in a deterministic way. This pulse resets the different dividers on the clock path and ensures that all the timing circuitry restarts deterministically. It also starts the synchronization sequence of the serial interface (refer to section ESIstream protocol for more information). It also resets the test modes to their initial value.

The SYNC signal should be synchronous to the external clock, is active high and should be compliant with the timing specified in Table 10. One setting for the SYNCTRIG input can be configured through SYNC_CTRL register at address 0x74:

SYNC_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															ESEL

The ESEL bit is used to configure which edges of the input clock recovers the SYNCTRIG input. By default, the SYNCTRIG input is recovered on rising edges of the clock (ESEL = '0'); when ESEL ='1', the SYNCTRIG input is recovered on falling edges of the input clock. In any case, the reset of the timing circuitry of the ADC is done on rising edges of the input clock. This feature is useful to avoid the meta-stability zone of the SYNCTRIG input specified in Table 10.

When a SYNCTRIG input pulse is sent in SYNC mode and LVDS DEMUX 1:1 output, the timing circuitry is reset; thus the data ready output will stop. The time before it restarts can be configured through the FLASH_RST_LENGTH register at address 0x67.

FLASH_RST_LENGTH															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				reset_length											

By default, reset_length is at 16. Refer to timing diagram in Figure 5 to see an example with reset_length = 4. For a deterministic timing, reset_length value must be within 2 (0b000010) and 64 (0b111111)

5.9 SYNCO output and Slow Synchronization Output (SSO)

SYNCO output is a copy of the SYNCTRIG input resampled onto the CLK signal. It can be used to synchronize multiple devices with a chained SYNCO to SYNCTRIG interface.
The SSO output signal is a clock signal that is a division by 16 of the master clock input. It is never stopped, reset nor interrupted as long as the master clock is provided to the ADC. It can be used as a slow reference clock to synchronize the sampling of multiple devices or provide a synchronous clock source to other elements in the system.

Both SYNCO and SSO are LVDS output signals; their swing can be configured through the bit 8 of register CHIP_CTRL at address 0x04

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							SOSA								

When SOSA is at '0', the LVDS output swing of SSO and SYNCO are reduced which is the default configuration. When set to '1' SSO and SYNCO are in full swing configuration.

5.10 Temperature calibration set selection

A factory calibration is performed on every part during industrial test. During this process, two sets of factory calibration (over temperature) are saved in on-chip One Time Programmable registers (OTP). To optimize performance of the device, hot temperature calibration should be chosen when working with diode temperature over 65°C and cold temperature should be chosen when working with diode temperature below 65°C.

To choose which factory temperature calibration set to load, bit 3 of register CHIP_CTRL at address 0x04 should be considered:

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
												CAL_S			

By default, hot temperature calibration is selected (CAL_S = '0'). To change to cold temperature calibration, CAL_S should be written to '1'. Whenever this bit is modified, the calibration should be loaded into the SPI register through writing '1' in bit 0 of register LOAD_CAL at address 0x7E:

LOAD_CAL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															L_CAL

5.11 Single event protection

5.11.1 Extra SEE protect

All sensitive areas of the device have been protected to increase robustness. This includes but is not limited to clock circuitry and SPI registers. To improve even more the robustness, an extra protection mode has been implemented. It can be activated through the following register EXTRA_SEE_PROTECT at address 0x7F:

EXTRA_SEE_PROTECT															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															SEP

Enabling register SEP by writing '1' disables the SYNCTRIG input when in SYNC mode and thus prevents unwanted timing reset of the ADC (See section SYNCTRIG input for more information). It prevents as well any modification on the SPI registers. The SPI clock (SCLK) can be provided from time to time to refresh the SPI (and flush out any SE that would have impacted one branch of the TMR). When it is necessary to modify the configuration of the device or synchronize the ADC, this register needs to be set back to '0'.

Use of this register is not mandatory, but improves the robustness of the device against radiation effects.

5.11.2 CRC checking

An option to verify that the calibration has been successfully loaded is available through SPI registers. The CRC reference value is stored in the OTP (One Time Programmable registers) during industrial testing of the part respectively for each channel and each calibration set at the following addresses:

- 0x76 for channel A and hot temperature calibration;
- 0x77 for channel A and cold temperature calibration;
- 0x78 for channel B and hot temperature calibration;
- 0x79 for channel B and cold temperature calibration;

When the calibration is loaded into the SPI, the CRC of the loaded set is automatically calculated for each channel and can be read in registers 0x69 for channel A and 0x6A for channel B. If the calculated CRC value and the reference value (corresponding to the loaded calibration) are equal, the load has been successful; if not, the desired calibration set should be reloaded. Refer to section Temperature calibration set selection for more information.

5.12 Interleaving the cores

5.12.1 Interleaving or aligning the sampling clocks

The sampling clocks of channel A and B can be interleaved (default configuration) or aligned. This is controlled through bit 0 of register CHIP_CTRL at address 0x04.

CHIP_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
															CLKINT

When CLKINT = '0', the sampling clocks of channel A and B are in phase; when CLKINT = '1' (default configuration), the sampling clocks of channel A and B are in phase opposition to allow interleaving.

5.12.2 Interleaving calibration

To improve interleaving performance, the offset, gain and phase of each core can be corrected thanks to embedded DACs. These settings are available through SPI commands and are application dependent.

The offset calibration is available in register X_OFFSET_CAL at address 0x23 for channel A and 0x42 for channel B.

X_OFFSET_CAL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							Offset_calibration								

These offset calibration registers offer a tuning range of +/- 27.4LSB by step of 0.11LSB. The default value is 0x100; the minimum value 0x000 corresponds to +27.4LSB correction; and the maximum value 0x1FF corresponds to -27.4LSB correction.

The gain calibration is available in register X_GAIN_CAL at address 0x21 for channel A and 0x40 for channel B.

X_GAIN_CAL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						Gain_calibration									

These gain calibration registers offer a tuning range of +260/-226LSB by step of 0.47 LSB. The default value is 0x200.

The phase calibration is available in register X_PHASE_CAL at address 0x22 for channel A and 0x41 for channel B.

X_PHASE_CAL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
								Phase_calibration							

These phase calibration registers offer a tuning range of +/- 0.9ps by step of 7fs. The default value is 0x80; the minimum value 0x00 corresponds to -900fs correction; and the maximum value 0xFF corresponds to +900fs correction. For wider range of phase correction, SDA could be used (refer to section Sampling Delay Adjust (SDA)).

5.13 Sampling Delay Adjust (SDA)

The effective sampling instant of each ADC cores is adjustable independently thanks to built in fine clock shifters. They provide 1023 steps of 10fs delay to achieve a total tuning range of 10ps. The delay is configured through the SPI register X_SDA_CTRL at address 0x20 for channel A and 0x3F for channel B.

X_SDA_CTRL															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			DIS			SDA_value									

To enable the SDA, the bit 12 should be set to '0', and the value of delay added on the sampling time will be SDA_value x 10 fs. The SDA is disabled by default (DIS = '1'). It should be noted that enabling the SDA has an impact on the jitter performance of the ADC.
Enabling the SDA automatically adds 30ps delay on the sampling clock path, hence the absolute range accessed through the use of the SDA is 30-40ps delay. Moreover, the SDA must be either enabled on both channels or disabled on both channels for the ADC to work. The SDA_value can be different between channels.

5.14 Stand-by modes

The stand-by modes are controlled through the STDBY register at address 0x62:

STDBY															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		SSL3	SSL2	SSL1	SSL0					SAB	SAA			SFB	SFA

Both channels can be put in full stand-by independently. Writing '1' in the register SFA (respectively SFB) will put the channel A (respectively B) in stand-by.

A standby of the analogic part of the ADC can also be done through writting '1' in the register SAA (respectively SAB) on channel A (respectively B). Its advantage is that it reduces the power consumption while keeping the output interface running.

A standby of each serial links is also available. When SSLn = '0', the serial lane ASLn et BSLn are running; when SSLn = '1', the serial lane ASLn and BSLn are in standby.

5.15 Die junction temperature monitoring diode

Two pins are provided so that the temperature diode can be probed using standard temperature sensors. Diode C must be connected to GND.

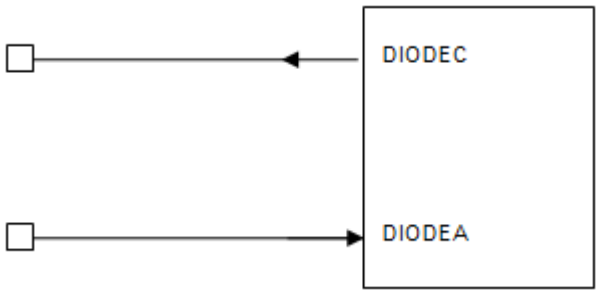


Figure 25: Temperature diode

To characterize the temperature diode a current of 1 mA is applied on the DIODEA pin. The voltage across the DIODEA pin and the GND pin gives the junction temperature using the intrinsic diode characteristics below

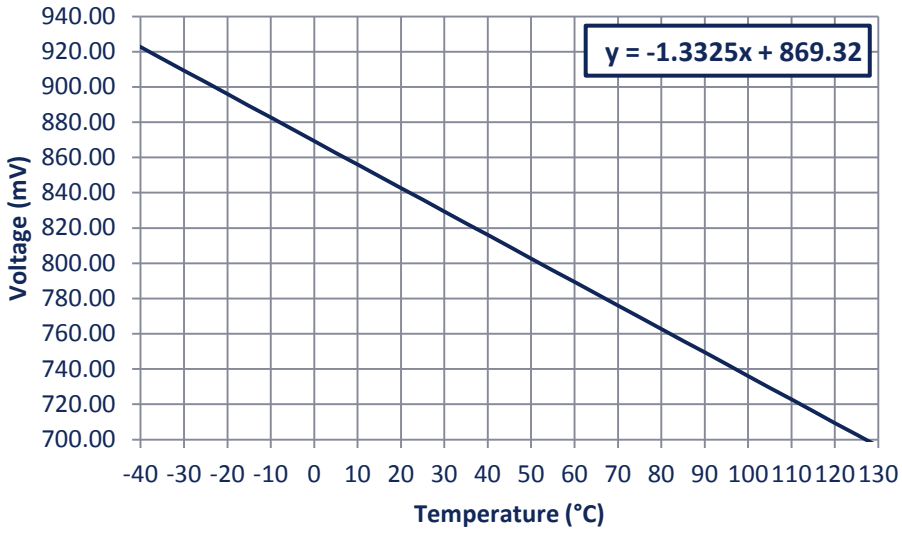


Figure 26: Diode temperature

6 Application information

6.1 Power supplies recommendation and decoupling

The ADC can work with a single rail. It is recommended to use ferrite and decoupling capacitance to avoid power supply pollution.
For VCCIOXn (X = H or S; n = 1 or 2), each supply should have 6x10nF decoupling capacitor.

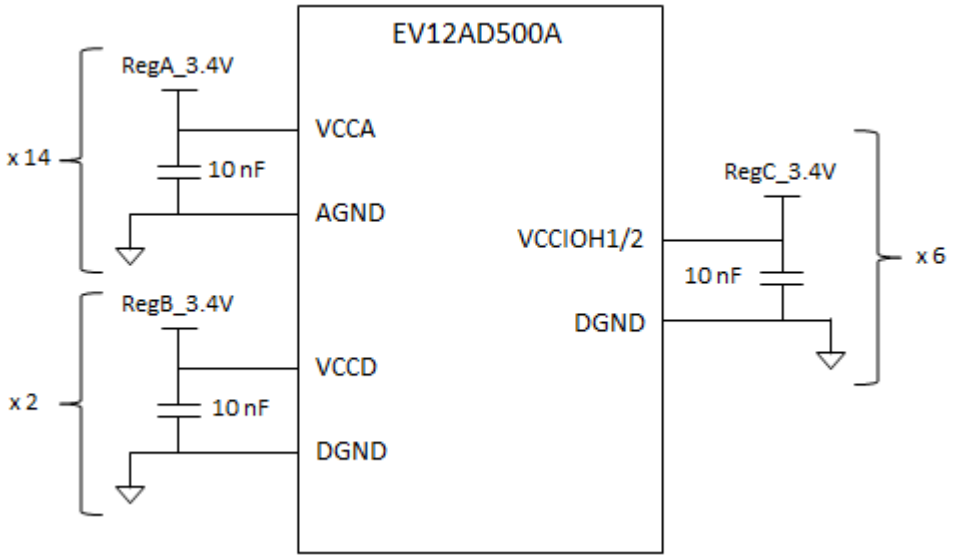


Figure 27: Decoupling with separate supplies at 3.4V (LVDS DEMUX 1:1 only)

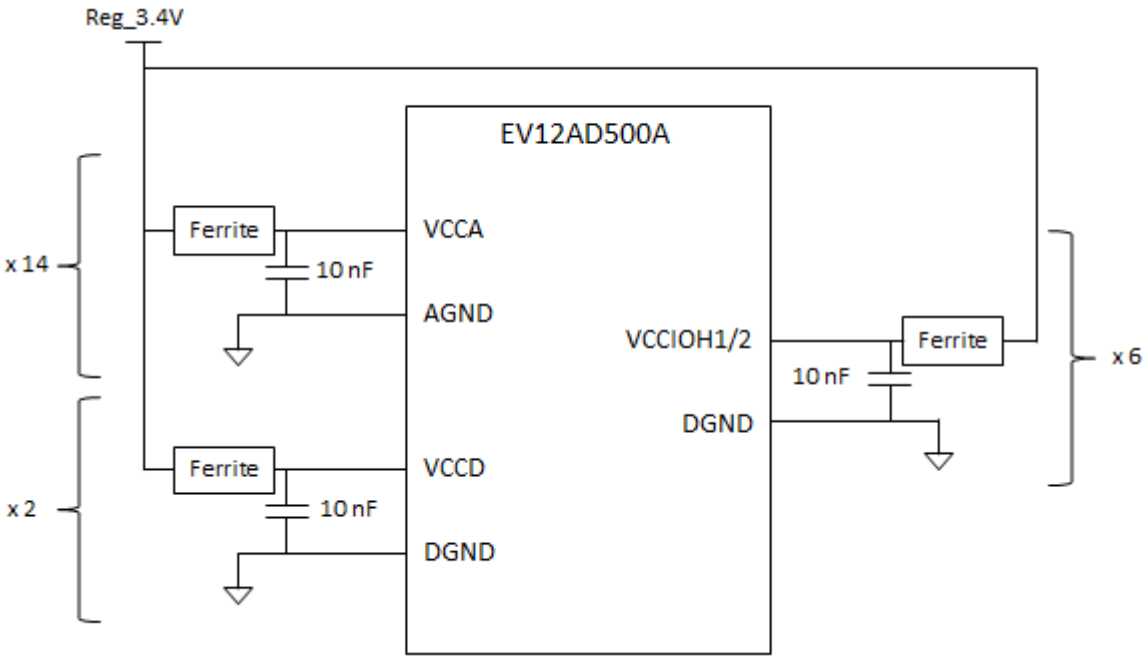


Figure 28: Decoupling with single supply at 3.4V (LVDS DEMUX 1:1 only)

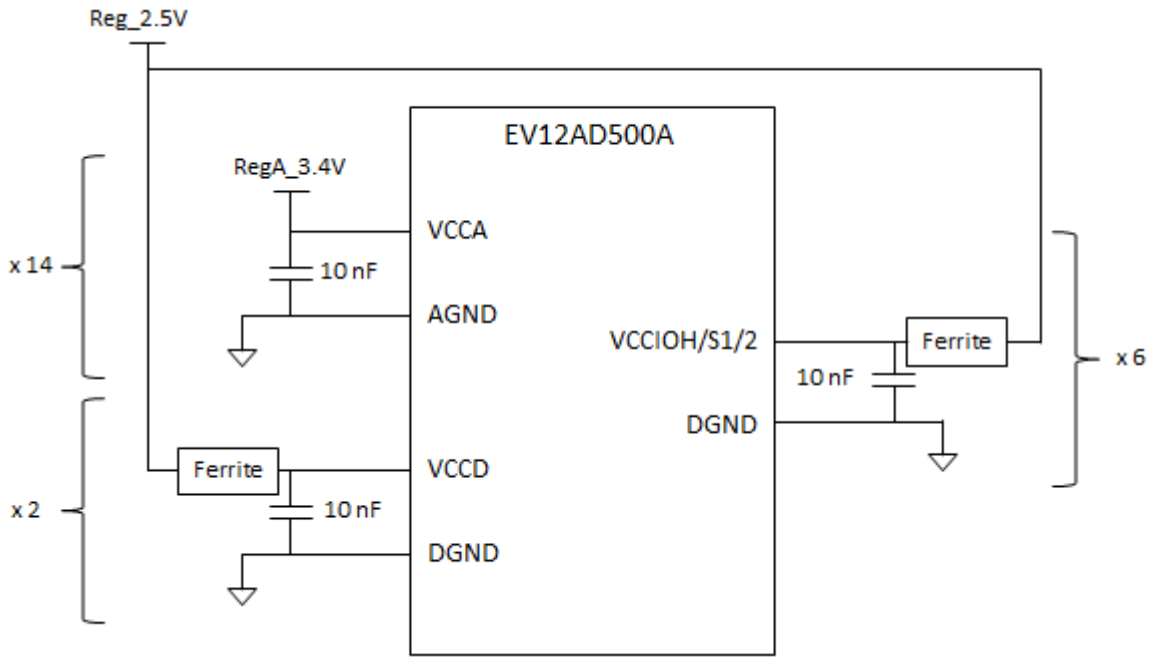


Figure 29: Decoupling with dual supplies at 3.4V and 2.5V

Supplies settling time should be faster than 10ms. No specific power sequencing is required.

6.2 Analog inputs

The analog inputs AIN_P, AIN_N and BIN_P, BIN_N can be DC coupled or AC coupled. The phase and amplitude imbalance on the inputs (XIN_P compared to XIN_N) have an impact on the linearity performance of the device. The input driver should be chosen to minimize these effects and the trace length should be matched between XIN_P and XIN_N.

7 Ordering information

Table 19: Ordering information

Part Number	Package	Temperature Range	Screening Level	Comments
EVP12AD500SHY-V1	CBGA255 SAC305	Ambient	Prototype	
P/N to be defined	CBGA255 SAC305	Tc -40°C, Tj +110°C	Industrial	

8 Revision history

Issue	Date	Comments
A	August 2016	Issued from preliminary datasheet 1156C
B	September 2016	Added serial interface data rate

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