# EV12DS130AG
# EV12DS130BG
# Low Power 12-bit 3 Gsps Digital to Analog Converter with 4/2:1 Multiplexer

**Datasheet DS1080**




## MAIN FEATURES

- 12-bit Resolution
- 3 Gsps Guaranteed Conversion Rate
- 7 GHz Analog Output Bandwidth
- 4:1 or 2:1 integrated Parallel MUX (Selectable)
- Selectable Output Modes for performance optimization: Return to Zero, Non Return to Zero, Narrow Return to Zero, RF
- Low Latency Time: 3.5 Clock Cycles
- 1.4 Watt Power Dissipation in MUX 4:1 Mode
- Functions
  - Selectable MUX Ratio 4:1 (Full Speed), 2:1 (Half Speed)
  - Triple Majority Voting
  - User-friendly Functions:
    - Gain Adjustment
    - Input Data Check Bit (FPGA Timing Check)
    - Setup Time and Hold Time Violation Flags (STVF, HTVF)
    - Clock Phase Shift Select for Synchronization with DSP (PSS[2:0])
    - Output Clock Division Selection (Possibility to Change the Division Ratio of the DSP Clock)
    - Input Under Clocking Mode
    - Diode for Die junction Temperature Monitoring
- LVDS Differential Data input and DSP Clock Output
- Analog Output Swing: $1V_{pp}$ Differential (100Ω Differential Impedance)
- External Reset for Synchronization of Multiple MuxDACs
- Power Supplies: 3.3 V (Digital), 3.3V & 5.0V (Analog)
- LGA255, CCGA255, Ci-CGA255 Package (21 × 21 mm Body Size, 1.27 mm Pitch)

## PERFORMANCES

Broadband: NPR at –14 dB Loading Factor, (See Section 7.2.7 ”NPR Performance” on page 62)

- 1st Nyquist (NRTZ): NPR = 51.3 dB 10.0 Bit
  Equivalent at Fs = 3 Gsps
- 1st Nyquist (NRTZ): NPR = 55.7 dB 10.8 Bit
  Equivalent at Fs = 1.5 Gsps
- 2nd Nyquist (NRTZ or RTZ): NPR = 44.6 dB 8.9 Bit
  Equivalent at Fs = 3 Gsps
- 3rd Nyquist (RF): NPR = 42.5 dB 8.6 Bit
  Equivalent at Fs = 3 Gsps

Single Tone: (see Section 5. ”Functional Description” on page 17)

- Performances Characterized for Fout from 100 MHz to 4500 MHz and from 2 Gsps to 3.2 Gsps
- Performance Industrially Screened Over 3 Nyquist Zones at 3 Gsps for Selected Fout.

Step Response

- Full Scale Rise /Fall Time 60 ps

## APPLICATIONS

- Direct Digital Synthesis for Broadband Applications (L-S and Lower C Band)
- Automatic Test Equipment (ATE)
- Arbitrary Waveform Generators
- Radar Waveform Signal Synthesis
- DOCSIS V3.0 Systems

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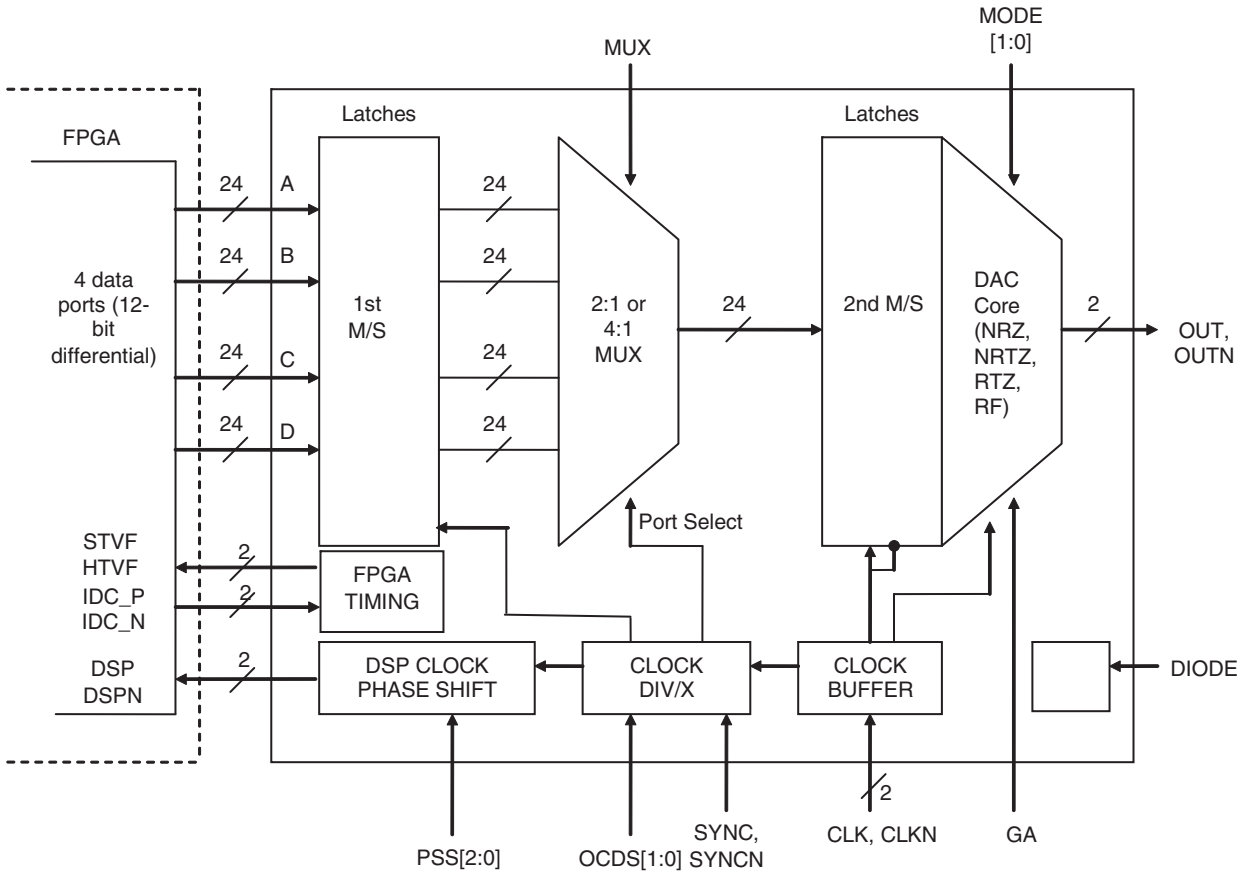
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## 1. BLOCK DIAGRAM

**Figure 1-1.** Simplified Block Diagram




## 2. DESCRIPTION

The EV12DS130A/B is a 12-bit 3 Gsps DAC with an integrated 4:1 or 2:1 multiplexer, allowing easy interface with standard LVDS FPGAs thanks to user friendly features as OCDS, PSS.

It embeds different output modes (RTZ, NRZ, narrow RTZ, RF) that allow performance optimizations depending on the working Nyquist zone.

The Noise Power Ratio (NPR) performance, over more than 900 MHz instantaneous bandwidth, and the high linearity (SFDR, IMD) over full 1$^{st}$ Nyquist zone at 3 Gsps (NRZ feature), make this product well suited for high-end applications such as arbitrary waveform generators and broadband DDS systems.



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# 3. ELECTRICAL CHARACTERISTICS

## 3.1 Absolute Maximum Ratings

**Table 3-1. Absolute Maximum Ratings**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Positive Analog supply voltage | $V_{CCA5}$ | 6.0 | V |
| Positive Analog supply voltage | $V_{CCA3}$ | 4.0 | V |
| Positive Digital supply voltage | $V_{CCD}$ | 4.0 | V |
| Digital inputs (on each single-ended input) and IDC, SYNC, signal<br>Port P = A, B, C, D<br>$V_{IL}$<br>$V_{IH}$<br>Digital Input maximum Differential mode swing | [P0..P11],<br>[P0N.. P11N]<br>IDC_P, IDC_N<br>SYNC, SYNCN | <br><br>GND–0.3<br>$V_{CCA3}$<br>2.0 | <br><br>V<br>V<br>$V_{pp}$ |
| Master clock input (on each single-ended input)<br>$V_{IL}$<br>$V_{IH}$<br>Master Clock Maximum Differential mode swing | CLK, CLKN | <br>1.5<br>3.5<br>2.5 | <br>V<br>V<br>$V_{pp}$ |
| Control functions inputs<br>$V_{IL}$<br>$V_{IH}$ | MUX,<br>MODE[0..1],<br>PSS[0..2],<br>OCDS[0..1] | <br>–0.4V<br>$V_{CCD}$ + 0.4 | <br>V<br>V |
| Gain Adjustment function | GA | –0.3V, $V_{CCA3}$ + 0.3 | V |
| Maximum Junction Temperature | Tj | 170 | °C |
| Storage Temperature | Tstg | –65 to 150 | °C |
| Electrostatic discharge immunity<br>ESD Classification | ESD HBM | 1000<br>Class 1B | V |

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
2. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
3. Maximum ratings enable active inputs with DAC powered off.
4. Maximum ratings enable floating inputs with DAC powered on.
5. DSP clock and STVF, HTVF output buffers must not be shorted to ground nor positive power supply.



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## 3.2 Recommended Conditions of Use

**Table 3-2. Recommended Conditions of Use**

| Parameter | Symbol | Comments | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| Positive analog supply voltage | $V_{CCA5}$ | | 5.0 | V | (2)(4) |
| Positive analog supply voltage | $V_{CCA3}$ | | 3.3 | V | (1)(2)(4) |
| Positive digital supply voltage | $V_{CCD}$ | | 3.3 | V | (2)(4) |
| Digital inputs (on each single-ended input) and IDC, SYNC, signal<br>Port P = A, B, C, D<br>$V_{IL}$<br>$V_{IH}$<br>Differential mode swing | [P0..P11],<br>[P0N.. P11N]<br>IDC_P, IDC_N<br>SYNC, SYNCN | | <br><br><br>1.075<br>1.425<br>700 | <br><br><br>V<br>V<br>$mV_{pp}$ | (3) |
| Master clock input power level (Differential mode) | $P_{CLK}$ | | 3 | dBm | (3) |
| Control functions inputs | MUX, OCDS, PSS, MODE, PSS | $V_{IL}$<br>$V_{IH}$ | 0<br>$V_{CCD}$ | V<br>V | |
| Gain Adjustment function | GA | Range | 0<br>$V_{CCA3}$ | V | |
| Operating Temperature Range | Tc = Tcase<br>Tj = T junction | Military "M" & space grade | –55°C < Tc, Tj < 125°C | °C | |

Notes:
1. For low temperature it is recommended to operate at maximum analog supplies ($V_{CCA3}$) level.
2. The rise time of any power supplies (Vccd, Vcca5, Vcca3) shall be <10ms.
   For EV12DS130A, in order to obtain the guaranteed performances and functionality, the following rules shall be followed when powering the devices (See Section 8.9 ”Power Up Sequencing” on page 75)
   For EV12DS130B, no specific power up sequence nor power supplies relationships are required.
3. Analog output is in differential. Single-ended operation is not recommended. Guaranteed performance is only in differential configuration.
4. No power-down sequencing is required.



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## 3.3 Electrical Characteristics

Values in the tables below are based on our conditions of measurement and valid over temperature range respectively for M, and Space quality level and for typical power supplies ($V_{CCA5}$ = 5.0V, $V_{CCA3}$ = 3.3V, $V_{CCD}$ = 3.3V), typical swing, unless specified and in MUX4:1 mode.

**Table 3-3.** Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test Level[2] |
|---|---|---|---|---|---|---|---|
| RESOLUTION | | | 12 | | bit | | 1,6 |
| **POWER REQUIREMENTS** | | | | | | | |
| Power Supply voltage<br>- Analog<br>- Analog<br>- Digital | <br>$V_{CCA5}$<br>$V_{CCA3}$<br>$V_{CCD}$ | <br>4.75<br>3.15<br>3.15 | <br>5<br>3.3<br>3.3 | <br>5.25<br>3.45<br>3.45 | <br>V<br>V | (7)(8) | 1,6 |
| Power Supply current (4:1 MUX)<br>- Analog<br>- Analog<br>- Digital | <br>$I_{CCA5}$<br>$I_{CCA3}$<br>$I_{CCD}$ | | <br>84<br>106<br>187 | <br>92<br>125<br>213 | <br>mA<br>mA<br>mA | | 1,6 |
| Power Supply current (2:1 MUX)<br>- Analog<br>- Analog<br>- Digital | <br>$I_{CCA5}$<br>$I_{CCA3}$<br>$I_{CCD}$ | | <br>84<br>106<br>160 | <br>92<br>125<br>185 | <br>mA<br>mA<br>mA | | 1,6 |
| Power dissipation (4:1 MUX) | $P_D$ | | 1.4 | 1.6 | W | | 1,6 |
| Power dissipation (2:1 DMUX) | $P_D$ | | 1.3 | 1.5 | W | | 1,6 |
| **DIGITAL DATA INPUTS, SYNC and IDC INPUTS** | | | | | | | |
| Logic compatibility | | | LVDS | | | | |
| Digital input voltages:<br>- Differential input voltage<br>- Common mode | <br>$V_{ID}$<br>$V_{ICM}$ | <br>100 | <br>350<br>1.25 | <br>500 | <br>$mV_p$<br>V | | <br>1,6<br>4 |
| Input capacitance from each single input to ground | | | | 2 | pF | | 5 |
| Differential Input resistance | | 80 | 100 | 120 | Ω | | 1,6 |
| **CLOCK INPUTS** | | | | | | | |
| Input voltages (Differential operation swing) | | 0.56 | 1 | 2.24 | $V_{pp}$ | | 4 |
| Power level (Differential operation) | | –4 | 1 | 8 | dBm | (1) | 4 |
| Common mode | | 2.4 | 2.5 | 2.6 | V | | 4 |
| Input capacitance from each single input to ground (at die level) | | | 2 | | pF | | 5 |
| Differential Input resistance | | 80 | 100 | 120 | Ω | | 1,6 |



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**Table 3-3.** Electrical Characteristics (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test Level[2] |
|---|---|---|---|---|---|---|---|
| **DSP CLOCK OUTPUT** | | | | | | | |
| Logic compatibility | | | LVDS | | | | |
| Digital output voltages: | | | | | | | |
| - Differential output voltage<br>- Common mode | $V_{OD}$<br>$V_{OCM}$ | 240 | 350<br>1.30 | 450 | $mV_p$<br>V | | 1,6<br>4 |
| **ANALOG OUTPUT** | | | | | | | |
| Full-scale Differential output voltage (100Ω differentially terminated) | | 0.92 | 1 | 1.08 | $V_{pp}$ | | 1,6 |
| Full-scale output power (differential output) | | 0.25 | 1 | 1.64 | dBm | | 1,6 |
| Single-ended mid-scale output voltage (50Ω terminated) | | | $V_{CCA5}$ – 0.43 | | V | (4) | |
| Output capacitance | | | 1.5 | | pF | | 5 |
| Output internal differential resistance | | 90 | 100 | 110 | Ω | | 1, 6 |
| Output VSWR (using e2v evaluation board)<br>1.5 GHz<br>3 GHz<br>4.5 GHz | | | <br>1.17<br>1.54<br>1.64 | | | | 4 |
| Output bandwidth | | | 6 | | GHz | | 4 |
| **FUNCTIONS** | | | | | | | |
| Digital functions: MODE, OCDS, PSS, MUX<br>- Logic 0<br>- Logic 1<br>- Input Current | <br>$V_{IL}$<br>$V_{IH}$<br>$I_{IN}$ | <br><br>1.6 | <br>0<br>$V_{CCD}$ | <br>0.8<br><br>150 | <br>V<br>V<br>µA | <br><br><br>(6) | |
| Gain Adjustment function | GA | 0 | 0<br>$V_{CCA3}$ | | | | 1,6 |
| Digital output function (HTVF, STVF)<br>- Logic 0<br>- Logic 1<br>- Output Current | <br>$V_{OL}$<br>$V_{OH}$<br>$I_O$ | <br>–<br>2.1 | <br>–<br>– | <br>0.8<br><br>80 | <br>V<br>V<br>µA | <br>(5)<br><br>(6) | <br><br>1,6 |
| **DC ACCURACY** | | | | | | | |
| Differential Non-Linearity | DNL+ | | | 0.95 | LSB | | 1,6 |
| Differential Non-Linearity | DNL- | –0.95 | | | LSB | | 1,6 |
| Integral Non-Linearity | INL+ | | | 3 | LSB | | 1,6 |
| Integral Non-Linearity | INL- | –3 | | | LSB | | 1,6 |
| DC gain:<br>- Initial gain error<br>- DC gain adjustment<br>- DC gain sensitivity to power supplies<br>- DC gain drift over temperature | <br><br><br><br> | <br>–8<br><br><br> | <br>0<br>±11<br><br>±2 | <br>+8<br><br>+6<br> | <br>%<br>%<br>%<br>% | <br><br>(3)<br><br> | <br>1,6<br>4<br>1,6<br>4 |

Notes: 1. For use in higher Nyquist zone, it is recommended to use higher power clock within the limit.



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2. See Section 3.6 on page 14 for explanation of test levels.
3. Initial gain error corresponds to the deviation of the DC gain center value from unity gain. The DC gain adjustment (GA function) ensures that the initial gain deviation can be cancelled.
   The DC gain sensitivity to power supplies is given according the rule:
   GainSensVsSupply = |Gain@VccMin – Gain@VccMax| / Gain@Vccnom
4. Single-ended operation is not recommended, this line is given for better understanding of what is output by the DAC.
5. In order to modify the $V_{OL}/V_{OH}$ value, potential divider could be used.
6. Sink or source.
7. Only for EV12DS130A dependency between power supplies:
   Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy.
8. Please refer Section 8.9 "Power Up Sequencing" on page 75.

## 3.4 AC Electrical Characteristics

Values in the tables below are based on our conditions of measurement and valid over temperature range respectively for M, and Space quality level and for typical power supplies ($V_{CCA5}$ = 5.0V, $V_{CCA3}$ = 3.3V, $V_{CCD}$ = 3.3V), typical swing, unless specified and in MUX4:1 mode.

**Table 3-4.** AC Electrical Characteristics NRZ Mode (First Nyquist Zone)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level(1) |
|---|---|---|---|---|---|---|---|
| Single-tone Spurious Free Dynamic Range<br>First Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 100 MHz 0 dBFS | \|SFDR\| | 57 | 68 | | dBc | | 1,6 |
| Fs = 3 GSps @ Fout = 400 MHz 0 dBFS | | | 63 | | | | 4 |
| Fs = 3 GSps @ Fout = 100 MHz –3 dBFS | | 59 | 70 | | | | 1,6 |
| Highest spur level<br>First Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 100 MHz 0 dBFS | | | –68 | –56 | | | 1,6 |
| Fs = 3 GSps @ Fout = 400 MHz 0 dBFS | | | –61 | | dBm | | 4 |
| Fs = 3 GSps @ Fout = 100 MHz –3 dBFS | | | –72 | –60 | | | 1,6 |
| SFDR sensitivity & high spur level variation over power supplies | | | ±2 | | dB | | 4 |
| Signal independent Spur (clock-related spur) | | | | | | | |
| Fc/2 | | | –82 | | dBm | | 4 |
| Fc/4 | | | –85 | | dBm | | 4 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>20 MHz to 900 MHz broadband pattern,<br>25 MHz notch centered on 450 MHz | NPR | 45 | 49 | | dB | (2) | 1,6 |



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**Table 3-4.** AC Electrical Characteristics NRZ Mode (First Nyquist Zone) (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 9 | 9.6 | | Bit | [2] | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 56 | 58 | | dB | [2] | 1,6 |
| DAC self noise density at code 0 or 4095 | | | –163 | –154 | dBm/Hz | | 1,6 |

Notes: 1. See Section 3.6 on page 14 for explanation of test levels.

2. Figures in tables are derived from industrial screening; for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 7.2 on page 42 for effect of the balun on performances.

**Table 3-5.** AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Single-tone Spurious Free Dynamic Range | | | | | | | |
| MUX4:1 | | | | | | | |
| Fs = 3 GSps @ Fout = 100 MHz 0 dBFS | \|SFDR\| | 60 | 68 | | dBc | | 1,6 |
| Fs = 3 GSps @ Fout = 700 MHz 0 dBFS | | 55 | 62 | | | | 1,6 |
| Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS | | 52 | 61 | | | | 1,6 |
| Fs = 3 GSps @ Fout = 700 MHz –3 dBFS | | 57 | 66 | | | | 1,6 |
| MUX2:1 | | | | | | | |
| Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS | | 51 | 65 | | | | 1,6 |
| Highest spur level | | | | | | | |
| MUX4:1 | | | | | | | |
| Fs = 3 GSps @ Fout = 100 MHz 0 dBFS | | | –70 | –62 | dBm | | 1,6 |
| Fs = 3 GSps @ Fout = 700 MHz 0 dBFS | | | –64 | –56 | | | 1,6 |
| Fs = 3 GSps @ Fout = 1800 MHz 0 dBFS | | | –67 | –57 | | | 1,6 |
| Fs = 3 GSps @ Fout = 700 MHz –3 dBFS | | | –70 | –62 | | | 1,6 |
| MUX2:1 | | | | | | | |
| Fs = 1.5 GSps @ Fout = 700 MHz 0 dBFS | | | –68 | –53 | | | 1,6 |
| SFDR sensitivity & high spur level variation over power supplies | | | ±2 | | dB | | 4 |



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**Table 3-5.** AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone) (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Signal independent Spur (clock-related spur)<br>Fc<br>Fc/2 | | | <br>–29<br>–80 | | <br>dBm<br>dBm | | <br>4<br>4 |
| Fc/4 | | | –80 | | dBm | | 4 |
| DAC self noise density at code 0 or 4095 | | | –149 | –143 | dBm/Hz | | 1,6 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>20 MHz to 900 MHz broadband pattern,<br>25 MHz notch centered on 450 MHz | NPR | 45.5 | 50.2 | | dB | (2) | 1,6 |
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 9.1 | 9.9 | | Bit | (2) | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 56.5 | 61.2 | | dB | (2) | 1,6 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 1.5 GSps<br>10 MHz to 450 MHz broadband pattern,<br>12.5 MHz notch centered on 225 MHz | NPR | | 55.7 | | dB | (2) | 4 |
| Equivalent ENOB<br>Computed from NPR figure at 1.5 GSps | ENOB | | 10.8 | | Bit | (2) | 4 |
| Signal to Noise Ratio<br>Computed from NPR figure at 1.5 GSps | SNR | | 66.7 | | dB | (2) | 4 |

Notes:
1. See Section 3.6 on page 14 for explanation of test levels.
2. Figures in tables are derived from industrial screening; for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic. For further details please refer to Section 7.2 on page 42 for effect of the balun on performances.



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**Table 3-6.** AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)[2]

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Single-tone Spurious Free Dynamic Range<br>MUX4:1<br>Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS<br>Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS | \|SFDR\| | <br><br><br>49 | <br><br>60<br>57 | | dBc | | <br><br>4<br>1,6 |
| Highest spur level<br>MUX4:1<br>Fs = 3 GSps @ Fout =1600 MHz 0 dBFS<br>Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS | | | <br><br>–67<br>–66 | <br><br><br>–59 | dBm | | <br><br>4<br>1,6 |
| SFDR sensitivity & high spur level variation over power supplies | | | ±2 | | dB | | 4 |
| Signal independent Spur (clock-related spur)<br>Fc<br>Fc/2<br>Fc/4 | | | <br>–25<br>–80<br>–80 | | <br>dBm<br>dBm<br>dBm | | <br>4<br>4<br>4 |
| DAC self noise density at code 0 or 4095 | | | –143 | –139 | dBm/Hz | | 1,6 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>1520 MHz to 2200 MHz broadband pattern,<br>25 MHz notch centered on 1850 MHz | NPR | 39.5 | 44.0 | | dB | | 1,6 |
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 8.1 | 8.8 | | Bit | | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 50.5 | 55.0 | | dB | | 1,6 |

Notes: 1. See Section 3.6 on page 14 for explanation of test levels.
2. Please refer to Section 7.2 ”AC Performances” on page 42 to have detailed characterization results.



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**Table 3-7.** AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones)[2]

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Single-tone Spurious Free Dynamic Range | | | | | | | |
| 2nd Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS | \|SFDR\| | 44 | 52 | | dBc | | 1,6 |
| Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS | | | 60 | | | | 4 |
| 3rd Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 3800 MHz 0 dBFS | | 45 | 53 | | | | 1,6 |
| Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS | | 45 | 54 | | | | 1,6 |
| Highest spur level | | | | | | | |
| 2nd Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 1600 MHz 0 dBFS | | | –58 | –50 | dBm | | 1,6 |
| Fs = 3 GSps @ Fout = 2900 MHz 0 dBFS | | | –58 | | | | 4 |
| 3rd Nyquist | | | | | | | |
| Fs = 3 GSps @ Fout = 3800 MHz 0 dBFS | | | –60 | –52 | | | 1,6 |
| Fs = 3 GSps @ Fout = 4400 MHz 0 dBFS | | | –62 | –55 | | | 1,6 |
| SFDR sensitivity & high spur level variation over power supplies | | | ±2 | | dB | | 4 |
| Signal independent Spur (clock-related spur) | | | | | | | |
| Fc | | | –28 | | dBm | | 4 |
| Fc/2 | | | –80 | | dBm | | 4 |
| Fc/4 | | | –80 | | dBm | | 4 |
| DAC self noise density at code 0 or 4095 | | | –141 | –138 | dBm/Hz | | 1,6 |
| Noise Power Ratio (2nd Nyquist)<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>1520 MHz to 2200 MHz broadband pattern,<br>25 MHz notch centered on 1850 MHz | NPR | 38 | 42 | | dB | | 1,6 |
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 7.8 | 8.5 | | Bit | | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 49 | 53 | | dB | | 1,6 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>2200 MHz to 2880 MHz broadband pattern,<br>25 MHz notch centered on 2550 MHz | NPR | 38 | 42 | | dB | | 1,6 |



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**Table 3-7.** AC Electrical Characteristics RF Mode (Second and Third Nyquist Zones)[2] (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 7.8 | 8.5 | | Bit | | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 49 | 53 | | dB | | 1,6 |
| Noise Power Ratio<br>–14 dBFS peak to rms loading factor<br>Fs = 3 GSps<br>3050 MHz to 3700 MHz broadband pattern,<br>25 MHz notch centered on 3375 MHz | NPR | 38 | 40 | | dB | (2) | 1,6 |
| Equivalent ENOB<br>Computed from NPR figure at 3 GSps | ENOB | 7.8 | 8.2 | | Bit | (2) | 1,6 |
| Signal to Noise Ratio<br>Computed from NPR figure at 3 GSps | SNR | 49 | 51 | | dB | (2) | 1,6 |

Notes: 1. See Section 3.6 on page 14 for explanation of test levels.

2. Figures in tables are derived from industrial screening without any correction to take in account the balun effect, but for practical reasons (necessity to cover also 2nd and 3rd Nyquist Zones) the balun used for industrial test is not optimum for first Nyquist performances, and results when Fout or folded low order hamonics are between DC to 400 MHz are very pessimistic.

## 3.5 Timing Characteristics and Switching Performances

**Table 3-8.** Timing Characteristics and Switching Performances

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level[1] |
|---|---|---|---|---|---|---|---|
| **SWITCHING PERFORMANCE AND CHARACTERISTICS** | | | | | | | |
| Operating clock frequency<br>4:1 MUX mode<br>2:1 MUX mode | | <br>300<br>300 | | <br>3000<br>1500 | MHz | | 4 |
| **TIMING CHARACTERISTICS** | | | | | | | |
| Analog output rise/fall time | $T_{OR}$<br>$T_{OF}$ | | 60 | | ps | (2) | 4 |
| Data Tsetup (Fc = 3 Gsps) | | 250 | | | ps | (3) | 4 |
| Data Thold (Fc = 3 Gsps) | | 100 | | | ps | (3) | 4 |
| Max Input data rate (Mux 4:1) | | 75 | | 750 | MSps | | 4 |
| Max Input data rate (Mux 2:1) | | 150 | | 750 | MSps | | 4 |
| Master clock input jitter | | | | 100 | fs rms | (4) | 5 |
| DSP clock phase tuning steps | | | 0.5 | | Clock period | | 5 |
| Master clock to DSP, DSPN delay | TDSP | | 1.6 | | ns | | 4 |



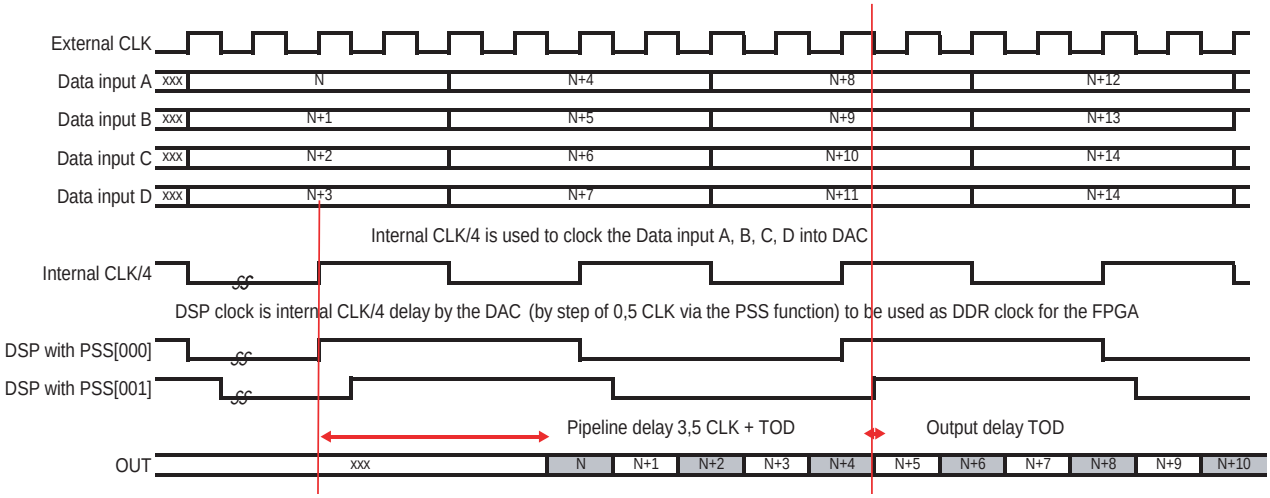
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**Table 3-8.** Timing Characteristics and Switching Performances (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note | Test level(1) |
|---|---|---|---|---|---|---|---|
| SYNC forbidden area lower bound (Fc = 3 Gsps) | $T_1$ | | 200 | | ps | (5)(6) | 4 |
| SYNC forbidden area upper bound (Fc = 3 Gsps) | $T_2$ | | 180 | | ps | (5)(6) | 4 |
| SYNC to DSP, DSPN<br>MUX 2:1<br>MUX4:1 | | | <br>880<br>1600 | | ps | | 4 |
| Data Pipeline Delay<br>MUX4:1<br>MUX2:1 | TPD | | <br>3.5<br>3.5 | | Clock period | | 4 |
| Data Output Delay | TOD | | 160 | | ps | | 4 |

Notes:
1. See Section 3.6 on page 14 for explanation of the test level.
2. Analog output rise/fall time measured from 20% to 80% of a full scale jump, after probe de-embedding.
3. Exclusive of period (pp) jitter on Data. Setup and hold time for DATA at input relative to DSP clock at output of the component, at PSS = 000; also applicable for IDC signal.
4. Master clock input jitter defined over 5 GHz bandwidth.
5. $T_C$ represents the master clock period. See Figure 3-3.
6. For EV12DS130A, please refer to erratasheet 1125

**Figure 3-1.** Timing Diagram for 4:1 MUX Principle of Operation OCDS[00]






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**Figure 3-2.** Timing Diagram for 2:1 MUX Principle of Operation OCDS[00]

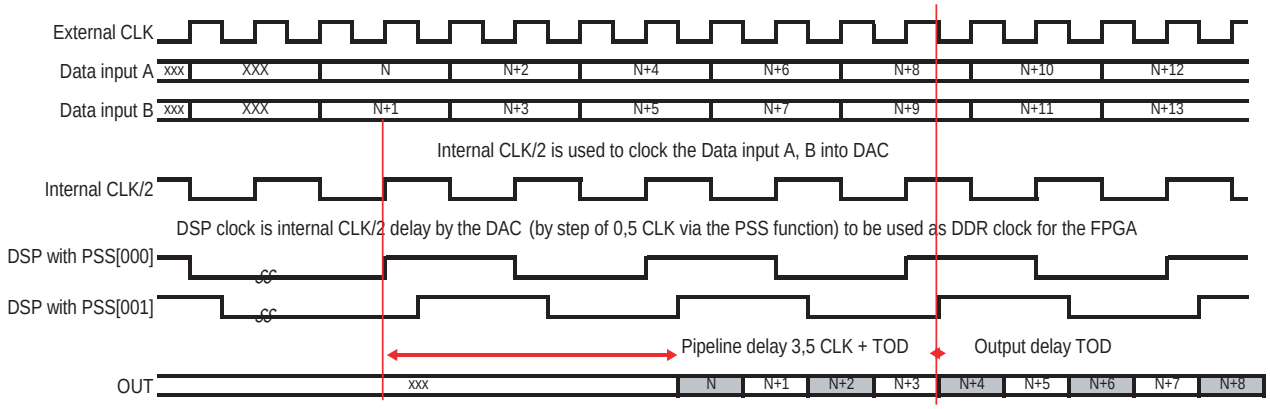
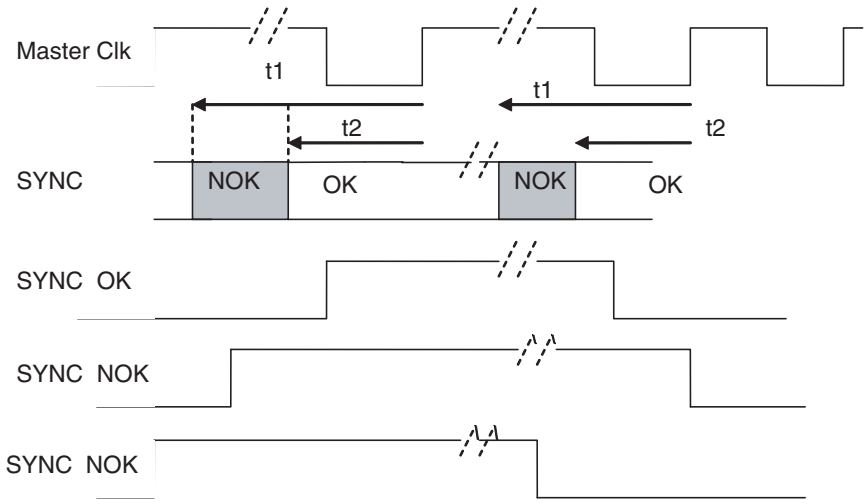



**Figure 3-3.** SYNC Timing Diagram




Please refer to Section 5.9 ”Synchronization functions for multi-DAC operation” on page 31.

## 3.6 Explanation of Test Levels

| | |
|---|---|
| 1 | 100% production tested at +25°C(1) |
| 2 | 100% production tested at +25°C(1), and sample tested at specified temperatures. |
| 3 | Sample tested only at specified temperatures |
| 4 | Parameter is guaranteed by design and/or characterization testing (thermal steady-state conditions at specified temperature) |
| 5 | Parameter value is guaranteed by design |
| 6 | 100% production tested over specified temperature range (for Space/Mil grade(2)) |

Only MIN and MAX values are guaranteed.

Notes: 1. Unless otherwise specified.

2. If applicable, please refer to “Ordering Information”



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## 3.7 Digital Input Coding Table

**Table 3-9.** Coding Table (Theorical values)

| Digital output msb……..lsb | Differential analog output |
|---|---|
| 000000000000 | –500 mV |
| 010000000000 | –250 mV |
| 011000000000 | –125 mV |
| 011111111111 | –0.122 mV |
| 100000000000 | 0.122 mV |
| 101000000000 | +125 mV |
| 110000000000 | +250 mV |
| 111111111111 | +500 mV |



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## 4. DEFINITION OF TERMS

| Abbreviation | Term | Definition |
|---|---|---|
| (Fs max) | *Maximum conversion Frequency* | Maximum conversion frequency |
| (Fs min) | *Minimum conversion frequency* | Minimum conversion Frequency |
| (SFDR) | *Spurious free dynamic range* | Ratio expressed in dB of the RMS signal amplitude, set at Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter 0 dB Full Scale), or in dBc (i.e, related to input signal level). |
| (HSL) | *High Spur Level* | Power of highest spurious spectral component expressed in dBm. |
| (ENOB) | *Effective Number Of Bits* | ENOB is determinated from NPR measurement with the formula: $ENOB = (NPR_{[dB]} + ILF_{[dB]}I - 3 - 1.76) / 6.02$ Where LF "Loading factor" is the ratio between the Gaussian noise standard deviation versus amplitude full scale. |
| (SNR) | *Signal to noise ratio* | SNR is determinated from NPR measurement with the formula: $SNR_{[dB]} = NPR_{[dB]} + ILF_{[dB]}I - 3$ Where LF "Loading factor" is the ratio between the Gaussian noise standard deviation versus amplitude full scale. |
| (DNL) | *Differential non linearity* | The Differential Non Linearity for an given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing point and that the transfer function is monotonic. |
| (INL) | *Integral non linearity* | The Integral Non Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all \|INL (i)\| |
| (TPD/TOD) | *Output delay* | The analog output propagation delay measured between the rising edge of the differential CLK, CLKN clock input (zero crossing point) and the zero crossing point of a full-scale analog output voltage step. TPD corresponds to the pipeline delay plus an internal propagation delay (TOD) including package access propagation delay and internal (on-chip) delays such as clock input buffers and DAC conversion time. |
| (NPR) | *Noise Power Ratio* | The NPR is measured to characterize the DAC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise pattern at the input to the DAC under test, the Noise Power Ratio is defined as the ratio of the average noise measured on the shoulder of the notch and inside the notch on the same integration bandwidth. |
| (VSWR) | *Voltage Standing Wave Ratio* | The VSWR corresponds to the insertion loss linked to power reflection. For example a VSWR of 1:2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected). |
| (IUCM) | *Input under clocking mode* | The IUCM principle is to apply a selectable division ratio between DAC section clock and the MUX section clock. |
| (PSS) | *Phase Shift Select* | The Phase Shift Select function allow to tune the phase of the DSPclock. |
| (OCDS) | *Output Clock Division Selectt* | It allows to divide the DSPclock frequency by the OCDS coded value factor |
| (NRZ) | *Non Return to Zero mode* | Non Return to Zero mode on analog output |
| (RF) | *Radio Frequency mode* | RF mode on analog output |
| (RTZ) | *Return to zero* | Return to zero mode on analog output |
| (NRTZ) | *Narrow return to zero* | Narrow return to zero mode on analog output |



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# 5. FUNCTIONAL DESCRIPTION

**Figure 5-1.** DAC Functional Diagram

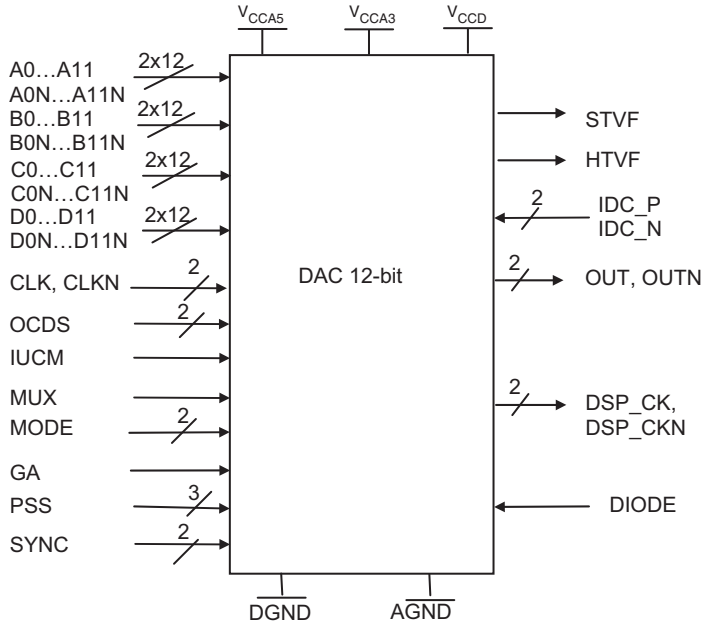



**Table 5-1.** Functions Description

| Name | Function | Name | Function |
|---|---|---|---|
| $V_{CCD}$ | 3.3V Digital Power Supply | CLK | In-phase Master clock |
| $V_{CCA5}$ | 5.0V Analog Power Supply | CLKN | Inverted phase Master clock |
| $V_{CCA3}$ | 3.3V Analog Power Supply | DSP_CK | In-phase Output clock |
| DGND | Digital Ground | DSP_CKN | Inverted phase Output clock |
| AGND | Analog ground (for analog supply reference) | PSS[0..2] | Phase shift select |
| A[11…0] | In-phase digital input Port A | GA | Gain Adjust |
| A[11..0]N | Inverted phase digital input Port A | MUX | Multiplexer Selection |
| B[11…0] | In-phase digital input Port B | MODE[0..1] | DAC Mode: NRZ, RTZ, NRTZ, RF |
| B[11..0]N | Inverted phase digital input Port B | STVF | Setup time Violation flag |
| C[11…0] | In-phase digital input Port C | HTVF | Hold time Violation flag |
| C[11..0]N | Inverted phase digital input Port C | IDC_P, IDC_N | Input data check |
| D[11…0] | In-phase digital input Port D | OCDS[0..1] | Output Clock Division factor Selection |
| D[11..0]N | Inverted phase digital input Port D | Diode | Diode for temperature monitoring |
| OUT | In-phase analog output | SYNC/SYNCN | Synchronization signal (Active High) |
| OUTN | Inverted phase analog output | IUCM | Input UnderClocking Mode |



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## 5.1 DSP Output Clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.

The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS settings. The DSP clock frequency is equal to (sampling frequency / [2N*X]) where N is the MUX ratio and X is the output clock division factor, determined by OCDS[0..1] bits.

For example, in a 4:1 MUX ratio application with a sampling clock of 3 GHz and OCDS set to “00” (ie. Factor of 1), the input data rate is 750 MSps and the DSP clock frequency is 375 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted using the PSS[2:0] bits (refer to Section 5.5 on page 26) in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.

The HTVF and STVF bits should be used to check whether the timing between the FPGA and the DAC is correct. HTVF and STVF bits will indicate whether the DAC and FPGA are aligned or not. PSS bits should then be used to shift the DSP clock and thus the input data of the DAC, so that a correct timing is achieved between the FPGA and the DAC.

**Important note: Maximum supported sampling frequency when using DSP to clock digital data is 2.1 Gsps on EV12DS130B. Please refer to application note AN1141 to use EV12DS130B at sampling frequency beyond 2.1 GHz.**

## 5.2 Multiplexer

Two multiplexer ratio are allowed:

- 4:1 which allows operation at full sampling rate (ie. 3 GHz)
- 2:1 which can only be used up to 1.5 GHz sampling rate, except in IUCM mode

| Label | Value | Description |
|---|---|---|
| MUX | 0 | 4:1 mode |
| | 1 | 2:1 mode |

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

## 5.3 MODE Function

| Label | Value | Description | Default Setting (Not Connected) |
|---|---|---|---|
| MODE[1:0] | 00 | NRZ mode | 11<br>RF mode |
| | 01 | Narrow RTZ (a.k.a. NRTZ) mode | |
| | 10 | RTZ Mode (50%) | |
| | 11 | RF mode | |

The MODE function allows choosing between NRZ, NRTZ, RTZ and RF functions. NRZ and narrow RTZ should be chosen for use in 1$^{st}$ Nyquist zone while RTZ should be chosen for use in 2$^{nd}$ and RF for 3$^{rd}$ Nyquist zones.



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Theory of operation: see following subsections for time domain waveform of the different modes.

Ideal equations describing max available Pout for frequency domain in the four modes are given hereafter, with X = normalized output frequency (that is Fout/Fclock, edges of Nyquist zones are then at X = 0 1/2 1 3/2 2 …). Due to limited bandwidth, an extra term must be added to take in account a first order low pass filter.

**NRZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{|k \cdot \text{sinc}(k \cdot \pi \cdot X)|}{0.893} \right]$$

where sinc(x) = sin(x)/x, and k = 1

**NRTZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{|k \cdot \text{sinc}(k \cdot \pi \cdot X)|}{0.893} \right] \qquad k = \frac{\text{Tclk} - \text{T}\tau}{\text{Tclk}}$$

where $\text{T}\tau$ is width of reshaping pulse, $\text{T}\tau$ is about 75ps.

**RTZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{|k \cdot \text{sinc}(k \cdot \pi \cdot X)|}{0.893} \right]$$

where k is the duty cycle of the clock presented at the DAC input, please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zones. Ideally k = 1/2.

**RF mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{\left| k \cdot \text{sinc}\left( \frac{k \cdot \pi \cdot X}{2} \right) \cdot \sin\left( \frac{k \cdot \pi \cdot X}{2} \right) \right|}{0.893} \right]$$

where k is as per in NRTZ mode.

As a consequence:

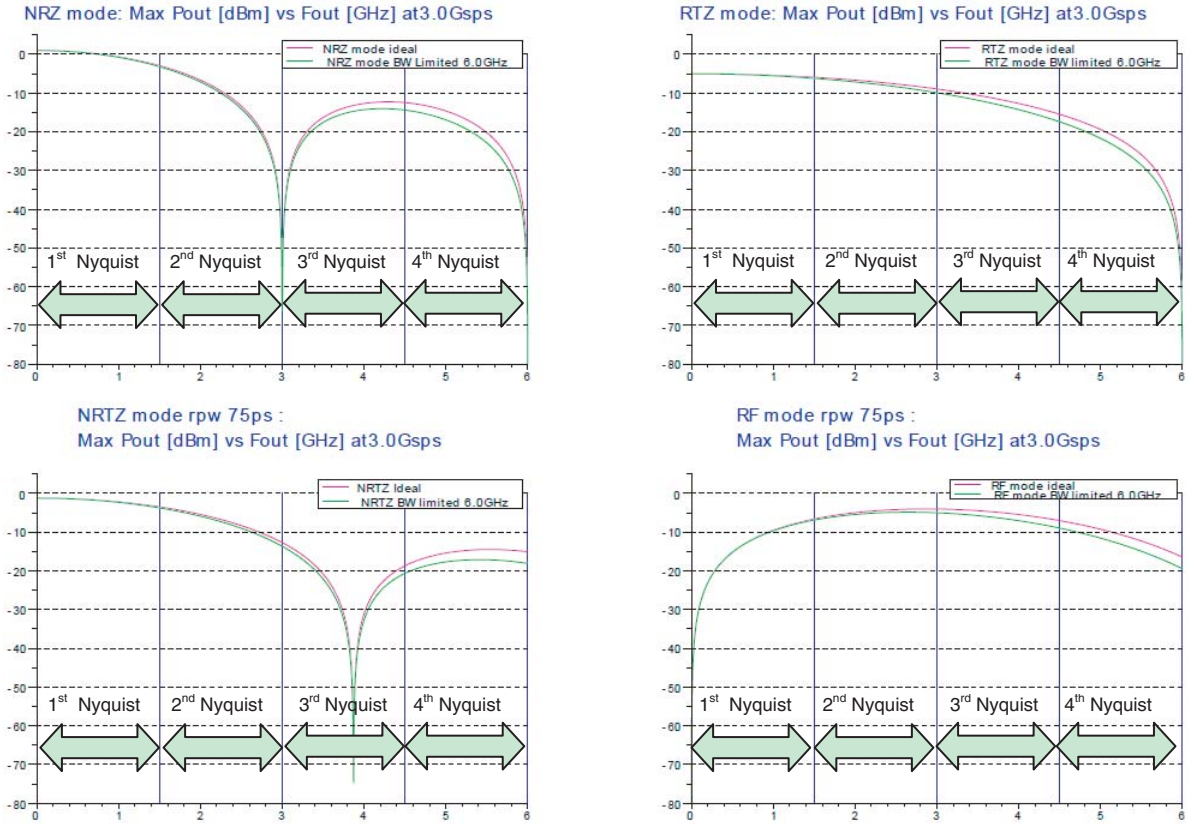
- NRZ mode offers max power for 1st Nyquist operation
- RTZ mode offers slow roll off for 2nd Nyquist or 3rd Nyquist operation
- RF mode offers maximum power over 2nd and 3rd Nyquist operation
- NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. This is the most relevant in term of performance for operation over 1st and beginning of 2nd Nyquist zone. Depending on the sampling rate the zero of transmission moves in the 3rd Nyquist zone from begin to end when sampling rate increases.



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Note in the two following figures: Pink line is ideal equation's result, and green line includes a first order 6 GHz cut-off low pass filter to take into account finite bandwidth effect due to die and package.

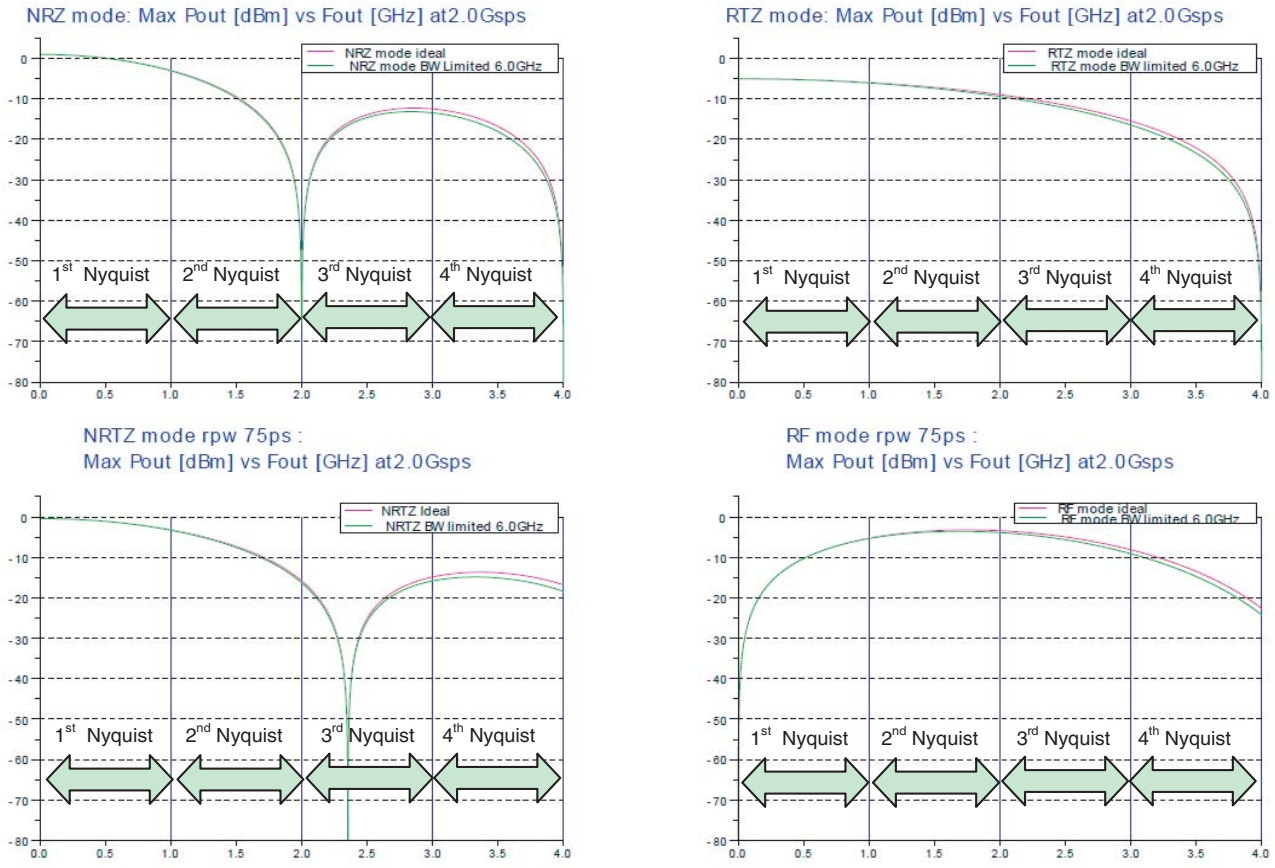
**Figure 5-2.** Max Available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 3 Gsps, over four Nyquist Zones, Computed for Tτ = 75 ps






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**Figure 5-3.** Max available Pout[dBm] at Nominal Gain vs Fout[GHz] in the Four Output Modes at 2 Gsps, over four Nyquist Zones, Computed for Tτ = 75 ps

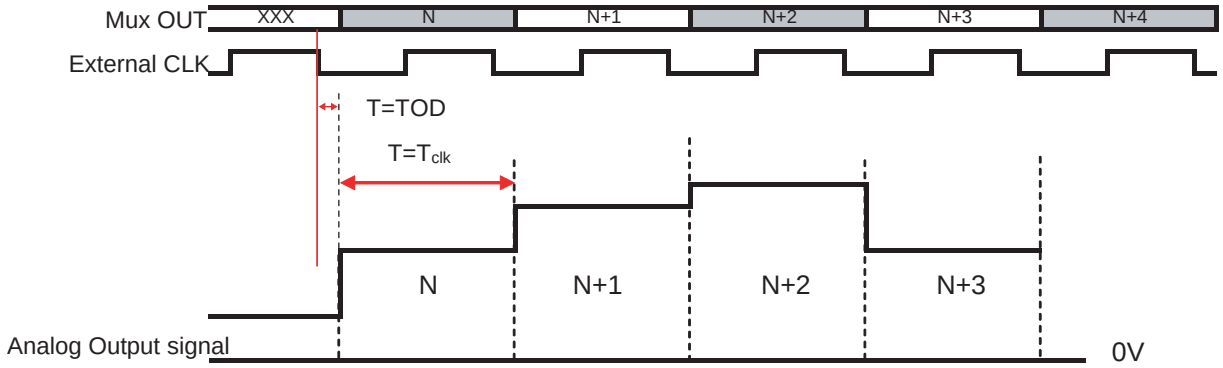



### 5.3.1 NRZ Output Mode

This mode does not allow for operation in the 2nd Nyquist zone because of the Sinx/x notch.

The advantage is that it gives good results at the beginning of the 1st Nyquist zone (less attenuation than in RTZ architecture), it removes the parasitic spur at the clock frequency (in differential).

**Figure 5-4.** NRZ Timing Diagram





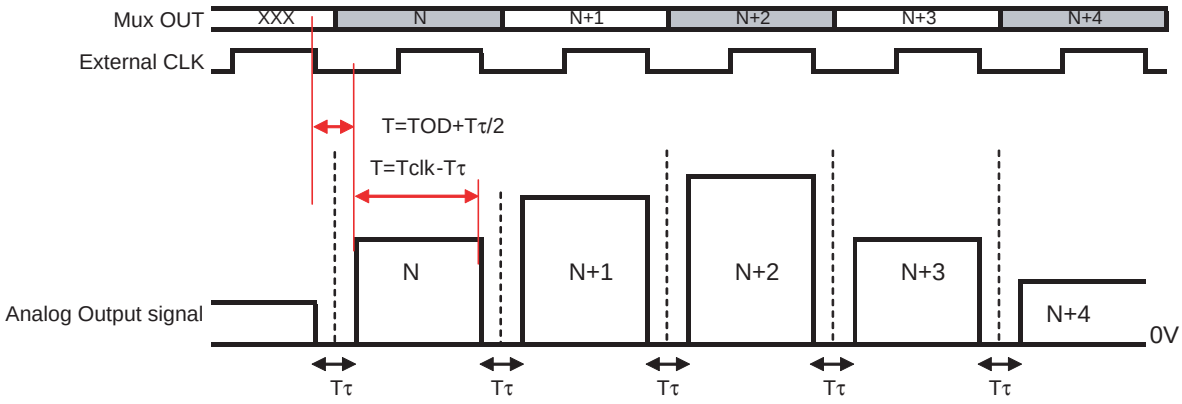
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### 5.3.2 Narrow RTZ Mode (NRTZ Mode)

This mode has the following advantages:

- Optimized power in 1st Nyquist zone
- Extended dynamic through elimination of noise on transition edges
- Improved spectral purity (see Section 7.2.3 on page 50)
- Trade off between NRZ and RTZ

**Figure 5-5.** Narrow RTZ Timing Diagram




Note: Tτ is independent of Fclock.

### 5.3.3 RTZ Mode

The advantage of the RTZ mode is to enable the operation in the 2nd zone but the drawback is clearly to attenuate more the signal in the first Nyquist zone.

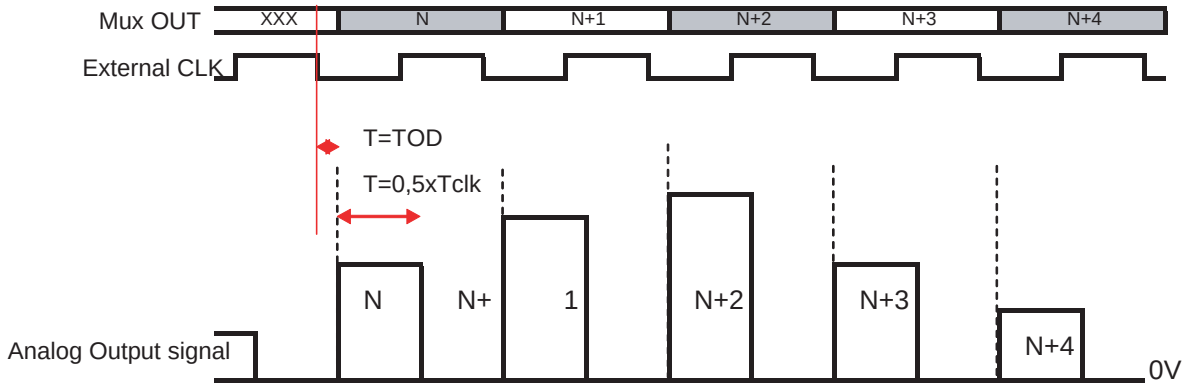
Advantages:

- Extended roll off of sinc
- Extended dynamic through elimination of hazardous transitions

Weakness:

- By construction clock spur at Fs.

**Figure 5-6.** RTZ Timing Diagram






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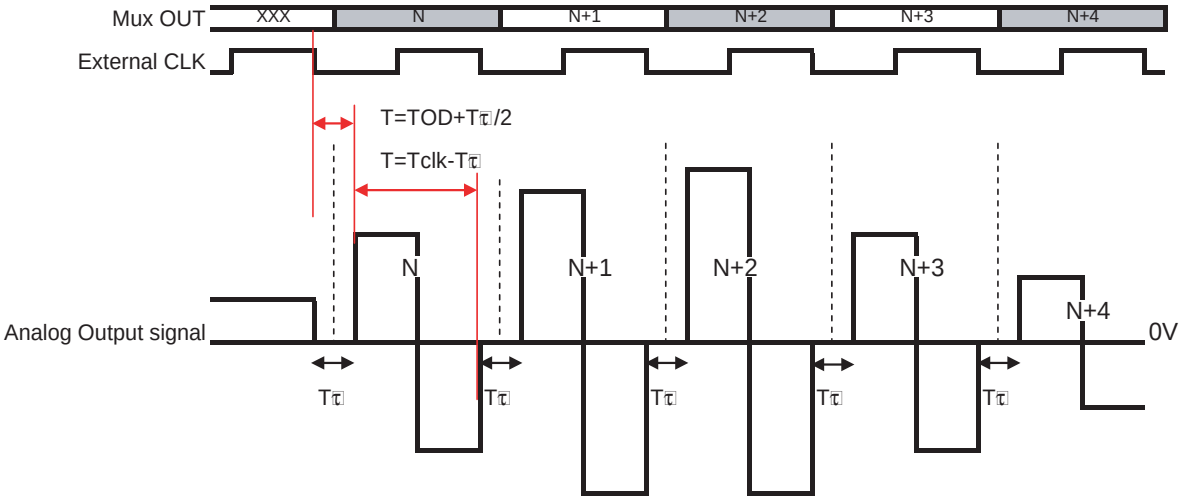
### 5.3.4 RF Mode

RF mode is optimal for operation at high output frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, RF mode presents a notch at DC and 2N*Fs, and minimum attenuation for Fout = Fs.

Advantages:

- Optimized for 2nd and 3rd Nyquist operation
- Extended dynamic range through elimination of hazardous transitions.
- Clock spur pushed to 2.Fs

**Figure 5-7.** RF Timing Diagram




Note: The central transition is not hazardous but its elimination allows to push clock spur to 2.Fs
Tτ is independent of Fclock.

## 5.4 Input Under Clocking Mode (IUCM), Principle and Spectral Response

An Input Under Clocking Mode has been added to the DAC in order to allow the DAC input data rate to be at half the nominal rate with respect of the DAC sampling rate.

When the under clocking mode is activated, the DAC expects data at half the nominal rate: if the DAC works at Fs sampling rate, then in 4:1 MUX mode, the input data rate should be Fs/4 and the DSP clock should be Fs/(2N*OCDS), with N = MUX ratio and OCDS = OCDS Ratio.

When the IUCM is active, the input data rate can be Fs/8 and the DSP clock frequency is Fs/(2N*OCDS*2), with N = MUX ratio and OCDS = OCDS Ratio. This means that in input under clocking mode, the DAC is capable to treat data at half the nominal rate. In this case, the DSP clock is also half its nominal speed.

| Label | Logic Value | Description |
|---|---|---|
| IUCM | 0 | Input Under Clocking Mode inactive |
| | 1 | Input Under Clocking Mode active |



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To disable this mode, the IUCM pin must be connected to GND.

To enable this mode, IUCM must be connected to $V_{CCD}$ or left unconnected

The IUCM mode affects spectral response of the different modes.

The first effect is that Nyquist zone edges are not anymore at n*Fclock/2 but at n*/Fclock/4 (direct consequence of the division by 2 of the data rate).

The second effect is the modification of the equations ruling the spectral responses in the different modes.

Ideal equations describing max available Pout for frequency domain in the four output modes when IUCM mode is activated are given hereafter, with X= normalised output frequency (that is Fout/Fclock, edges of Nyquist Zones are then at X = 0, 1/4, 1/2, 3/4, 1, …)

In fact due to limited bandwidth, an extra term must be added to take in account a first order low pass filter with a 6 GHz cut-off frequency.

**NRZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{\left| k \cdot \text{sinc}(k \cdot \pi \cdot X) . \cos(\pi \cdot X) \right|}{0.893} \right]$$

where sinc(x) = sin(x)/x, and k = 1

**NRTZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{\left| k \cdot \text{sinc}(k \cdot \pi \cdot X) . \cos(\pi \cdot X) \right|}{0.893} \right] \qquad k = \frac{\text{Tclk} - T\tau}{\text{Tclk}}$$

where $T\tau$ is width of reshaping pulse, $T\tau$ is about 75ps.

**RTZ mode:**

$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{\left| k \cdot \text{sinc}(k \cdot \pi \cdot X) . \cos(\pi \cdot X) \right|}{0.893} \right]$$

where k is the duty cycle of the clock presented at the DAC input, please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zones. Ideally k = 1/2.

**RF mode:**

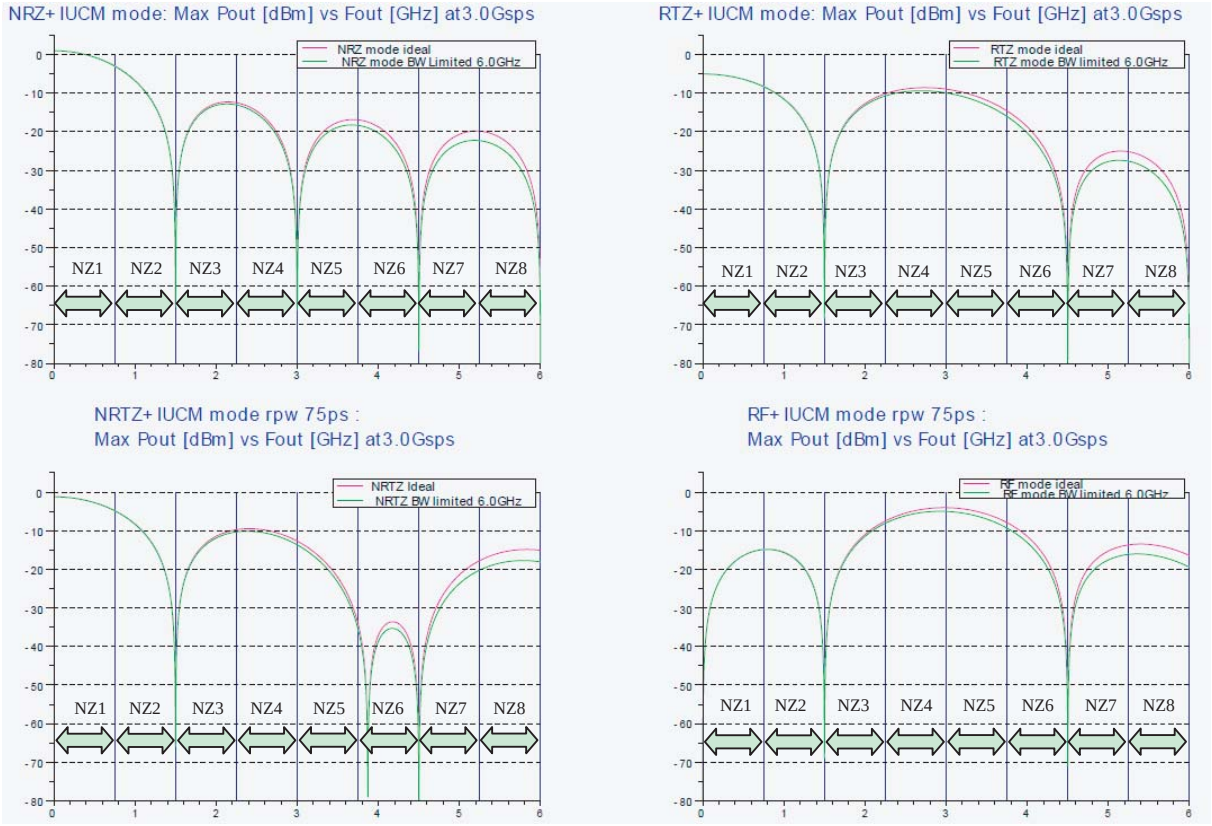
$$\text{Pout}(X) = 20 \cdot \log_{10} \cdot \left[ \frac{\left| k \cdot \text{sinc}\left( \frac{k \cdot \pi \cdot X}{2} \right) \cdot \sin\left( \frac{k \cdot \pi \cdot X}{2} \right) . \cos(\pi . X) \right|}{0.893} \right]$$

where k is as per in NRTZ mode.



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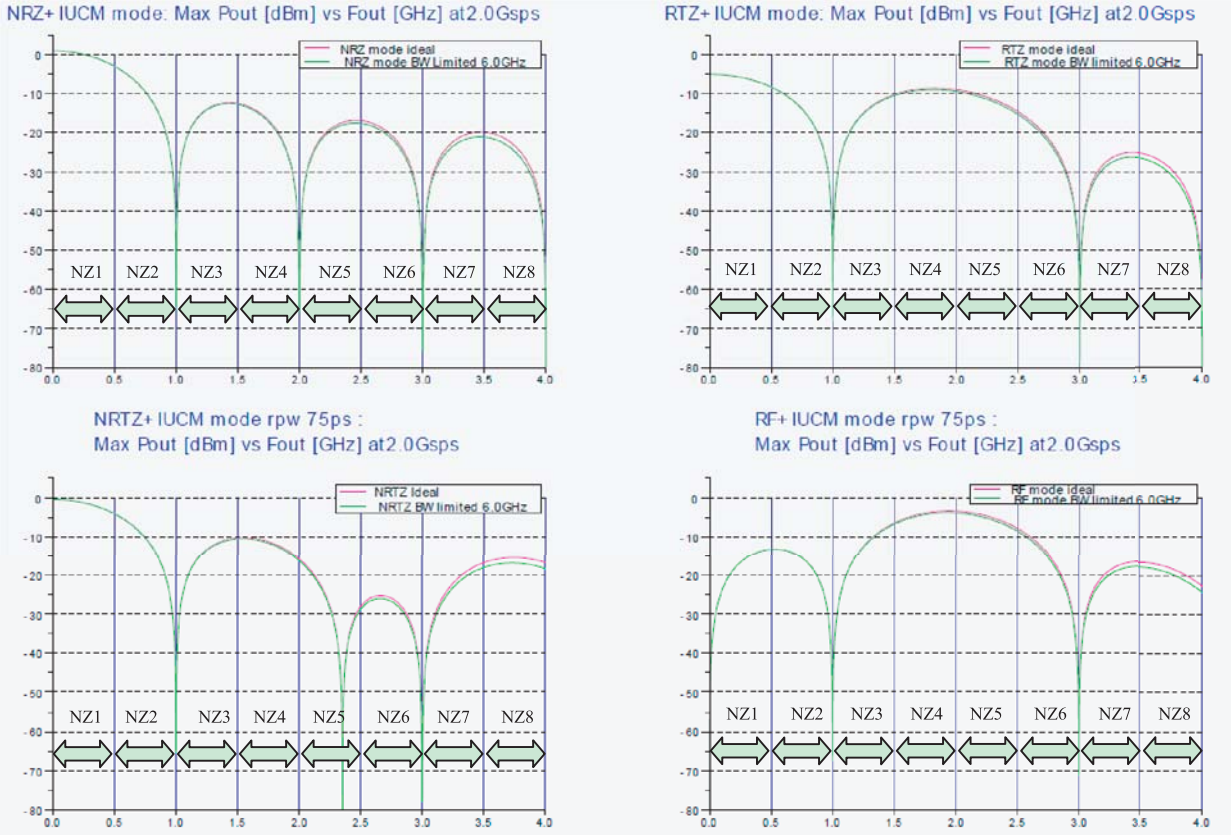
**Figure 5-8.** Max available Pout[dBm] at nominal gain vs Fout[GHz] in the four output modes at 3 GSps, combined with IUCM, over four nyquist zones, computed for Tτ =75 ps.






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**Figure 5-9.** Max available Pout[dBm] at nominal gain vs Fout[GHz] in the four output modes at 2 GSps, combined with IUCM, over four nyquist zones, computed for Tτ = 75 ps




## 5.5 PSS (Phase Shift Select Function)

It is possible to adjust the timings between the sampling clock and the DSP output clock (which frequency is given by the following formula: Sampling clock / 2NX where N is the MUX ratio, X the output clock division factor).

The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).

Three bits are provided for the phase shift function: PSS[2:0].

By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).



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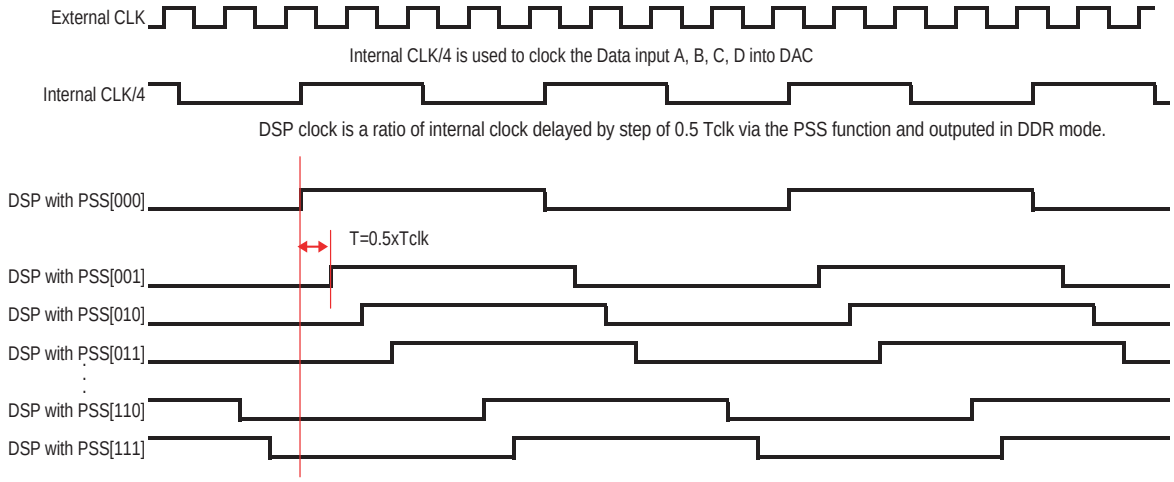
**Table 5-2.** PSS Coding Table

| Label | Value | Description |
|---|---|---|
| PSS[2:0] | 000 | No additional delay on DSP clock |
| | 001 | 0.5 input clock cycle delay on DSP clock |
| | 010 | 1 input clock cycle delay on DSP clock |
| | 011 | 1.5 input clock cycle delay on DSP clock |
| | 100 | 2 input clock cycle delay on DSP clock |
| | 101 | 2.5 input clock cycle delay on DSP clock |
| | 110 | 3 input clock cycle delay on DSP clock |
| | 111 | 3.5 input clock cycle delay on DSP clock |

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the HTVF and STVF bits should be monitored. Refer to Section 5.7 on page 29.

Note: In MUX 4:1 mode the 8 settings are relevant, in MUX 2:1 only the four first settings are relevant since the four last ones will yield exactly the same results.

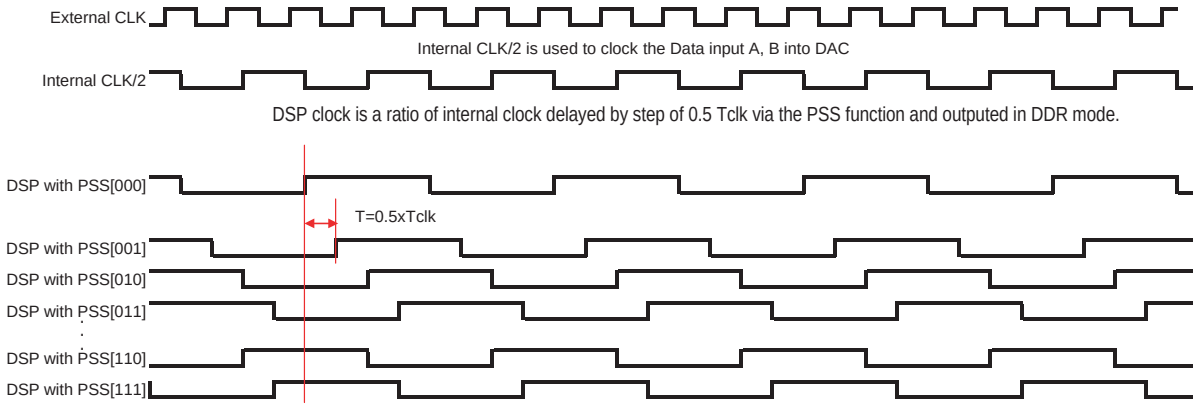
**Figure 5-10.** PSS Timing Diagram for 4:1 MUX, OCDS[00]





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**Figure 5-11.** PSS Timing Diagram for 2:1 MUX, OCDS[00]




## 5.6 Output Clock Division Select Function

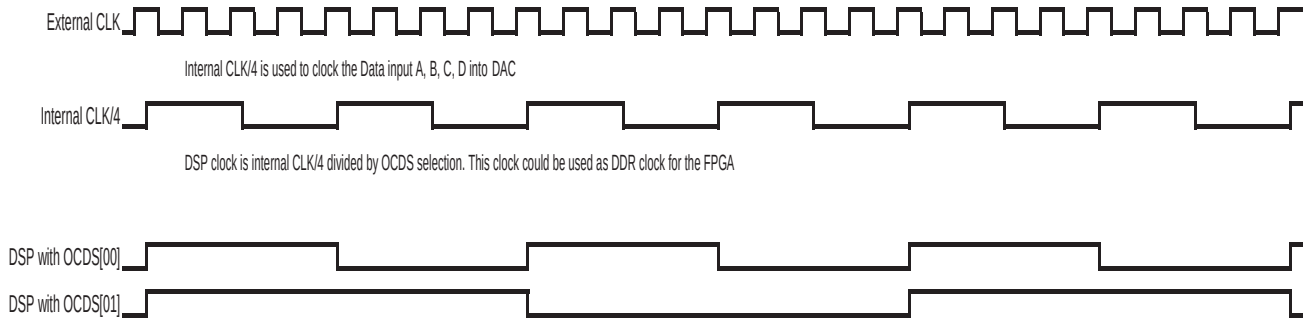
It is possible to change the DSP clock internal division factor from 1 to 2 with respect to the sampling clock/2N where N is the MUX ratio. This is possible via the OCDS "Output Clock Division Select" bits.

OCDS is used to obtain a synchronization clock for the FPGA slow enough to allow the FPGA to operate with no further internal division of this clock, thus its internal phase is determined by the DSP clock phase. This is useful in a system with multiple DACs and multiple FPGAs to guarantee deterministic phase relationship between the FPGAs after a synchronization of all the DACs.

**Table 5-3.** OCDS[1:0] Coding Table

| Label | Value | Description |
|---|---|---|
| OCDS [1:0] | 00 | DSP clock frequency is equal to the sampling clock divided by 2N |
| | 01 | DSP clock frequency is equal to the sampling clock divided by 2N*2 |
| | 10 | Not allowed |
| | 11 | Not allowed |

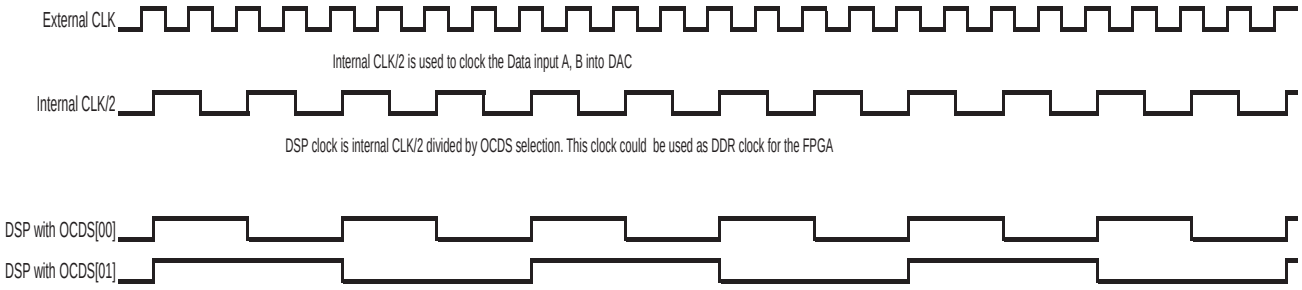
**Figure 5-12.** OCDS Timing Diagram for 4:1 MUX






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**Figure 5-13.** OCDS Timing Diagram for 2:1 MUX




## 5.7 Synchronization FPGA-DAC: IDC_P, IDC_N, HTVF and STVF Functions

IDC_P, IDC_N: Input Data check function (LVDS signal).

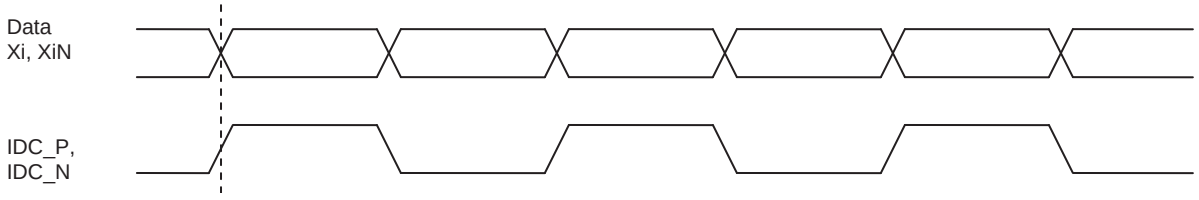
HTVF: Hold Time Violation Flag. (cmos3.3V signal)

STVF: Setup Time Violation Flag. (cmos3.3V signal)

IDC signal is toggling at each cycle synchronously with other data bits. It should be considered as a DAC input data that toggles at each cycle.

This signal should be generated by the FPGA in order for the DAC to check in real-time if the timings between the FPGA and the DAC are correct.

**Figure 5-14.** IDC Timing vs Data Input




The information on the timings is then given by HTVF, STVF signals (flags).

**Table 5-4.** HTVF, STVF Coding Table

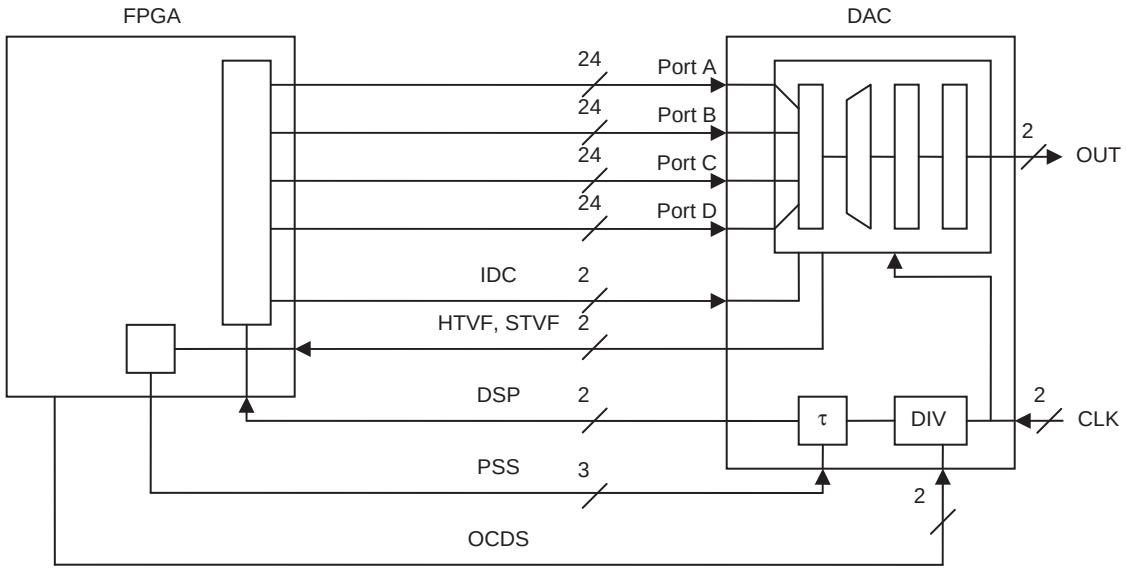
| Label | Value | Description |
|---|---|---|
| HTVF | 0 | SYNCHRO OK |
| | 1 | Data Hold time violation detected |
| STVF | 0 | SYNCHRO OK |
| | 1 | Data Setup time violation detected |

During monitoring STVF indicates setup time of data violation (Low -> OK, High -> Violation), HTVF indicates hold time of data violation (Low -> OK, High -> Violation).



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**Figure 5-15.** FPGA to DAC Synoptic




Principle of Operation:

The Input Data Check pair (IDC_P, IDC_N) will be sampled three times with half a master clock period shift (the second sample being synchronous with all the data sampling instant), these three samples will be compared, and depending on the results of the comparison a violation may be signalled.

- Violation of setup time -> STVF is high level
- Violation of hold time -> HTVF is high level

In case of violation of timing (setup or hold) the user has two solutions:

- Shift phase in the FPGA PLL (if this functionality is available in FPGA) for changing the internal timing of DATA and Data Check signal inside FPGA.
- Shift the DSP clock timing (Output clock of the DAC which can be used for FPGA synchronization – refer to Section 5.5 on page 26), in this case this shift also shift the internal timing of FPGA clock.

Note: When used, it should be routed as the data signals (same layout rules and same length). if not used, it should be driven to an LVDS low or high level.

For further details, refer to application note AN1087.



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## 5.8 OCDS, MUX Combinations Summary

**Table 5-5.** OCDS, IUCM, MUX, PSS Combinations Summary

| MUX | | IUCM | | OCDS | | PSS range | Data rate | Comments |
|---|---|---|---|---|---|---|---|---|
| 0 | 4:1 | 1 | ON | 00 | DSP clock division factor 16 | 0 to 7/(2Fs) by 1/(2Fs) steps | Fs/8 | Refer to Section 5.6 |
| 0 | | 1 | | 01 | DSP clock division factor 32 | | | |
| 0 | | 1 | | 10 | Not allowed | | | |
| 0 | | 1 | | 11 | Not allowed | | | |
| 0 | | 0 | OFF, normal mode | 00 | DSP clock division factor 8 | 0 to 7/(2Fs) by 1/(2Fs) steps | Fs/4 | Refer to Section 5.6 |
| 0 | | 0 | | 01 | DSP clock division factor 16 | | | |
| 0 | | 0 | | 10 | Not allowed | | | |
| 0 | | 0 | | 11 | Not allowed | | | |
| 1 | 2:1 | 1 | ON | 00 | DSP clock division factor 8 | 0 to 7/(2Fs) by 1/(2Fs) steps | Fs/4 | Not recommended mode, not guaranteed |
| 1 | | 1 | | 01 | DSP clock division factor 16 | | | |
| 1 | | 1 | | 10 | Not allowed | | | |
| 1 | | 1 | | 11 | Not allowed | | | |
| 1 | | 0 | OFF, normal mode | 00 | DSP clock division factor 4 | 0 to 7/(2Fs) by 1/(2Fs) steps | Fs/2 | Refer to Section 5.6 |
| 1 | | 0 | | 01 | DSP clock division factor 8 | | | |
| 1 | | 0 | | 10 | Not allowed | | | |
| 1 | | 0 | | 11 | Not allowed | | | |

Note: Behaviour according to MUX, OCDS and PSS combination is independent of output mode (MODE).

## 5.9 Synchronization functions for multi-DAC operation

In order to synchronize the timings, a SYNC operation can be generated.

After the application of the SYNC signal the DSP clock from the DAC will stop for a period and after a constant and known time the DSP clock will start up again.

There are two SYNC functions integrated in this DAC:

- a power up reset, which is triggered by the power supplies if the dedicated power up sequence is applied Vccd => Vcca3 => Vcca5;
- External SYNC pulse applied on (SYNC, SYNCN).

The external SYNC is LVDS compatible (same buffer as for the digital input data). It is active high.

Depending on the settings for OCDS, PSS and also the MUX ratio the width of the SYNC pulse must be greater than a certain number of external clock pulses. It is also necessary that the sync pulse be synchronized with the system clock and is an integer number of clock pulses. See application note (ref 1087) for further details.



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**Figure 5-16.** Reset Timing Diagram (4:1 MUX)

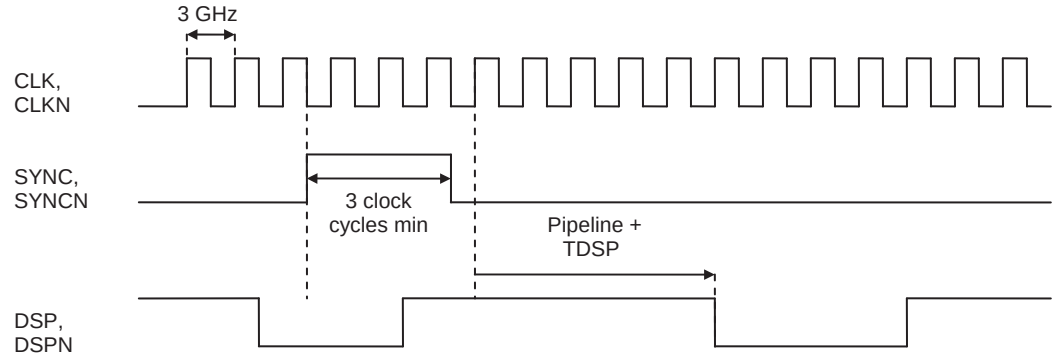
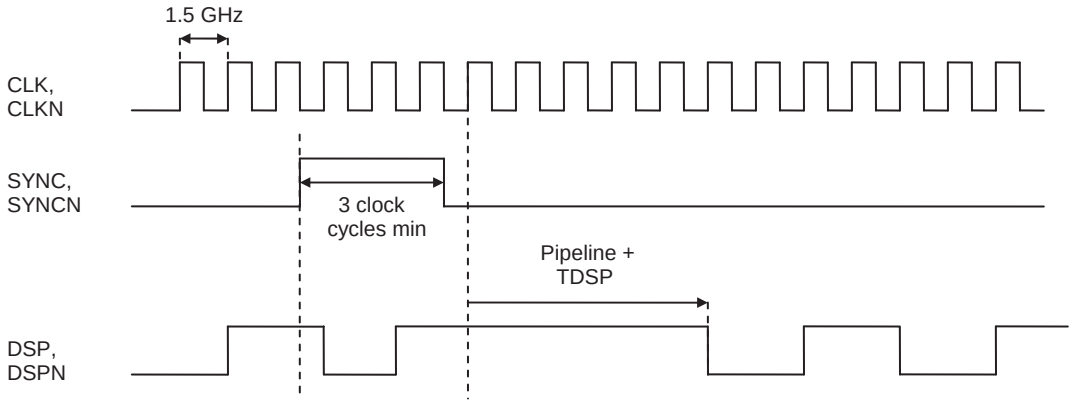



**Figure 5-17.** Reset Timing Diagram (2:1 MUX)




**Important note:**

**For EV12DS130A:**

- **See erratasheet (ref 1125) for SYNC condition of use.**
- **SYNC, SYNCN pins have to be driven.**

**For EV12DS130B:**

- **SYNC, SYNCN pins can be left floating if unused.**
- **No specific timing constraints (other than T1 and T2) are required.**

## 5.10 Gain Adjust GA Function

This function allows to adjust the internal gain of the DAC to cancel the initial gain deviation.
The gain of the DAC can be adjusted by ±11% by tuning the voltage applied on GA by varying GA potential from 0 to $V_{CCA3}$.
GA max is given for GA = 0 and GA min for GA = $V_{CCA3}$

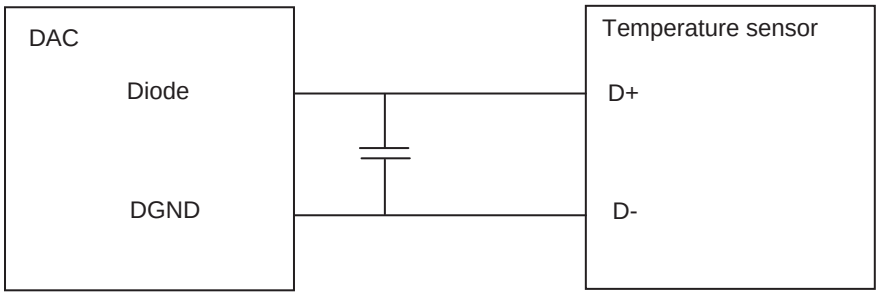


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## 5.11 Diode Function

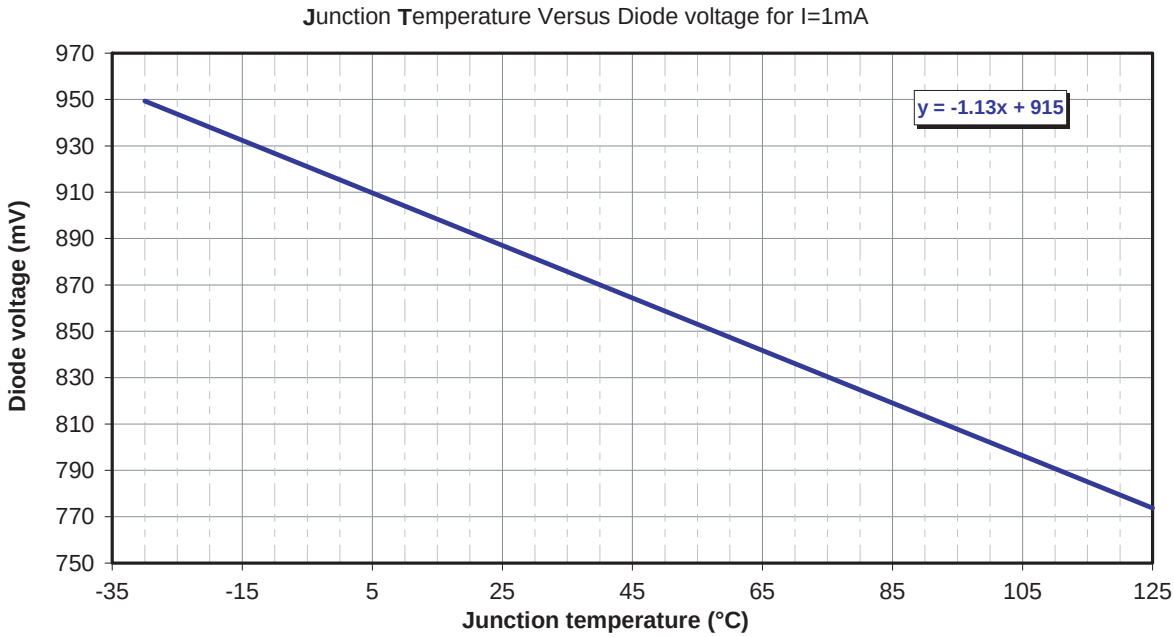
A diode is available to monitor the die junction temperature of the DAC.
For the measurement of die junction temperature, you may use a temperature sensor.

**Figure 5-18.** Temperature DIODE Implementation




In characterization measurement a current of 1 mA is applied on the DIODE pin. The voltage across the DIODE pin and the DGND pin gives the junction temperature using the intrinsic diode characteristics below Figure 5-19.

**Figure 5-19.** Diode Characteristics for Die Junction Monitoring

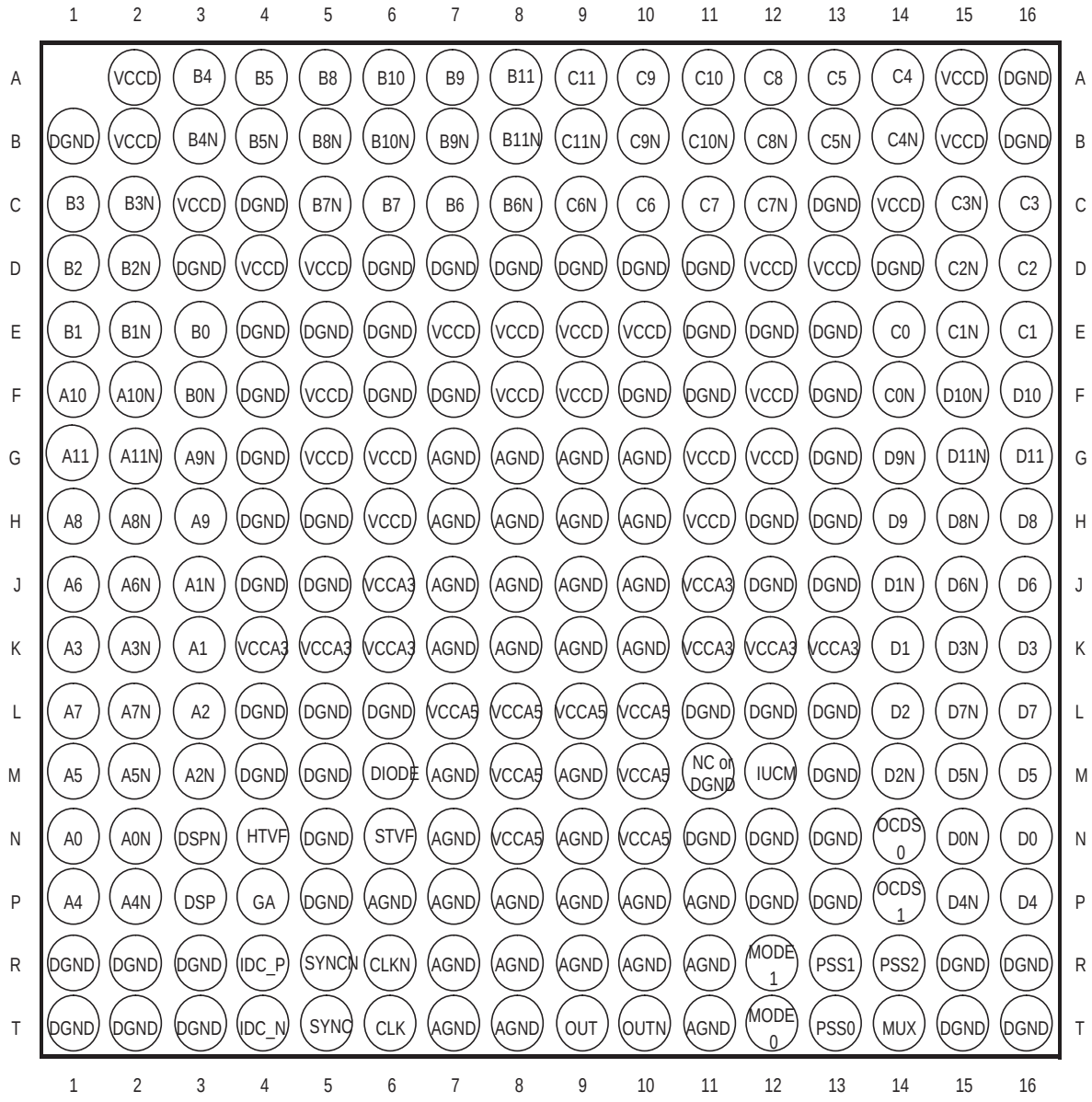




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# 6. PIN DESCRIPTION

**Figure 6-1.** Pinout View (Top View)

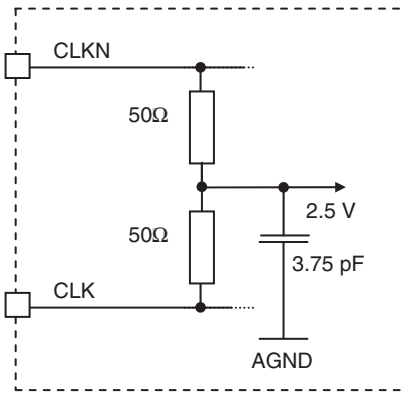


| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | VCCD | B4 | B5 | B8 | B10 | B9 | B11 | C11 | C9 | C10 | C8 | C5 | C4 | VCCD | DGND | A |
| B | DGND | VCCD | B4N | B5N | B8N | B10N | B9N | B11N | C11N | C9N | C10N | C8N | C5N | C4N | VCCD | DGND | B |
| C | B3 | B3N | VCCD | DGND | B7N | B7 | B6 | B6N | C6N | C6 | C7 | C7N | DGND | VCCD | C3N | C3 | C |
| D | B2 | B2N | DGND | VCCD | VCCD | DGND | DGND | DGND | DGND | DGND | DGND | VCCD | VCCD | DGND | C2N | C2 | D |
| E | B1 | B1N | B0 | DGND | DGND | DGND | VCCD | VCCD | VCCD | VCCD | DGND | DGND | DGND | C0 | C1N | C1 | E |
| F | A10 | A10N | B0N | DGND | VCCD | DGND | DGND | VCCD | VCCD | DGND | DGND | VCCD | DGND | C0N | D10N | D10 | F |
| G | A11 | A11N | A9N | DGND | VCCD | VCCD | AGND | AGND | AGND | AGND | VCCD | VCCD | DGND | D9N | D11N | D11 | G |
| H | A8 | A8N | A9 | DGND | DGND | VCCD | AGND | AGND | AGND | AGND | VCCD | DGND | DGND | D9 | D8N | D8 | H |
| J | A6 | A6N | A1N | DGND | DGND | VCCA3 | AGND | AGND | AGND | AGND | VCCA3 | DGND | DGND | D1N | D6N | D6 | J |
| K | A3 | A3N | A1 | VCCA3 | VCCA3 | VCCA3 | AGND | AGND | AGND | AGND | VCCA3 | VCCA3 | VCCA3 | D1 | D3N | D3 | K |
| L | A7 | A7N | A2 | DGND | DGND | DGND | VCCA5 | VCCA5 | VCCA5 | VCCA5 | DGND | DGND | DGND | D2 | D7N | D7 | L |
| M | A5 | A5N | A2N | DGND | DGND | DIODE | AGND | VCCA5 | AGND | VCCA5 | NC or DGND | IUCM | DGND | D2N | D5N | D5 | M |
| N | A0 | A0N | DSPN | HTVF | DGND | STVF | AGND | VCCA5 | AGND | VCCA5 | DGND | DGND | DGND | OCDS 0 | D0N | D0 | N |
| P | A4 | A4N | DSP | GA | DGND | AGND | AGND | AGND | AGND | AGND | AGND | DGND | DGND | OCDS 1 | D4N | D4 | P |
| R | DGND | DGND | DGND | IDC_P | SYNCN | CLKN | AGND | AGND | AGND | AGND | AGND | MODE 1 | PSS1 | PSS2 | DGND | DGND | R |
| T | DGND | DGND | DGND | IDC_N | SYNC | CLK | AGND | AGND | OUT | OUTN | AGND | MODE 0 | PSS0 | MUX | DGND | DGND | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |



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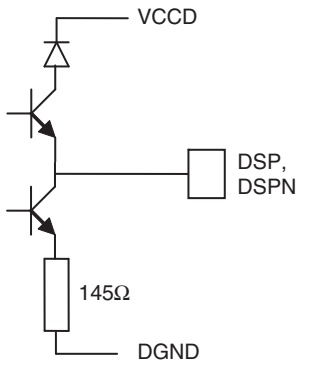
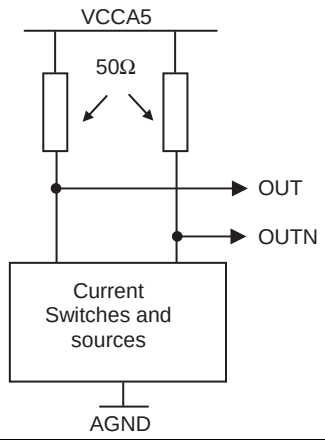
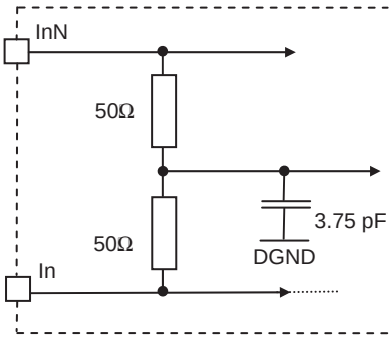
**Table 6-1.** Pinout Table

| Signal Name | Pin number | Description | Direction | Equivalent simplified schematics |
|---|---|---|---|---|
| **Power supplies** | | | | |
| VCCA5 | L7, L8, L9, L10, M8, M10, N8, N10 | 5.0V analog power supplies<br>Referenced to AGND | | |
| VCCA3 | J6, J11, K4, K5, K6, K11, K12, K13 | 3.3V analog power supply<br>Referenced to AGND | NA | |
| VCCD | A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11 | 3.3V digital power supply<br>Referenced to DGND | NA | |
| AGND | G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11 | Analog Ground | NA | |
| DGND | A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16 | Digital Ground | NA | |
| **Clock Signals** | | | | |
| CLK, CLKN | T6, R6 | Sampling clock signal input (In-phase and inverted phase) | I |  |



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**Table 6-1.** Pinout Table (Continued)

| Signal Name | Pin number | Description | Direction | Equivalent simplified schematics |
|---|---|---|---|---|
| DSP, DSPN | P3, N3 | Output clock (in-phase and inverted phase) | O |  |
| **Analog Output Signal** | | | | |
| OUT, OUTN | T9, T10 | In phase and inverted phase analog output signal (differential termination required) | O |  |
| **Digital Input Signals** | | | | |
| A0, A0N<br>A1, A1N<br>A2, A2N<br>A3, A3N<br>A4, A4N<br>A5, A5N<br>A6, A6N<br>A7, A7N<br>A8, A8N<br>A9, A9N<br>A10, A10N<br>A11, A11N | N1, N2<br>K3, J3<br>L3, M3<br>K1, K2<br>P1, P2<br>M1, M2<br>J1, J2<br>L1, L2<br>H1, H2<br>H3, G3<br>F1, F2<br>G1, G2 | In-phase, inverted phase Digital input<br>Port A<br>Data A0, A0N is the LSB<br>Data A11, A11N is the MSB | I |  |



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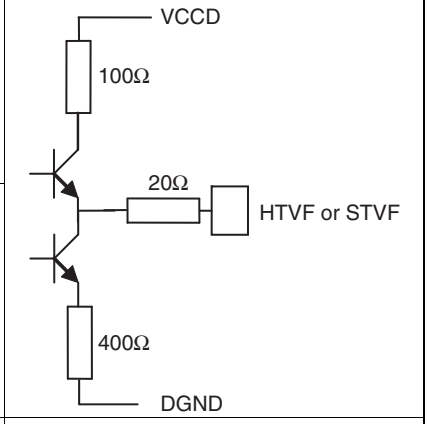
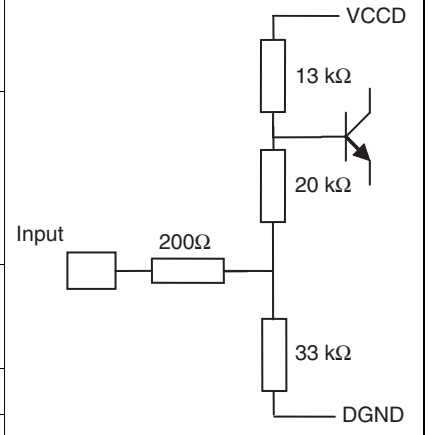
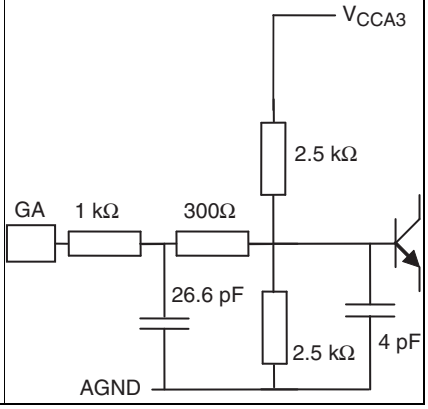
**Table 6-1.** Pinout Table (Continued)

| Signal Name | Pin number | Description | Direction | Equivalent simplified schematics |
|---|---|---|---|---|
| B0, B0N<br>B1, B1N<br>B2, B2N<br>B3, B3N<br>B4, B4N<br>B5, B5N<br>B6, B6N<br>B7, B7N<br>B8, B8N<br>B9, B9N<br>B10, B10N<br>B11, B11N | E3, F3<br>E1, E2<br>D1, D2<br>C1, C2<br>A3, B3<br>A4, B4<br>C7, C8<br>C6, C5<br>A5, B5<br>A7, B7<br>A6, B6<br>A8, B8 | In-phase, inverted phase Digital input<br>Port B<br>Data B0, B0N is the LSB<br>Data B11, B11N is the MSB | I | |
| C0, C0N<br>C1, C1N<br>C2, C2N<br>C3, C3N<br>C4, C4N<br>C5, C5N<br>C6, C6N<br>C7, C7N<br>C8, C8N<br>C9, C9N<br>C10, C10N<br>C11, C11N | E14, F14<br>E16, E15<br>D16, D15<br>C16, C15<br>A14, B14<br>A13, B13<br>C10, C9<br>C11, C12<br>A12, B12<br>A10, B10<br>A11, B11<br>A9, B9 | In-phase, inverted phase Digital input<br>Port D<br>Data D0, D0N is the LSB<br>Data D11, D11N is the MSB | I | |
| D0, D0N<br>D1, D1N<br>D2, D2N<br>D3, D3N<br>D4, D4N<br>D5, D5N<br>D6, D6N<br>D7, D7N<br>D8, D8N<br>D9, D9N<br>D10, D10N<br>D11, D11N | N16, N15<br>K14, J14<br>L14, M14<br>K16, K15<br>P16, P15<br>M16, M15<br>J16, J15<br>L16, L15<br>H16, H15<br>H14, G14<br>F16, F15<br>G16, G15 | In-phase, inverted phase Digital input<br>Port D<br>Data D0, D0N is the LSB<br>Data D11, D11N is the MSB | I | |
| IDC_P<br>IDC_N | R4<br>T4 | Input data check | I | |
| SYNC,<br>SYNCN | T5<br>R5 | In phase and Inverted phase reset signal | I | |



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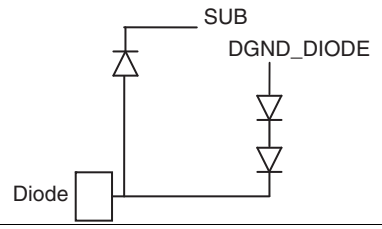
**Table 6-1.** Pinout Table (Continued)

| Signal Name | Pin number | Description | Direction | Equivalent simplified schematics |
|---|---|---|---|---|
| **Control Signals** | | | | |
| HTVF | N4 | Hold time violation flag | O |  |
| STVF | N6 | Setup time violation flag | O | |
| PSS0<br>PSS1<br>PSS2 | T13<br>R13<br>R14 | Phase Shift Select (PSS2 is the MSB) | I |  |
| MODE0<br>MODE1 | T12<br>R12 | DAC Mode selection bits:<br>- RTZ<br>- NRZ<br>- Narrow RTZ<br>- RF | I | |
| OCDS0<br>OCDS1 | N14<br>P14 | Output Clock Division Select = these bits allow to select the clock division factor applied on the DSP, DSPN signal. | I | |
| MUX | T14 | MUX selection: | I | |
| IUCM | M12 | Input underclocking mode enable | I | |
| GA | P4 | Gain adjust | I |  |



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**Table 6-1.** Pinout Table (Continued)

| Signal Name | Pin number | Description | Direction | Equivalent simplified schematics |
|---|---|---|---|---|
| Diode | M6 | Diode for die junction temperature monitoring function | I |   |
| NC | M11 | Reserved pin, NC, can be connected to DGND | | |

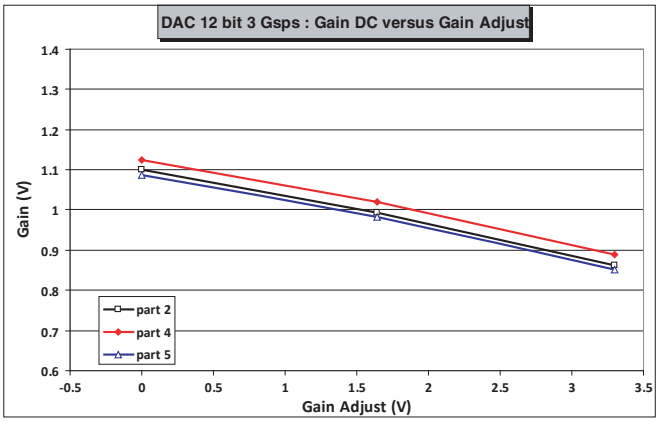
# 7. CHARACTERIZATION RESULTS

Unless otherwise specified results are given at room temperature (Tj ~ 60°C), nominal power supply, in 4:1 MUX mode, gain at nominal setting.

## 7.1 Static Performances

### 7.1.1 DC Gain Characterization

**Figure 7-1.** DAC DC Gain vs Gain Adjust (Measured in NRZ Mode)






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**Figure 7-2.** DAC DC Gain Drift from Unity Gain vs Temperature (Measured in NRZ Mode)

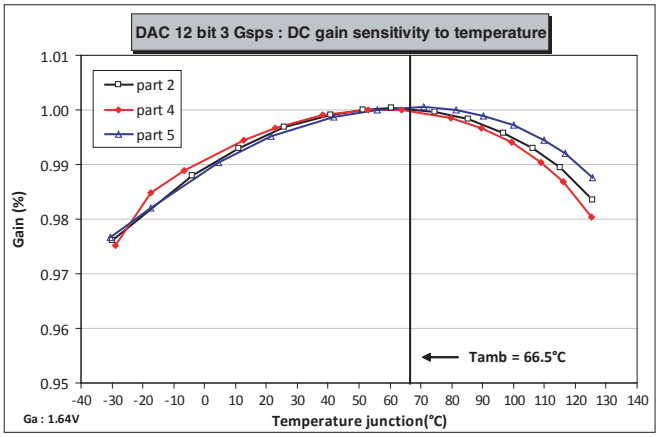
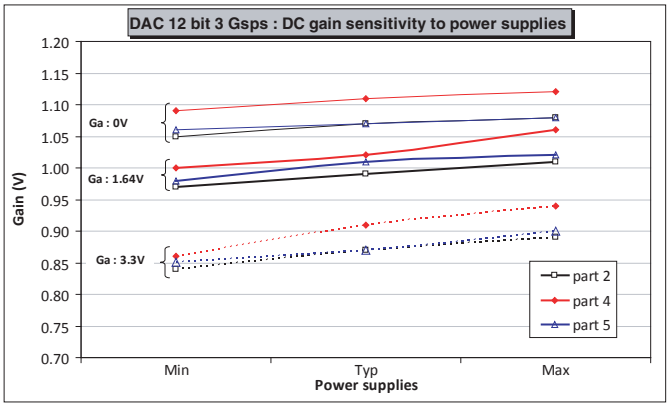



**Figure 7-3.** DC Gain Sensitivity to Power Supply (Measured in NRZ Output Mode)



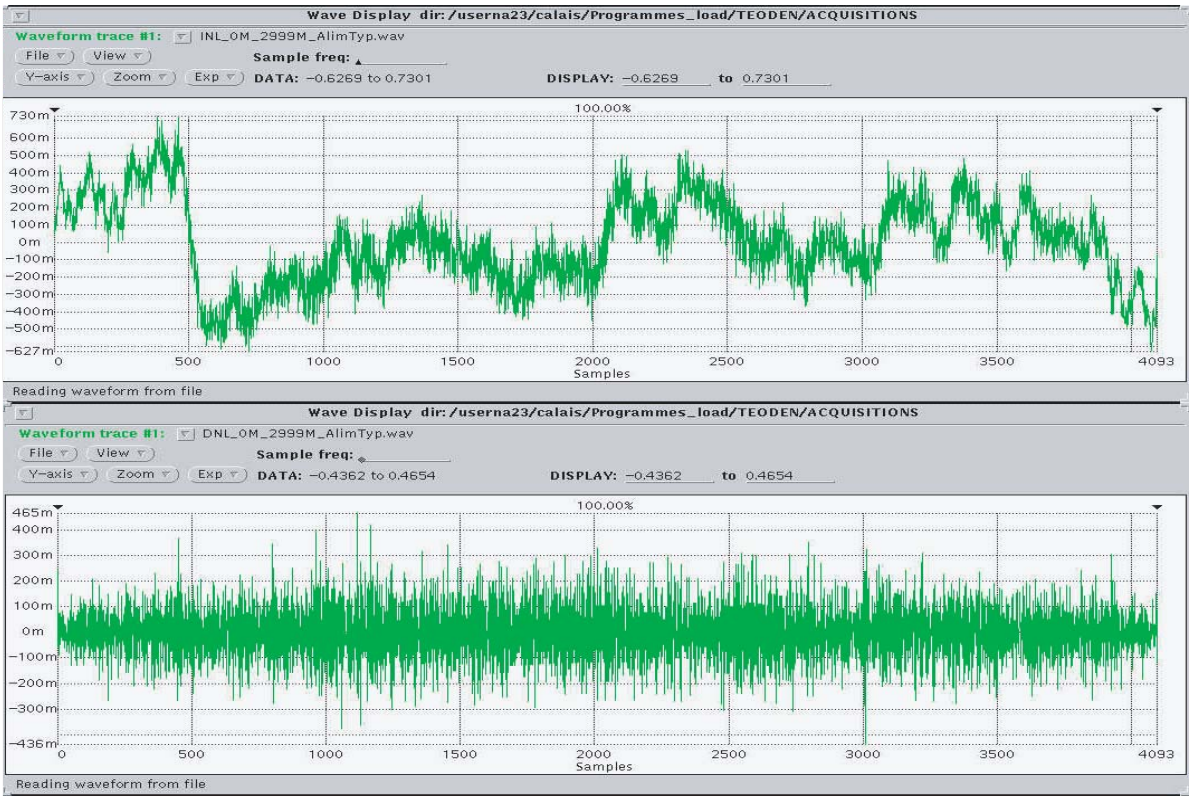

Conditions: room temperature, supply levels:
- Min: $V_{CCA}$: 4.75V // $V_{CCA3}$ = $V_{CCD}$ = 3.15V
- Typ: $V_{CCA}$: 5V // $V_{CCA3}$ = $V_{CCD}$ = 3.3V
- Max: $V_{CCA}$: 5.25V // $V_{CCA3}$ = $V_{CCD}$ = 3.45V



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### 7.1.2 Static Linearity

**Figure 7-4.** INL/DNL Measurement at Fout = 100 kHz and 3 Gsps




INL reflects a true 12 bit DAC.

Low DNL values reflect a strictly monotonous 12 bit DAC.



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## 7.2 AC Performances

### 7.2.1 Available Output Power vs Fout.

The following plots summarize characterization results, for a Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

**Figure 7-5.** Available Pout vs Fout from 98 MHz to 4498 MHz in the 4 Output Modes at 3 Gsps

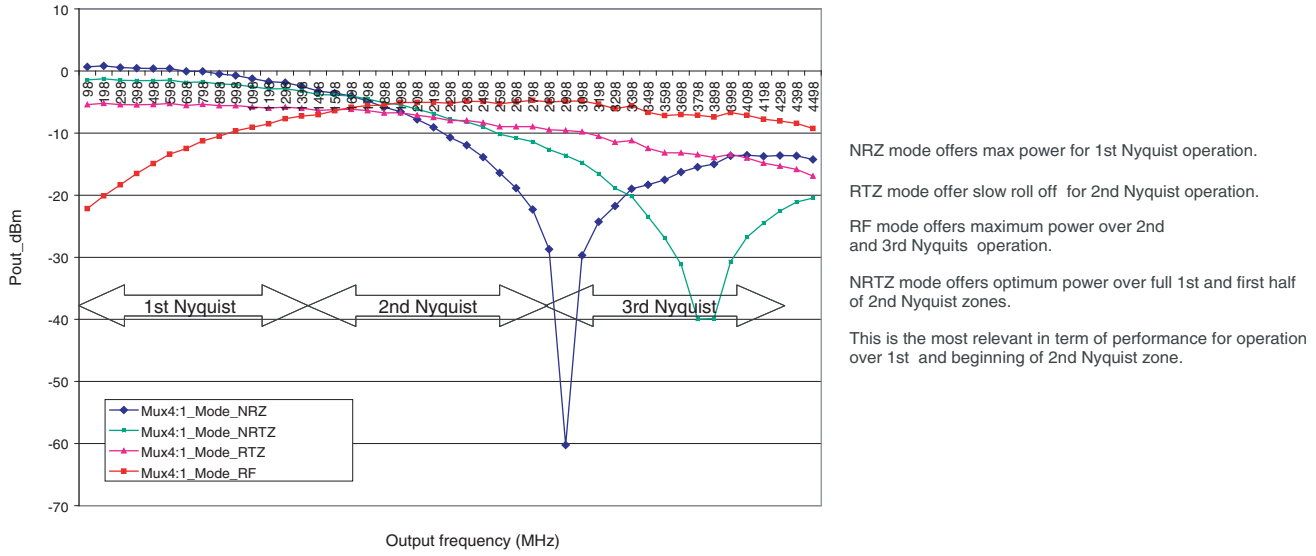
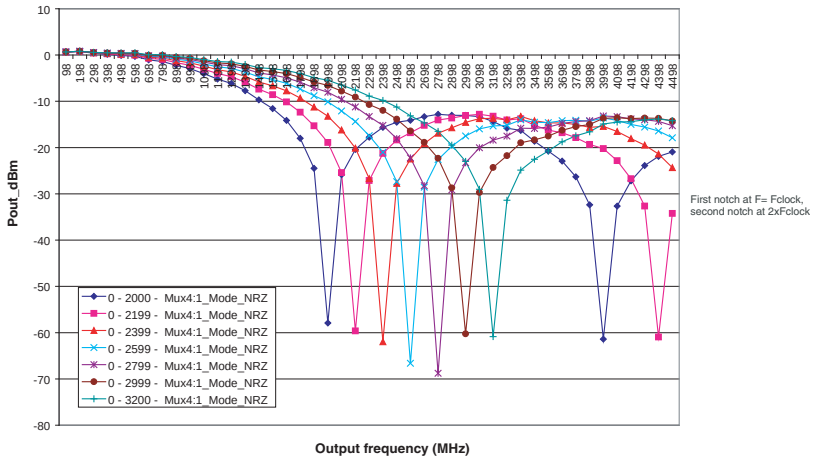


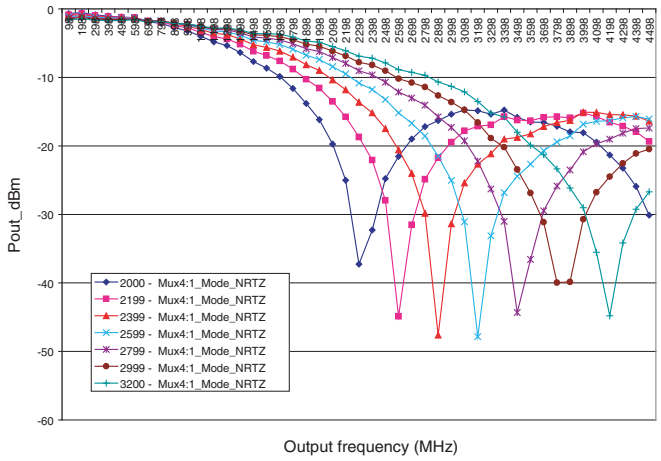

**Figure 7-6.** Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 Gsps to 3.2 Gsps in NRZ Mode





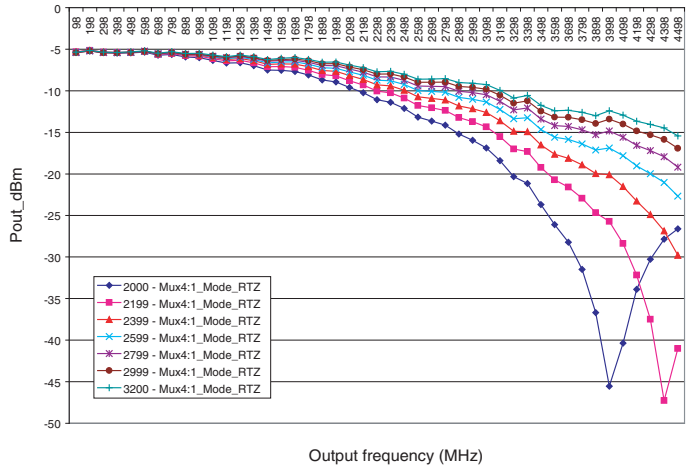

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**Figure 7-7.** Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 Gsps to 3.2 Gsps in NRTZ Mode



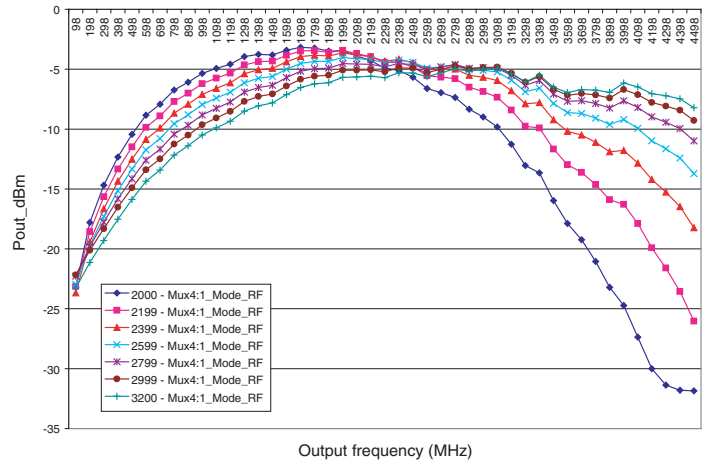

First notch at F=1/((1/Fclock) - 75ps), second notch at 2xF

**Figure 7-8.** Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 Gsps to 3.2 Gsps in RTZ Mode




First notch at F = 2 x Fclock

**Figure 7-9.** Available Pout vs Fout from 98 MHz to 4498 MHz and from 2 Gsps to 3.2 Gsps in RF Mode




First notch at DC



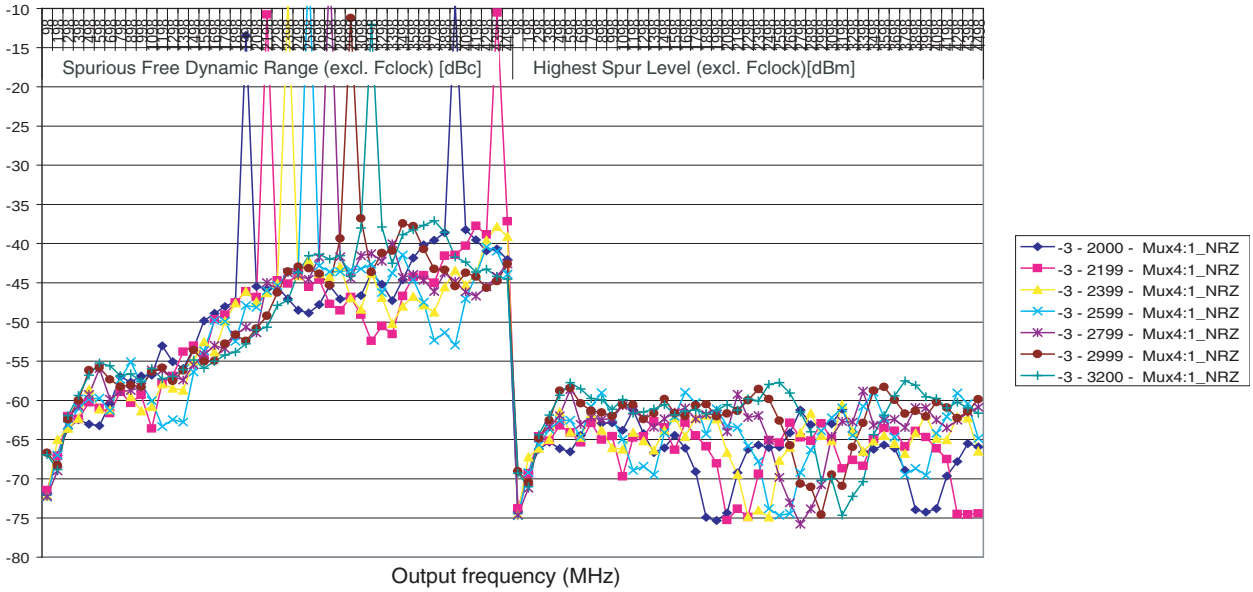
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### 7.2.2 Single Tone Measurements

The following plots summarize characterization results in MUX4:1 mode, for an Fout sweep from 98 MHz to 4498 MHz (step 100 MHz).

The left side of the plot gives SFDR expressed in dBc and the right side gives HSL (Highest Spur Level excluding Fclock spur) expressed in dBm.

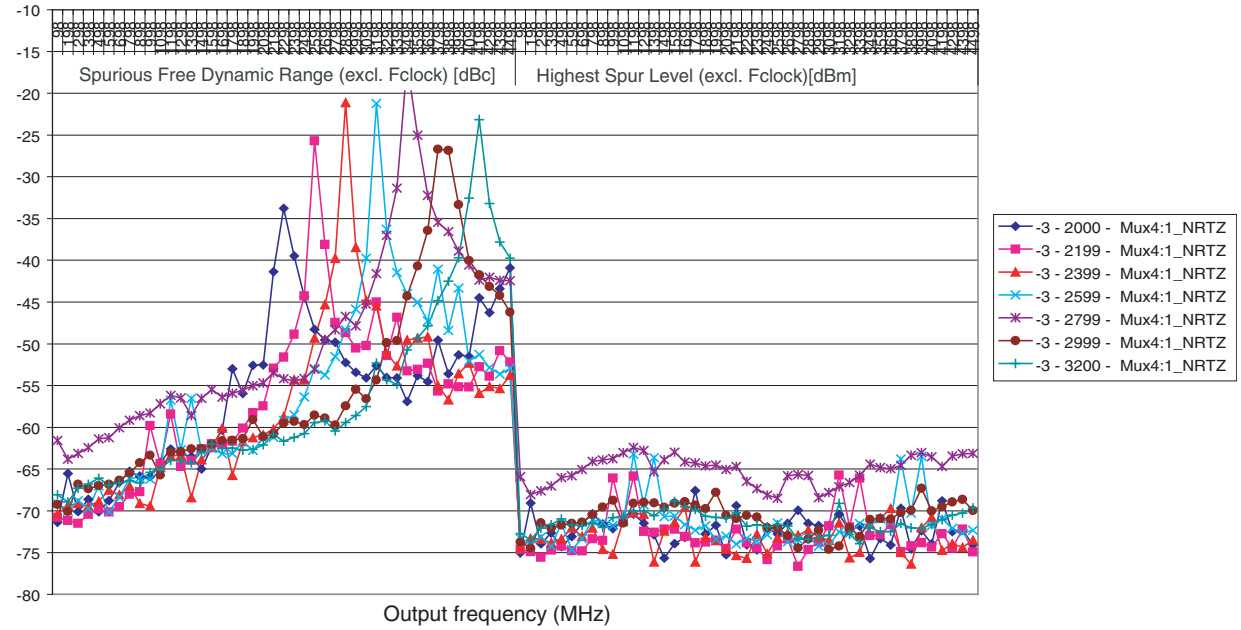
**Figure 7-10.** SFDR and HSL in NRZ mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps




NRZ mode is only relevant for Fout below 400 MHz.

The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

**Figure 7-11.** SFDR and HSL in NRTZ mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps

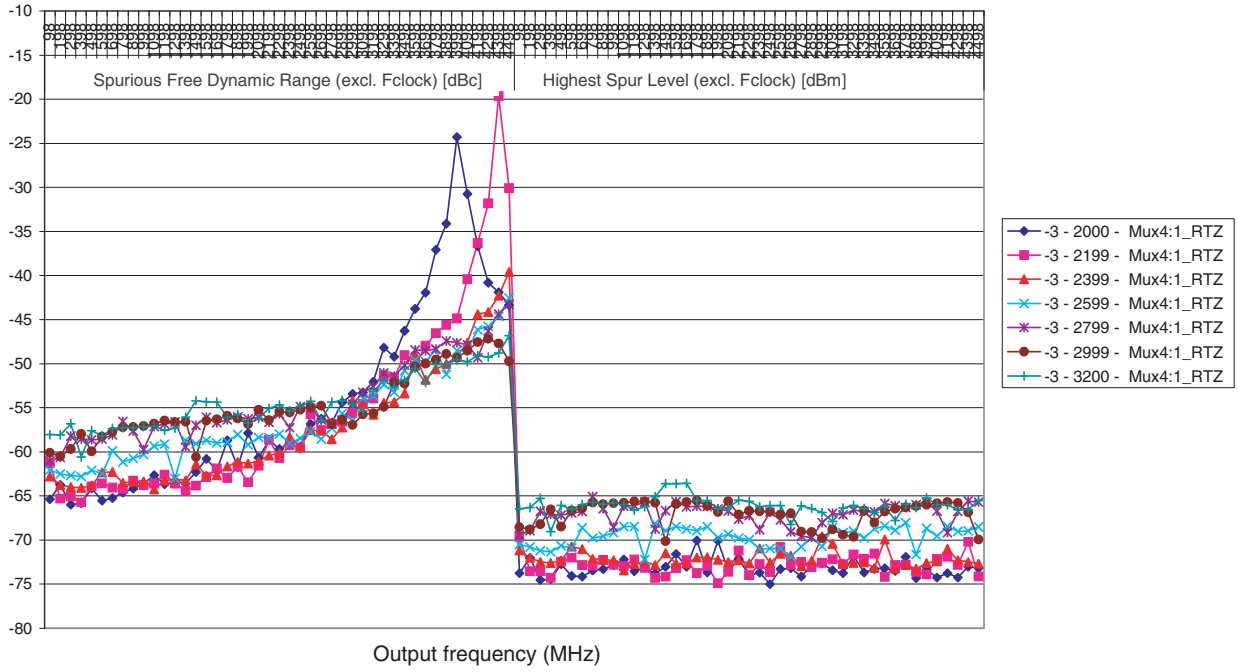





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NRTZ mode brings significant improvement regarding NRZ mode. This mode concentrates the benefits of both NRZ mode (high power available) and RTZ mode (extended available dynamic range).
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

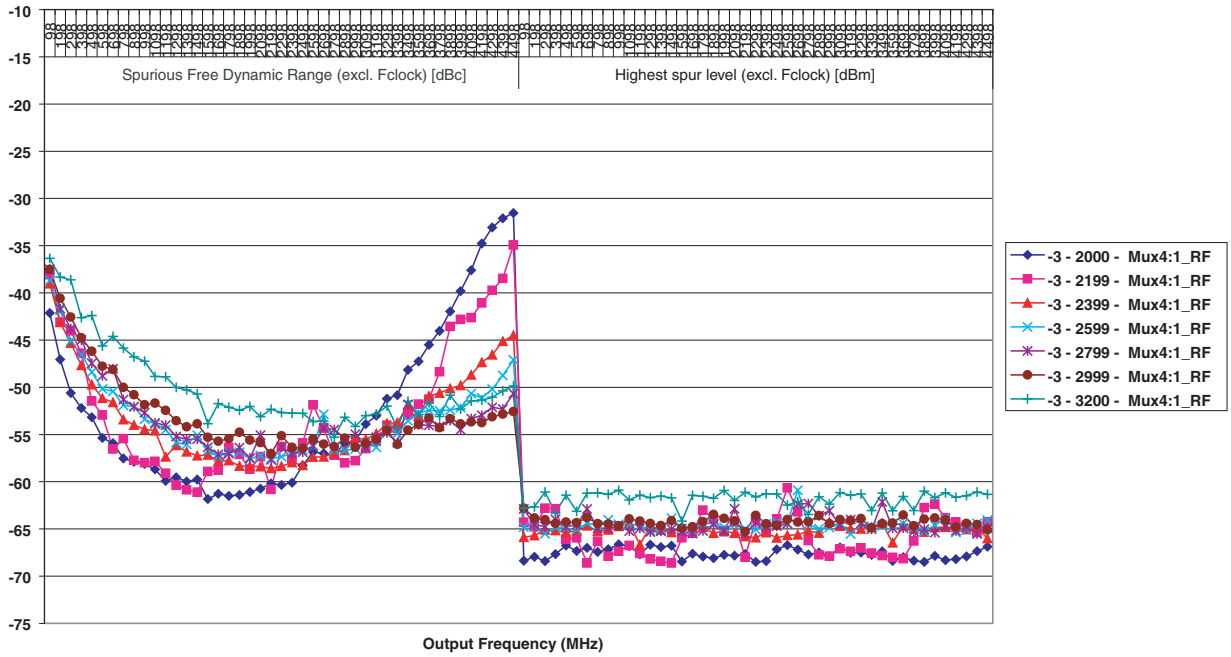
**Figure 7-12.** SFDR and HSL in RTZ Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps




RTZ mode allows for operation over the 3 first Nyquist zones.
In first and beginning of second Nyquist zone NRTZ mode is mode relevant. The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null.

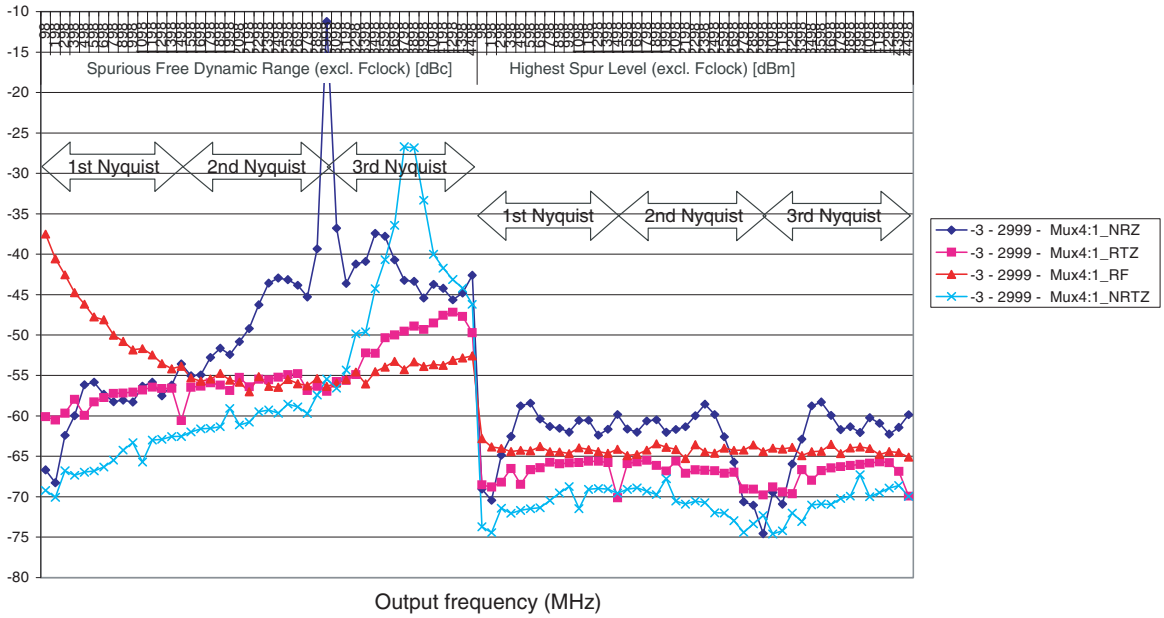

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**Figure 7-13.** SFDR and HSL in RF Mode at –3 dBFS for Sampling Rate from 2000 MSps to 3200 MSps




RF mode allows for operation over 3rd Nyquist zones. Performances are not sensitive to output level. Performance roll off occurs beyond 3000 MSps.

**Figure 7-14.** Comparison of the 4 Output Modes at 2999 MSps and at –3 dBFS: SFDR and HSL

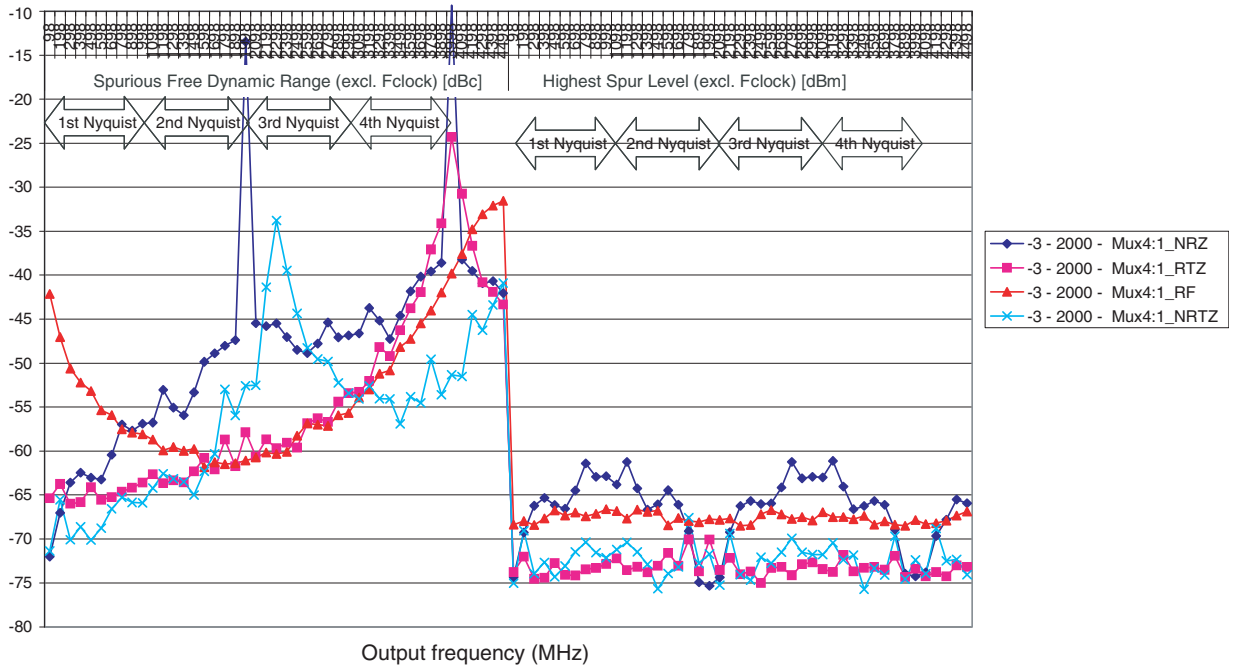



NRZ is interesting only at the very beginning of the first Nyquist zone.
NRTZ is relevant over 1st 2nd and 4th Nyquist zones.
RTZ is relevant over 2nd and 3rd Nyquist zones.
RF mode displays a good behavior over 2nd and 3rd Nyquist Zones.
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null



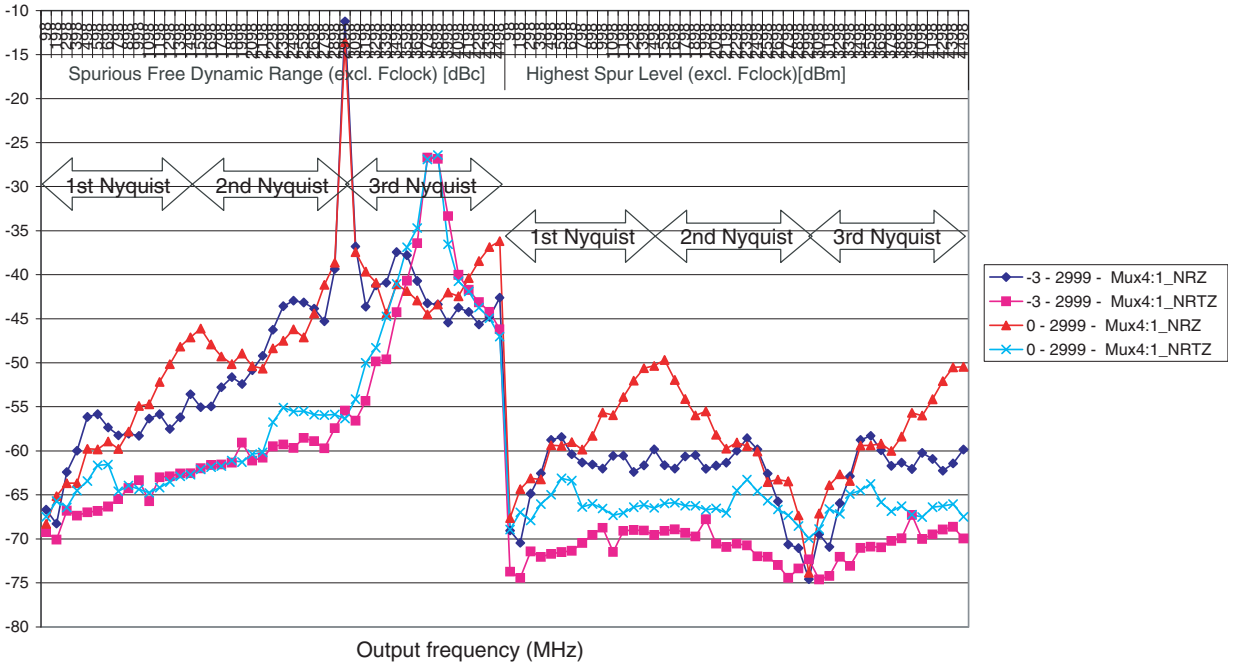
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**Figure 7-15.** Comparison of the 4 Output Modes at 2000 MSps and –3 dBFS: SFDR and HSL




NRTZ is the most relevant over 1st Nyquist zone, 1st half of 2nd Nyquits zone and 4th Nyquist zone.
RF mode is the best choice for 2nd half of 2nd Nyquist Zone and 3rd Nyquist zone.
RTZ gives relevant performances over the three first Nyquist zones.
The spikes in the SFDR are caused by normalization artefacts due to the Sinc(x) null

**Figure 7-16.** Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL (Excluding Fclock)

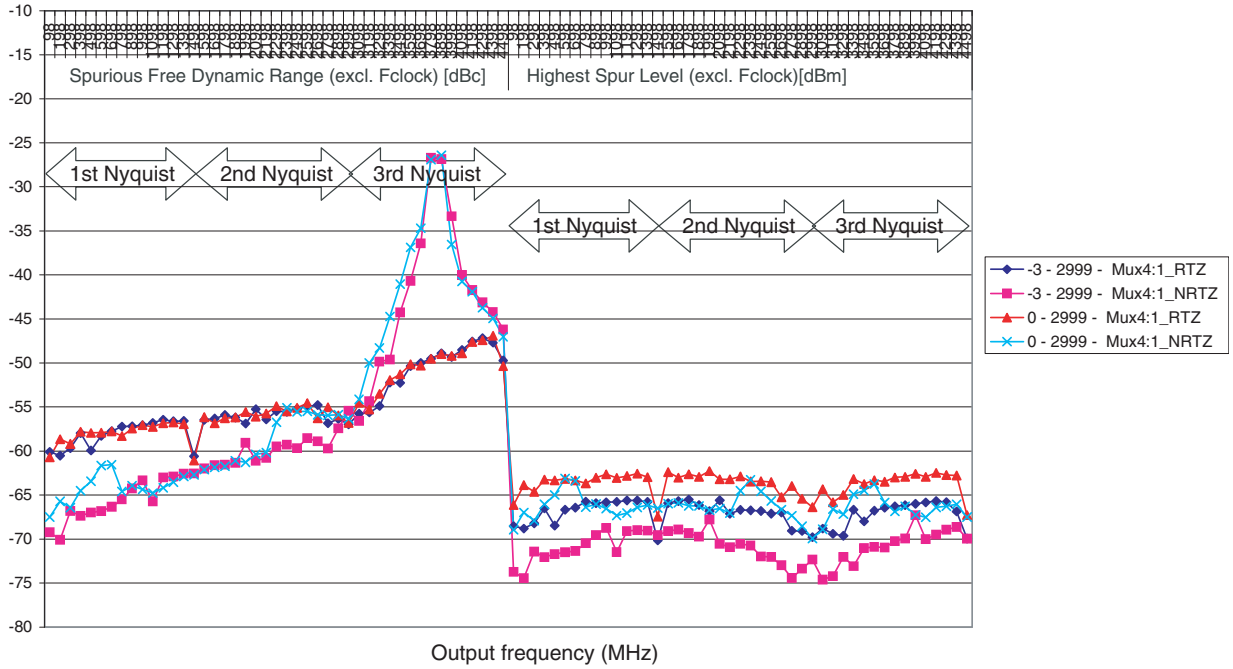




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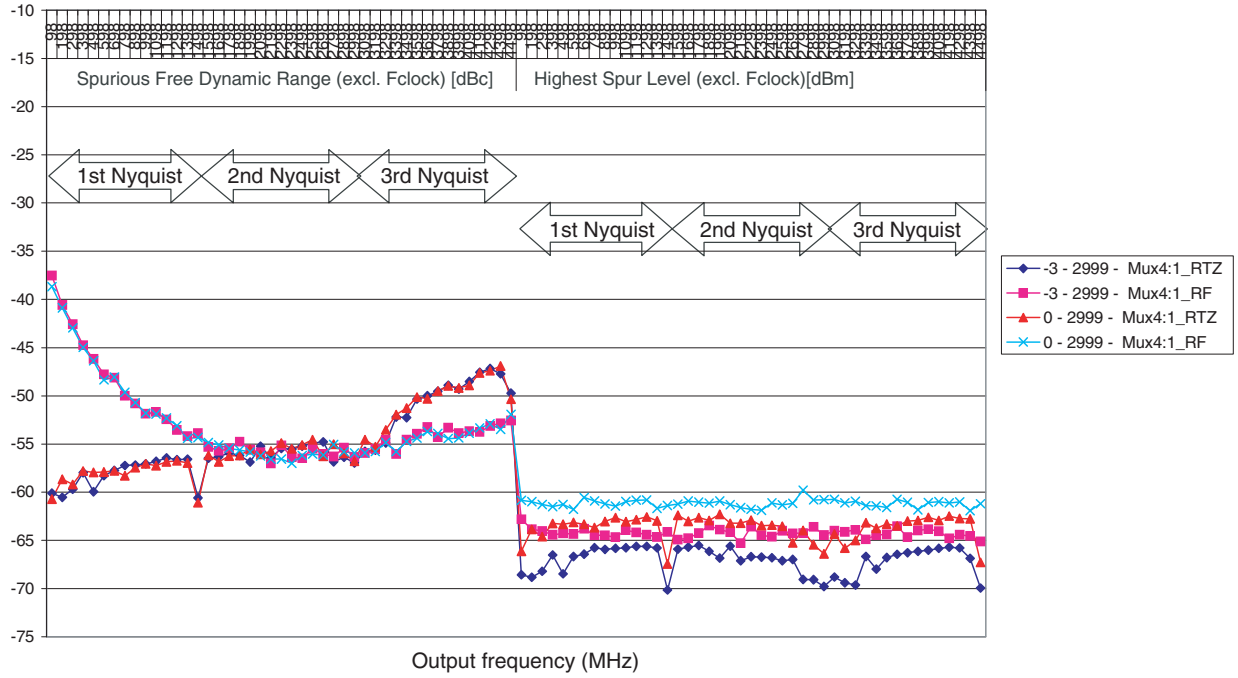
NRTZ gives better performances over 1st and 2nd Nyquist zone, and is much less sensitive to output level.

**Figure 7-17.** Comparison of NRTZ and RTZ Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL




NRTZ is more relevant for 1st Nyquist zone and 1st half of 2nd Nyquist zone. Beyond middle of second Nyquist zone RTZ mode is more relevant.

**Figure 7-18.** Comparison of RTZ and RF Modes at Full Scale and –3 dBFS at 2999 MSps: SFDR and HSL

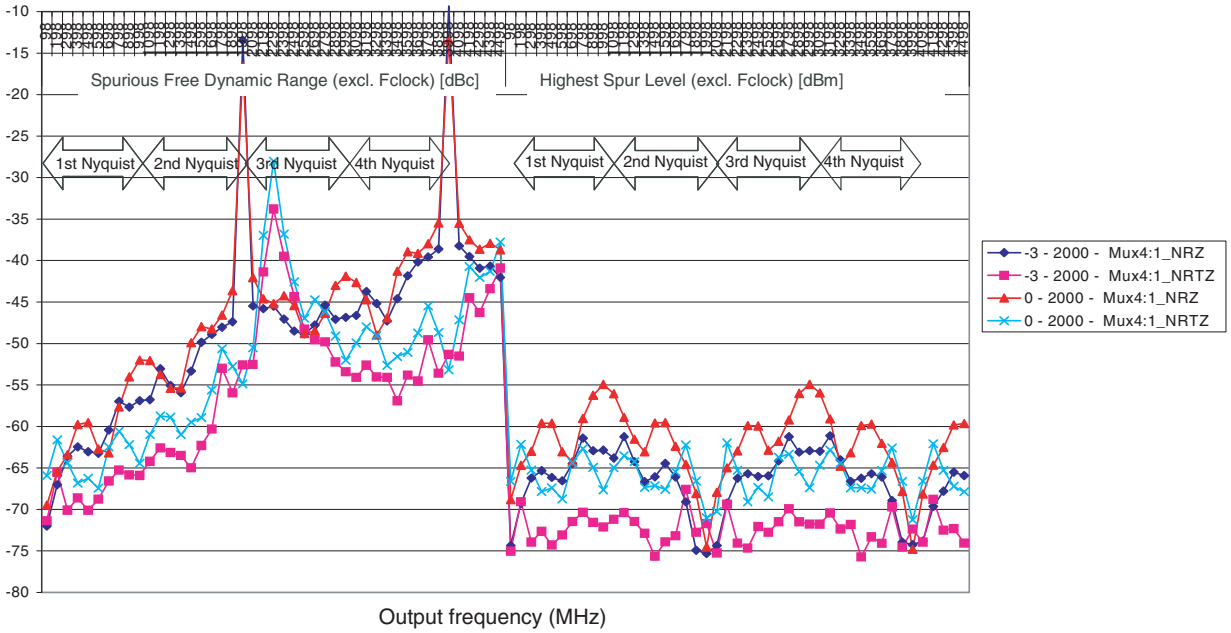



RF mode gives better performance over 3rd Nyquist zone.



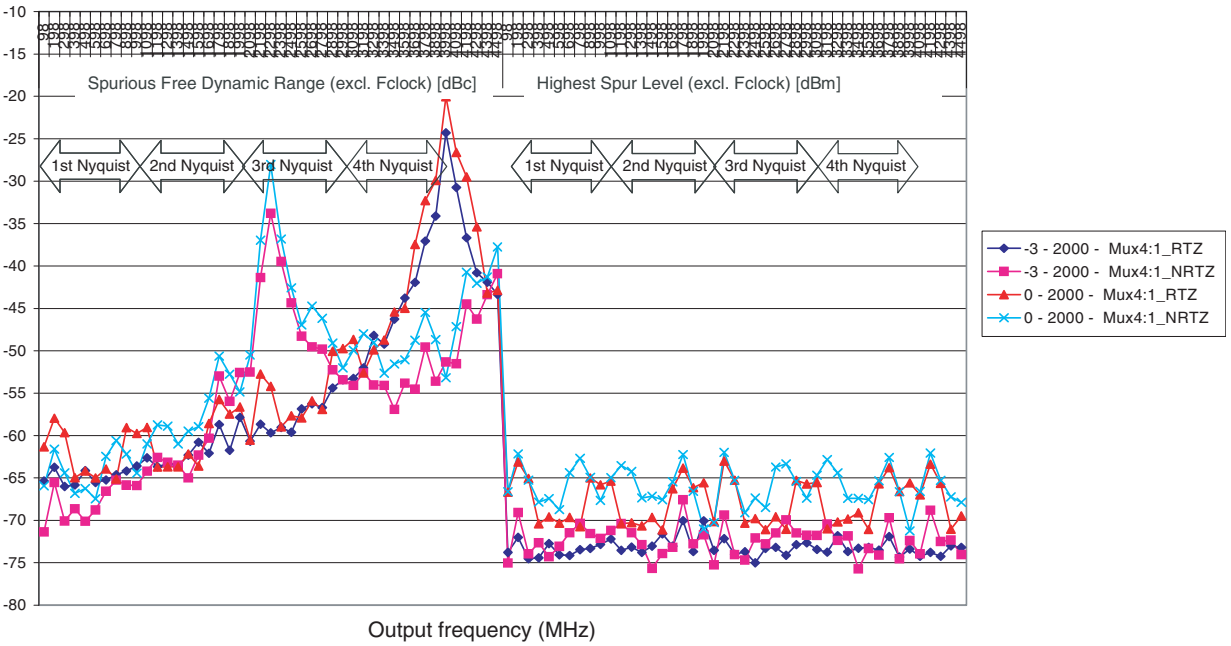
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**Figure 7-19.** Comparison of NRZ and NRTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)




NRTZ linearity is slightly improved reducing the sampling rate to 2000 MSps, possibility of operation over the 4th Nyquist zone is demonstrated.

**Figure 7-20.** Comparison of NTRZ and RTZ Modes at Full Scale and –3 dBFS at 2000 MSps: SFDR and HSL (Excluding Fclock)




NRTZ mode is relevant in 1st, 2nd Nyquist zones and is still usable over 4th Nyquist zone with SFDR in excess of 50 dBc.



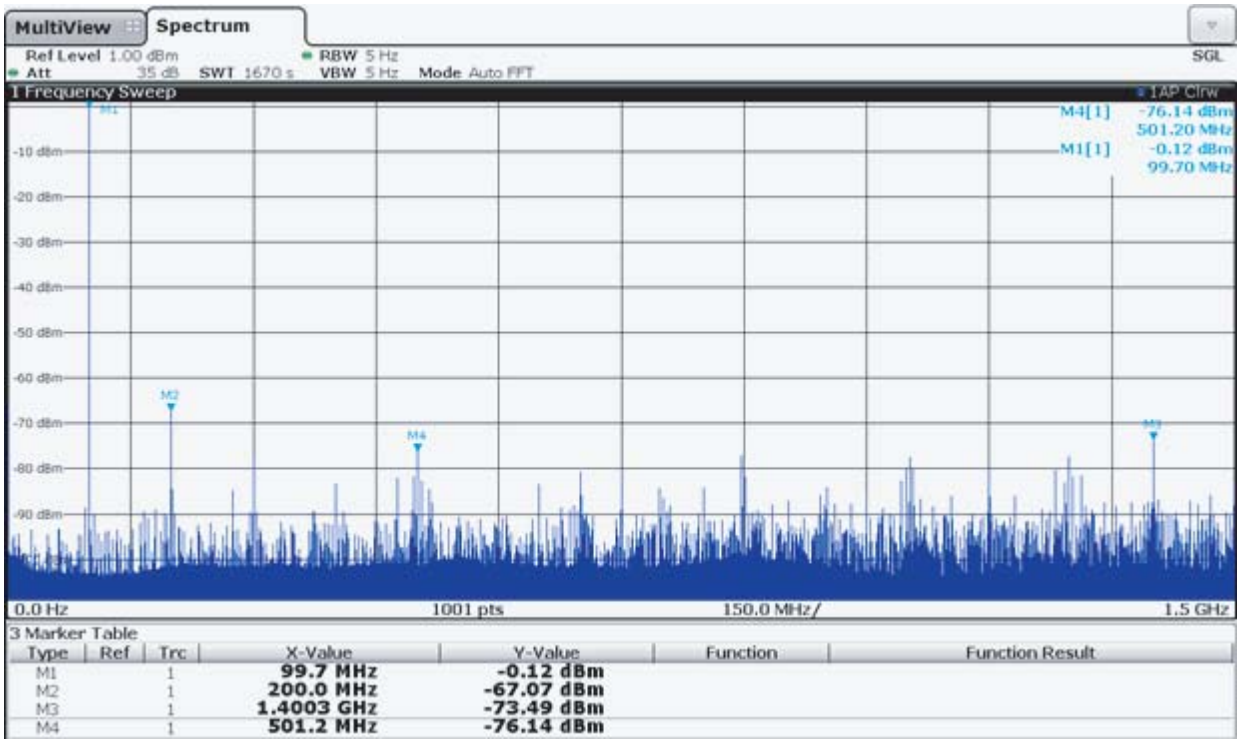
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### 7.2.3 Single tone measurements: typical spectra at 3Gsps

The following figures show typical SFDR spectra obtained for the four DAC modes on an EV12DS130A/B device.

Conditions: typical power supplies, ambient temperature, MUX4:1, Fs = 3 Gsps.

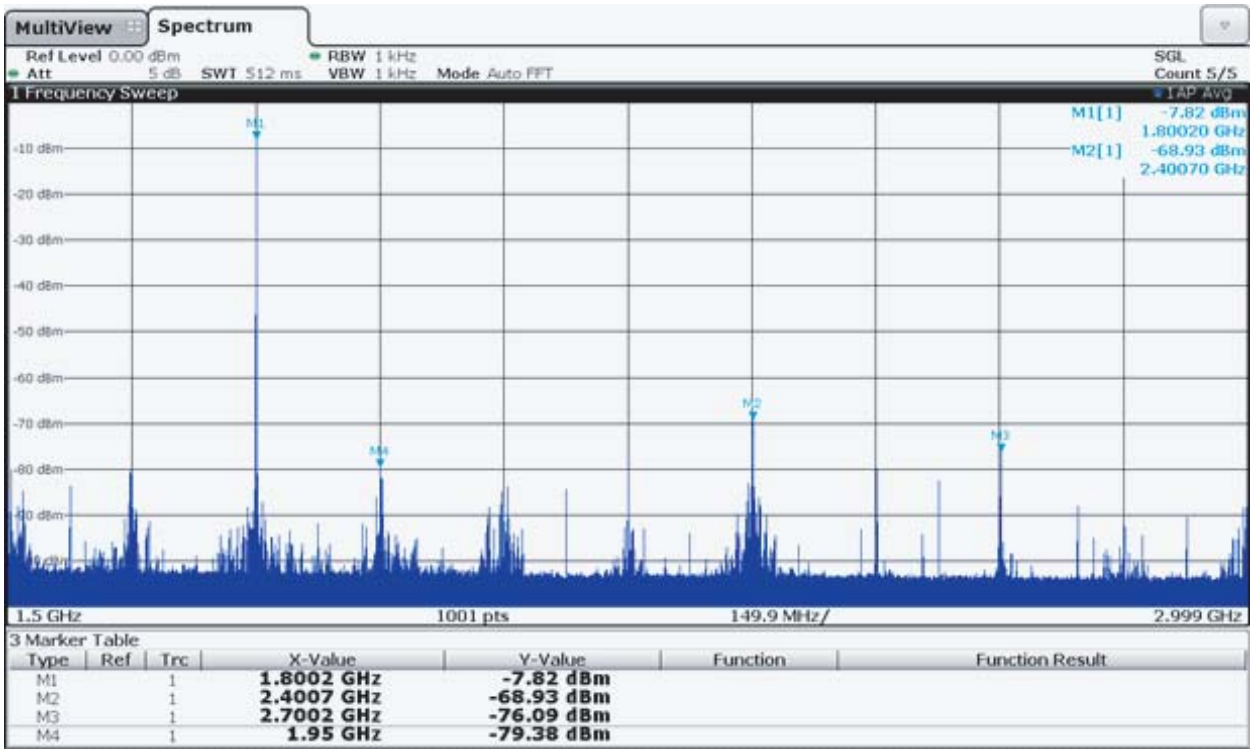
**Figure 7-21.** Typical SFDR spectrum in NRZ mode. Fout = 100MHz (1st Nyquist), MUX4:1, Fs = 3Gsps. SFDR = 67dBc






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**Figure 7-22.** Typical SFDR spectrum in NRTZ mode. Fout = 1800MHz (2nd Nyquist), MUX4:1, Fs = 3Gsps. SFDR = 61dBc






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**Figure 7-23.** Typical SFDR spectrum in RTZ mode. Fout = 2900MHz (2nd Nyquist), MUX4:1, Fs = 3Gsps. SFDR = 59dBc.

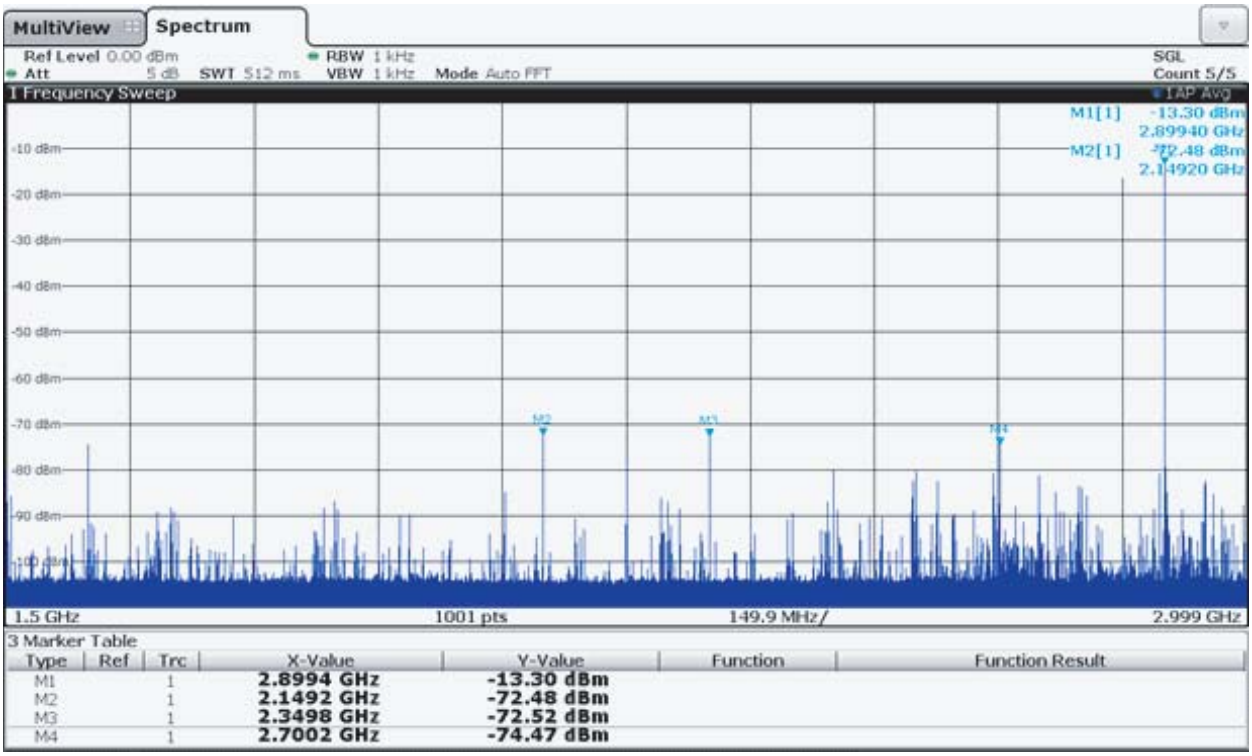
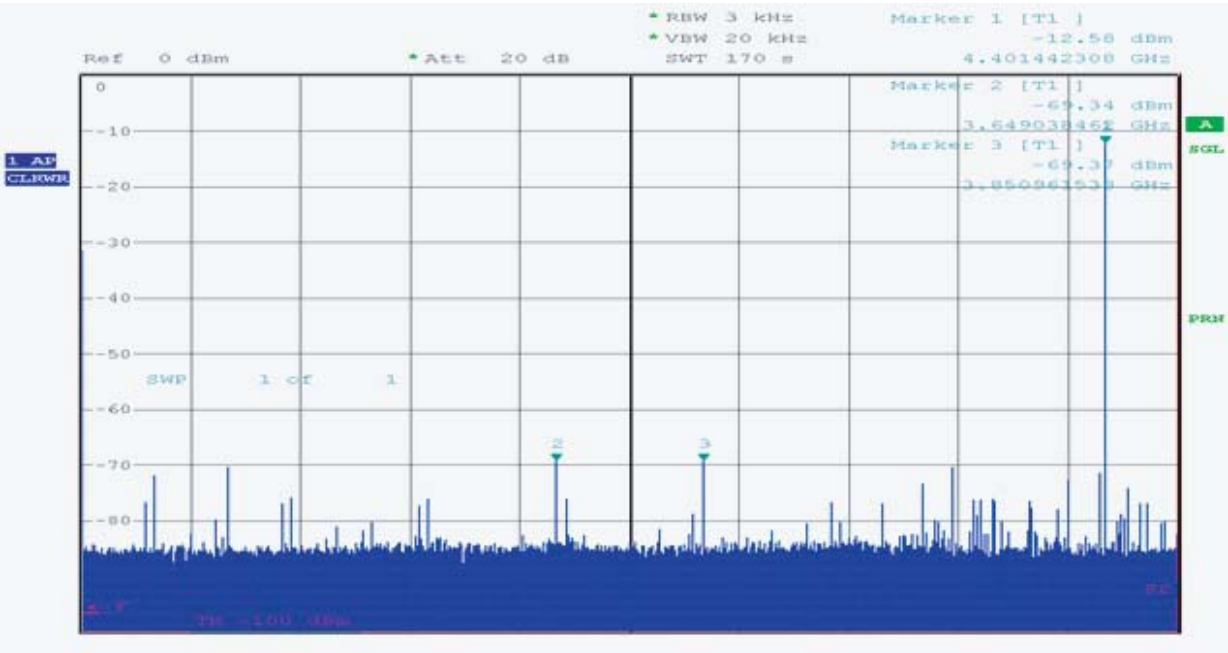



**Figure 7-24.** Typical SFDR spectrum in RF mode. Fout = 4400MHz (3rd Nyquist), MUX4:1, Fs = 3Gsps. SFDR = 56 dBc






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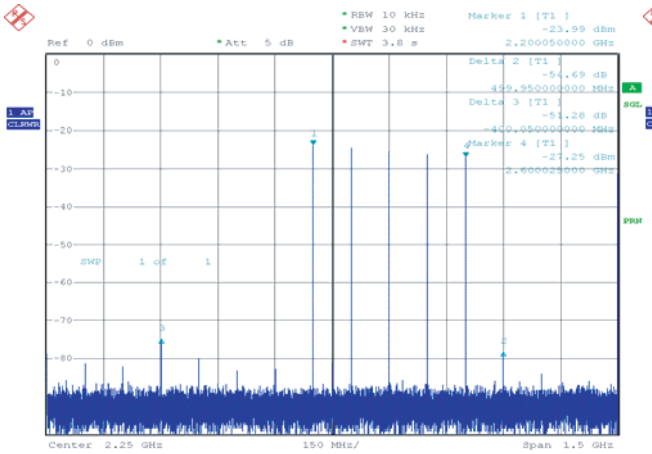
### 7.2.4 Multi Tone Measurements

A five tones pattern (400 MHz, 500 MHz, 600 MHz, 700 MHz and 800 MHz) is applied to the DAC operating at 3 Gsps and results are observed in the 2nd, 3rd, 4th and 5th Nyquist zones.

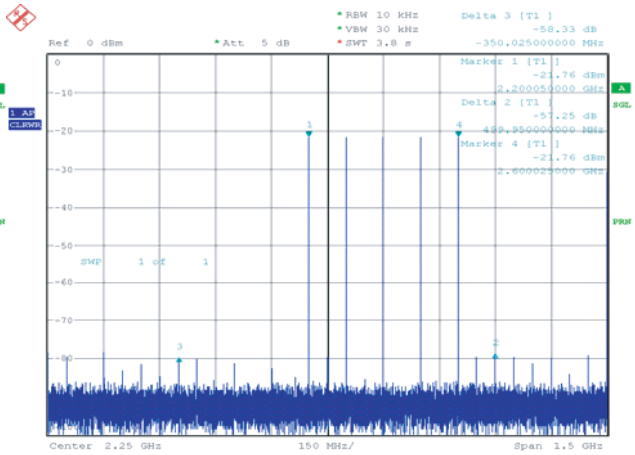
Results are given in the most relevant mode considering the Nyquist zone observed.

**Figure 7-25.** Observation of the 2nd Nyquist Zone (Tones are pushed from 2.2 GHz to 2.6 GHz): NRTZ, RF and RTZ Modes

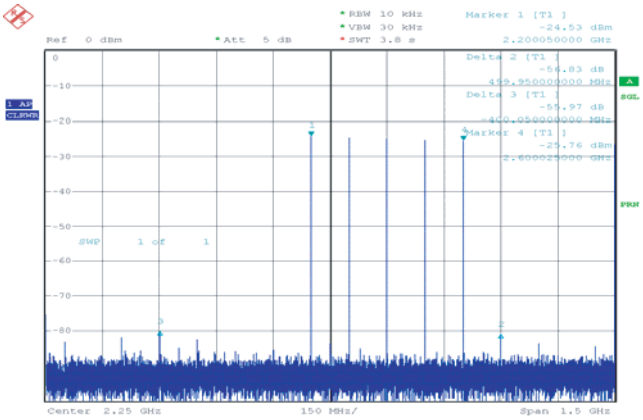
NRTZ mode:



RF mode:



RTZ mode:



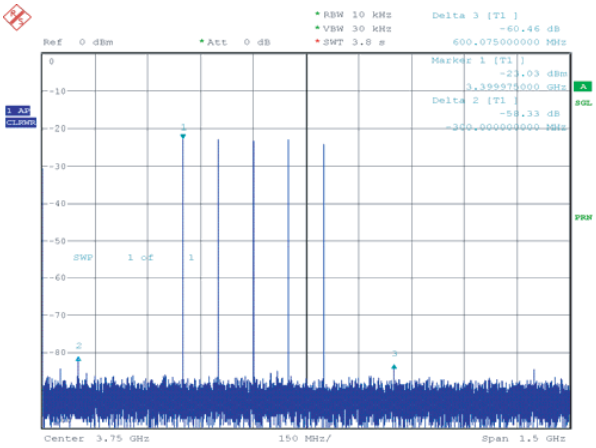
| | Fout (MHz) | Pout (dBm) | SFDR (freq) | SFDR (dBc) |
|---|---|---|---|---|
| N RTZ | 2200 | -23,99 | 1800 | -51,28 |
| RTZ | 2200 | -24,53 | 1800 | -55,97 |
| RF | 2200 | -21,76 | 2700 | -57,25 |



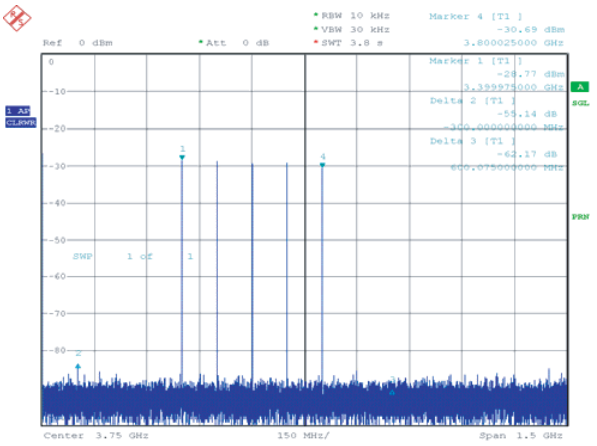
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**Figure 7-26.** Observation of the 3rd Nyquist Zone (Tones are pushed from 3.4GHz to 3.8GHz): RF and RTZ Modes

RF mode:



RTZ mode:

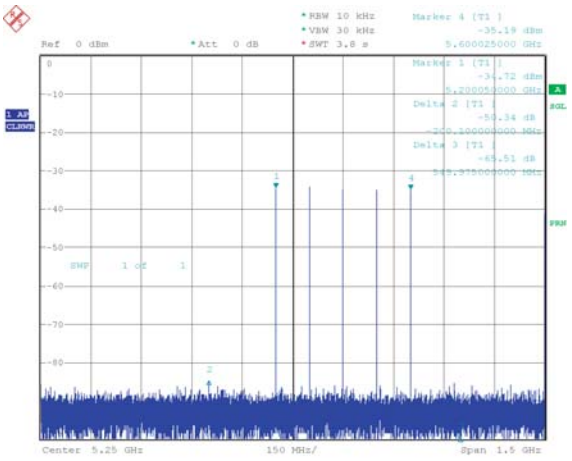


| | Fout (MHz) | Pout (dBm) | SFDR (freq) | SFDR (dBc) |
|---|---|---|---|---|
| NRTZ | 3400 | –39.43 | 4000 | –44.48 |
| RTZ | 3400 | –28.77 | 3100 | –55.14 |
| RF | 3400 | –23.03 | 3100 | –58.33 |

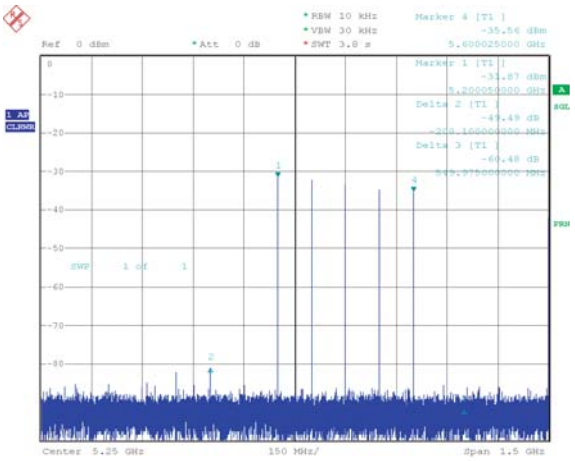
NRTZ performances are degraded because of the sinc attenuation (first notch in the first half of the 3rd Nyquist zone).

**Figure 7-27.** Observation of the 4th Nyquist Zone (Tones are pushed from 5.2 GHz to 5.6 GHz): NRTZ and RF Modes

NRTZ mode



RF mode





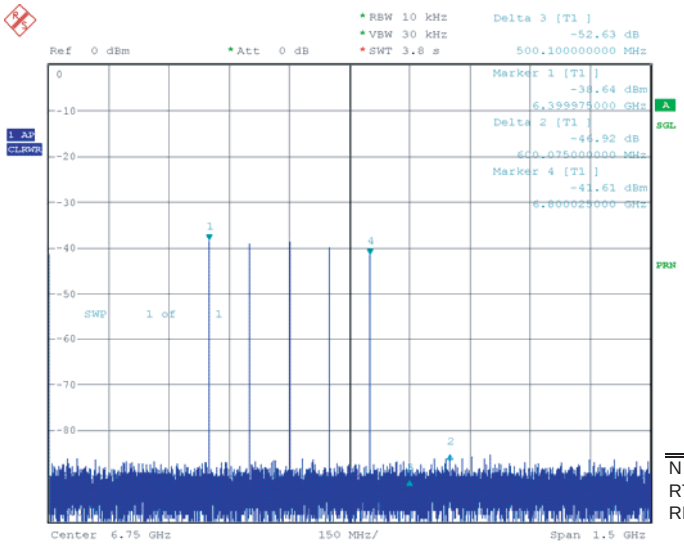
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| | Fout (MHz) | Pout (dBm) | SFDR (freq) | SFDR (dBc) |
|---|---|---|---|---|
| NRTZ | 5200 | –34.72 | 5000 | –50.34 |
| RTZ | 5200 | –40.37 | 4700 | –45 |
| RF | 5200 | –31.87 | 4700 | –49.49 |

RTZ mode is degraded because of the sinc attenuation (first notch at the end of the 4th Nyquist zone). RF mode offers significantly more power than RTZ mode, this is why we still have acceptable performances.

NRTZ operation is possible because the 4th Nyquist zone is fully included in the secondary spectral lobe.

**Figure 7-28.** Observation of the 5th Nyquist Zone (Tones are pushed from 6.4 GHz to 6.8 GHz): NRTZ Mode




| | Fout (MHz) | Pout (dBm) | SFDR (freq) | SFDR (dBc) |
|---|---|---|---|---|
| N RTZ | 6400 | -38,64 | 7000 | -46,92 |
| RTZ | 6800 | -46,69 | 7000 | -39,25 |
| RF | 6400 | -46,89 | 7000 | -38,01 |

NRTZ mode is still usable in the 5th Nyquist zone (SFDR in excess of 46 dB).



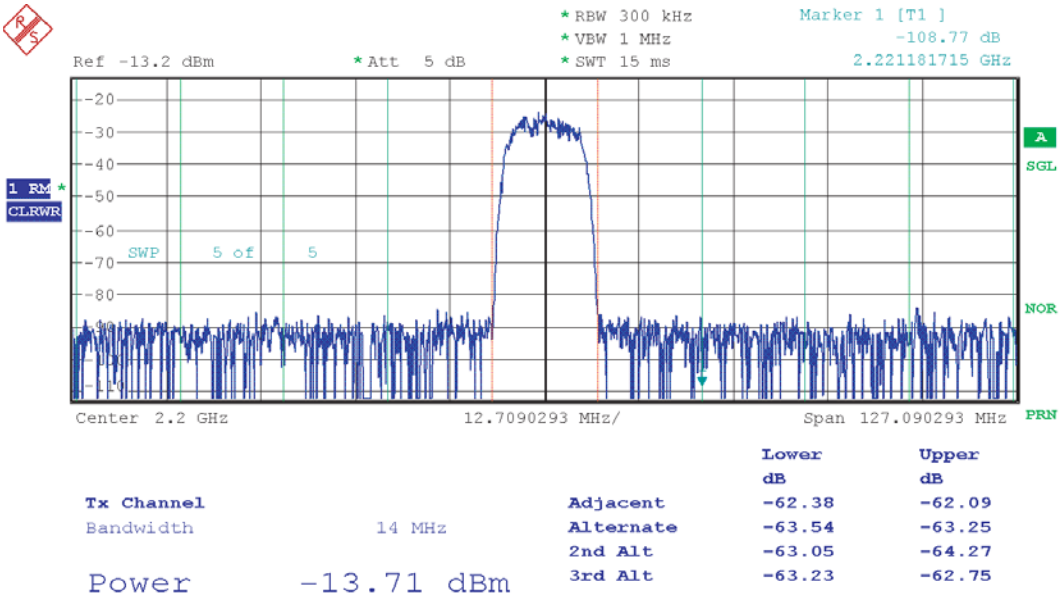
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### 7.2.5 Direct Microwave Synthesis Capability Measurements: ACPR

Measurements given hereafter are performed on the DAC at 3 Gsps with a 10 MHz wide QPSK pattern centered on 800 MHz.

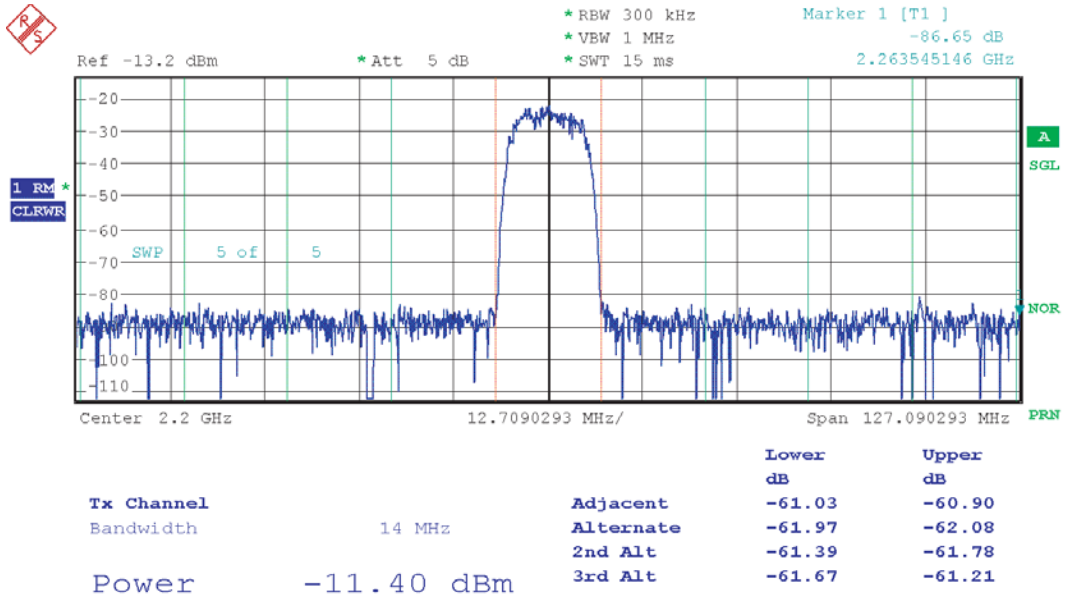
Results are observed in 2nd, 3rd, 4th and 5th Nyquist zones and are given only for the most relevant modes (that is RF and/or NRTZ modes).

**Figure 7-29.** NRTZ Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz




ACPR is in excess of 62 dB. DMWS capability is proven for second Nyquist in NRTZ mode.

**Figure 7-30.** RF Mode, 2nd Nyquist: Center Frequency is pushed to 3 GHz – 800 MHz = 2.2 GHz

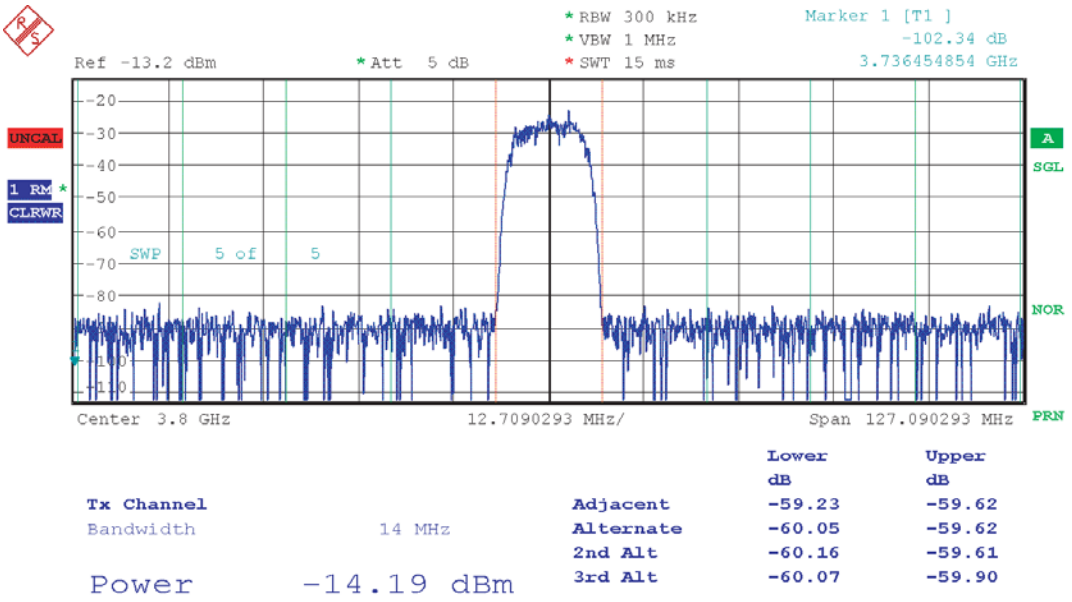





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ACPR is in excess of 60 dB. DMWS capability is proven for the second Nyquist zone in RF mode with slightly reduced dynamic range regarding NRTZ mode but with increased output power.

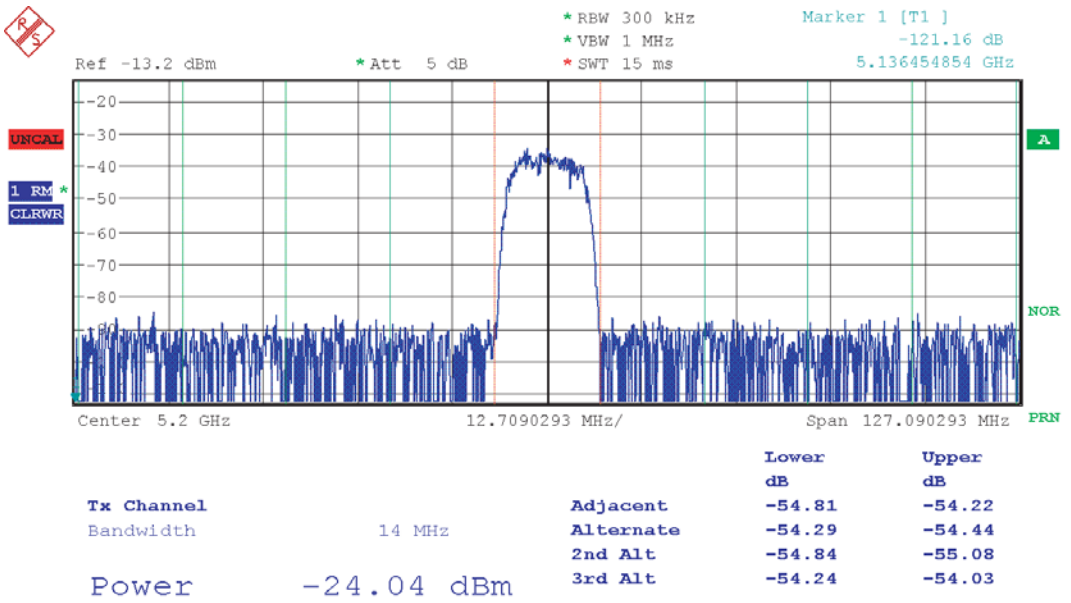
**Figure 7-31.** RF Mode, 3rd Nyquist Zone: Center Frequency is pushed to 3 GHz+ 800 MHz = 3.8 GHz




ACPR is in excess of 59 dB. DMWS capability is proven for the third Nyquist zone in RF mode.

Note: due to the notch of available Pout near the middle of the third Nyquist zone, the NRTZ mode is not relevant for DMWS in the third Nyquist zone.

**Figure 7-32.** NRTZ Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz

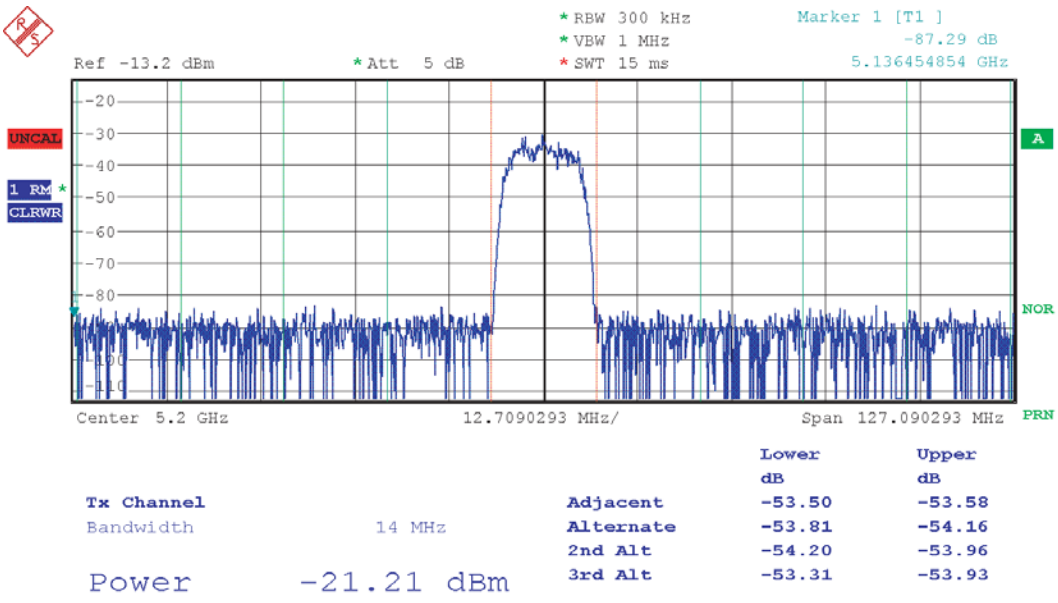



ACPR is in excess of 54 dB. DMWS capability is proven for the fourth Nyquist zone in NRTZ mode.



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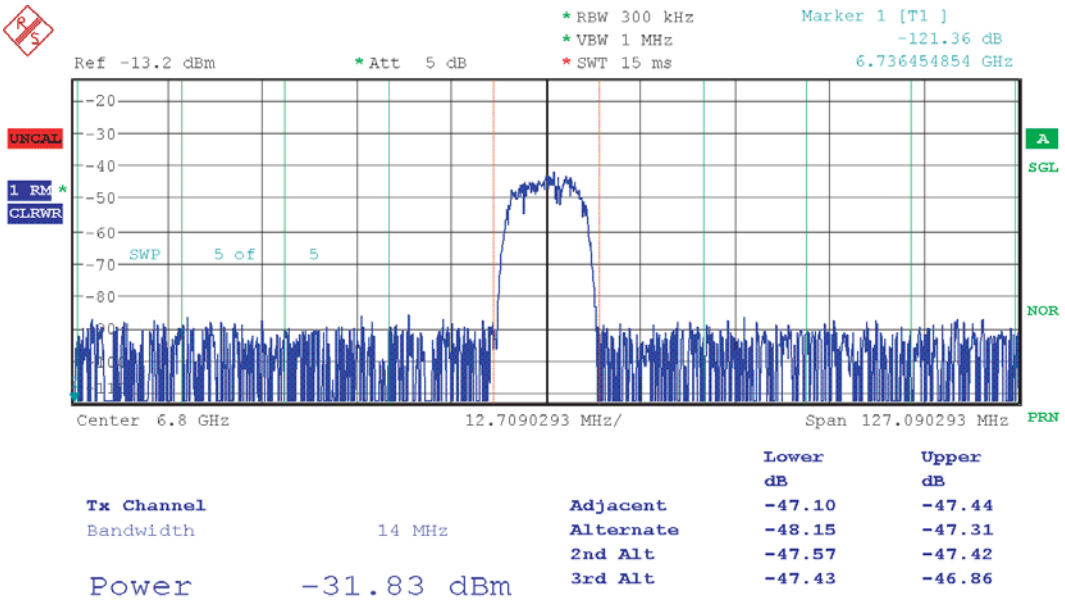
**Figure 7-33.** RF Mode, 4th Nyquist Zone: Center Frequency is pushed to 6 GHz – 800 MHz = 5.2 GHz




ACPR is in excess of 53 dB. DMWS capability is proven for the fourth Nyquist zone in RF mode.

Note due to a notch of available Pout near the end of the 4th Nyquist zone in RF output mode, for DMWS beyond middle of 4th Nyquist zone it is recommended to use the NRTZ output mode instead of the RF output mode.

**Figure 7-34.** NRTZ Mode, 5th Nyquist Zone: Center Frequency is pushed to 6 GHz + 800 MHz = 6.8 GHz




ACPR is still in excess of 47 dB. DMWS capability if proven for the fifth Nyquist zone in NRTZ mode with reduced available dynamic range.



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### 7.2.6 DOCSIS v3.0 Capability Measurements

Measurements hereafter have been carried out on a soldered device EV12DS130A/B, in NRTZ mode at 3 GSps.

Note: Results illustrated hereafter (spectrum and zoom on notch) come from measurement on a EV12DS130A/B device (CI-CGA255 package). Measurements have been carried out using the ACP treatment of the spectrum analyzer Rhode & Schwarz FSU8, in RMS detection mode.

**Figure 7-35.** ACPR 1 Channel Centered on 300 MHz, Output Mode NRTZ

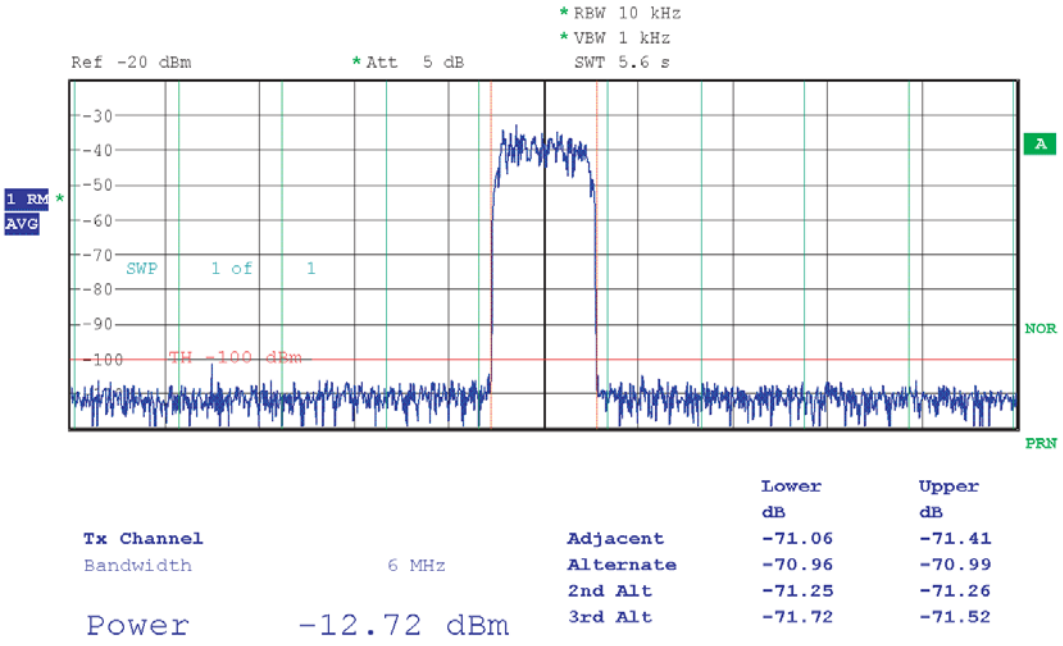
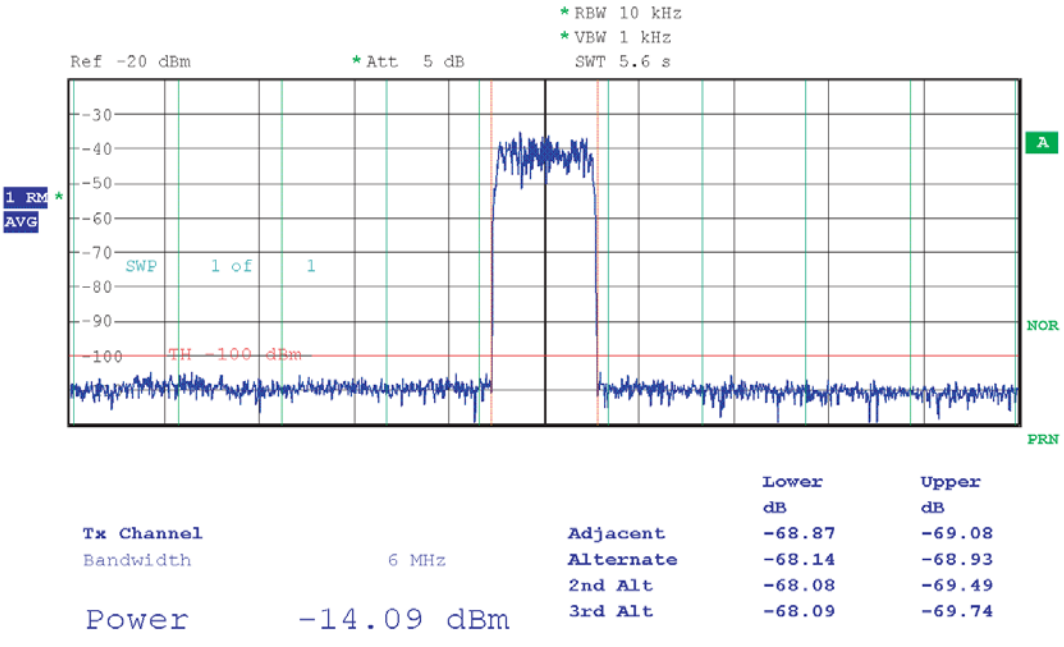



**Figure 7-36.** ACPR 1 Channel Centered on 900 MHz, Output Mode NRTZ






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**Figure 7-37.** ACPR 1 channel centered on 300 MHz, Output Mode NRTZ

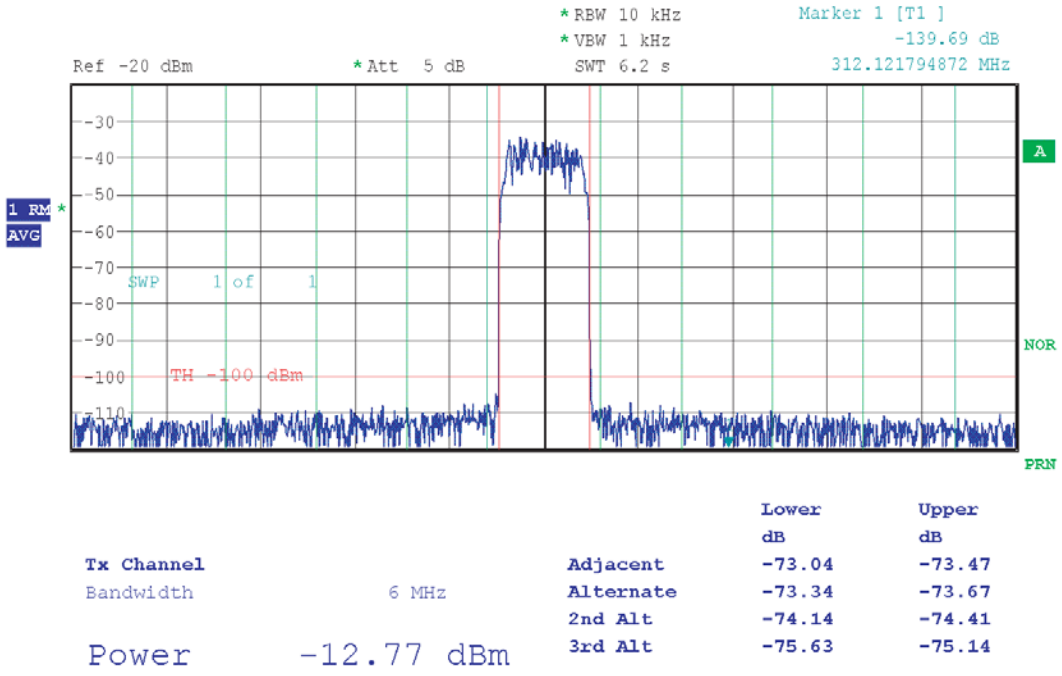
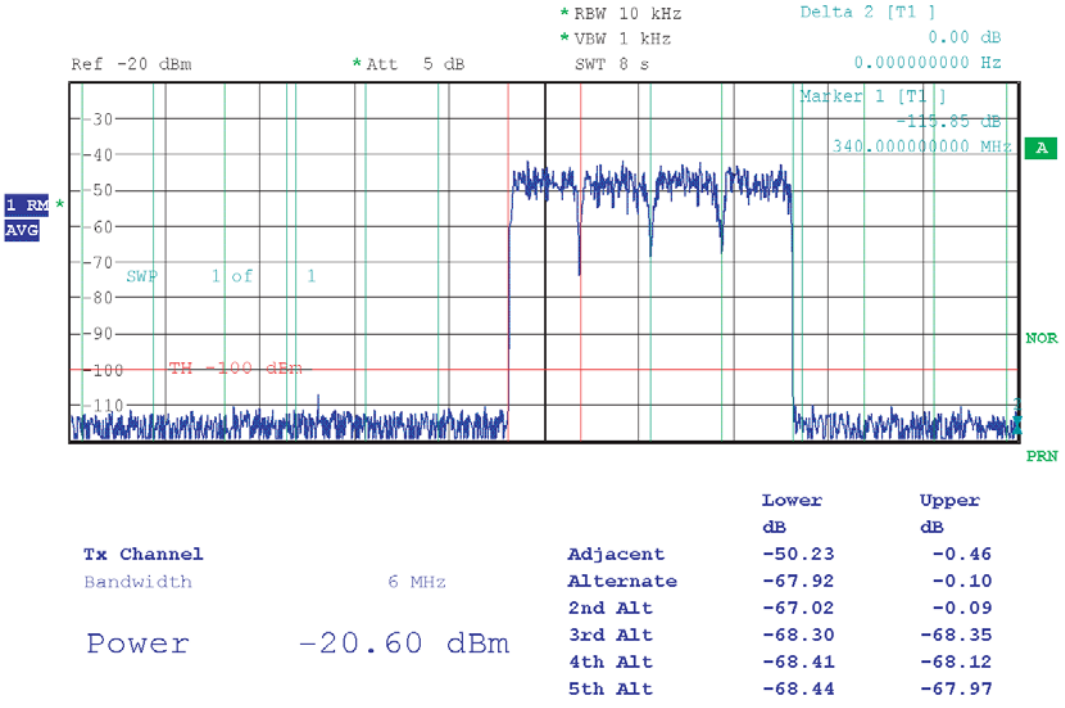



**Figure 7-38.** ACPR 4 Channels Centered on 300 MHz, Output Mode NRTZ






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**Figure 7-39.** ACPR 1 Channel Centered on 900 MHz, Output Mode NRTZ

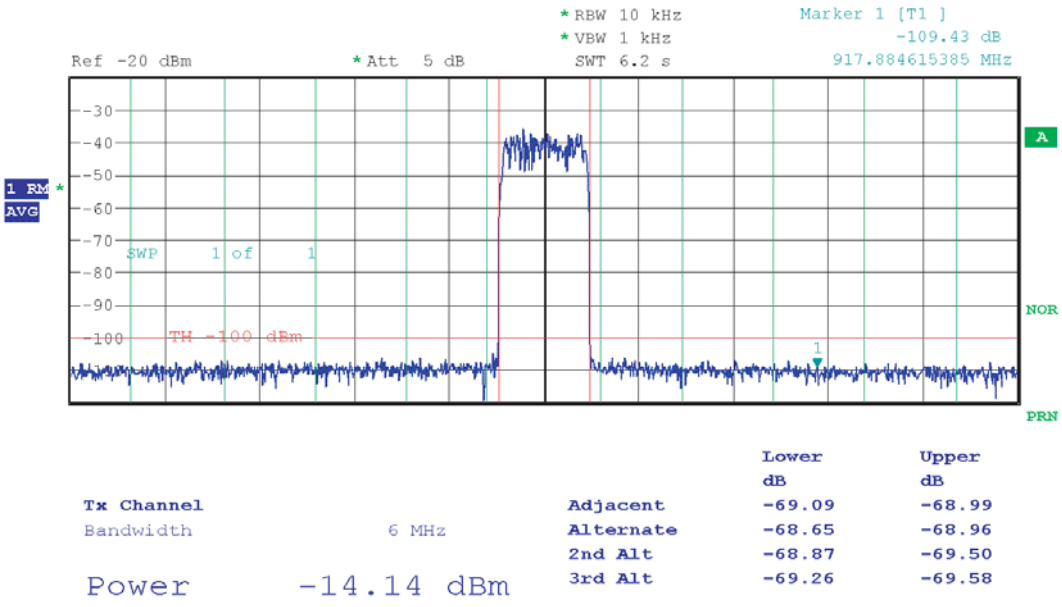
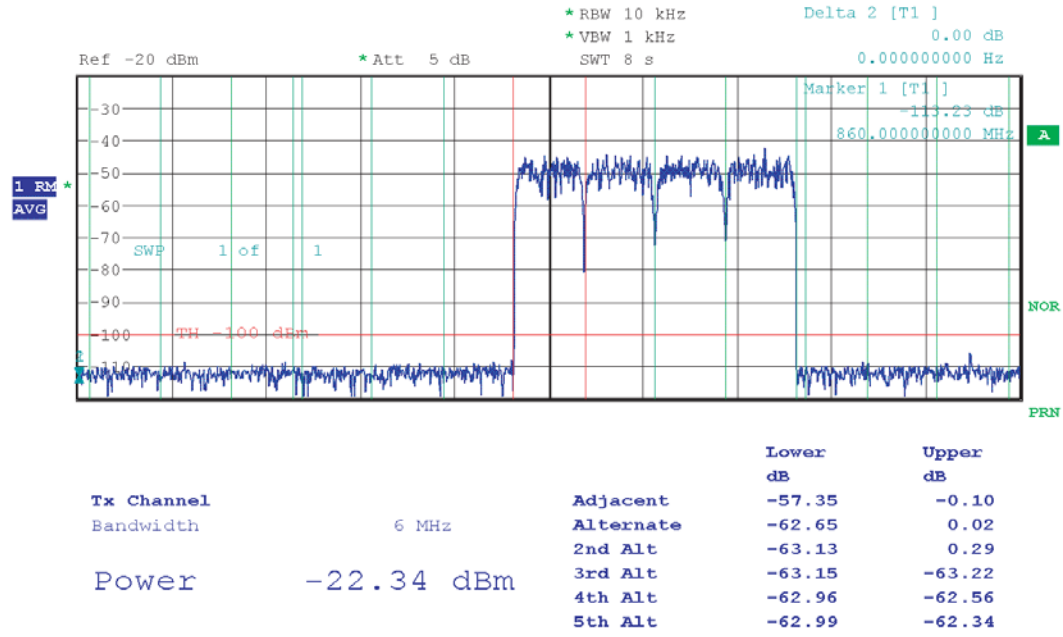



**Figure 7-40.** ACPR 4 Channels Centered on 900 MHz, Output Mode NRTZ





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### 7.2.7 NPR Performance

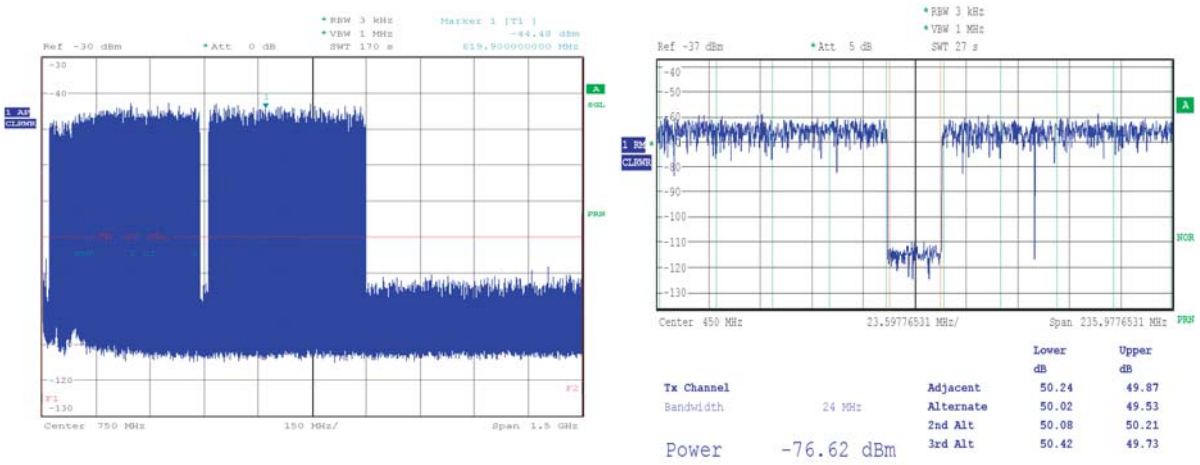
NPR measurements have been carried out at optimum loading factor (LF) for a 12 bit DAC, that is – 14 dBFS, with the DAC operating at 3 Gsps.

SNR can be computed from SNR measurement with the formula: $SNR_{[dB]} = NPR_{[dB]} + ILF_{[dB]}| - 3$.

ENOB can be computed with the formula: $ENOB = (SNR_{[dB]} - 1.76) / 6.02$.

Note: Results illustrated hereafter (spectrum and zoom on notch) come from measurement on a EV12DS130A/B device (CI-CGA255 package). Measurements have been carried out using the ACP treatment of the spectrum analyzer Rhode & Schwarz FSU8, in RMS detection mode.

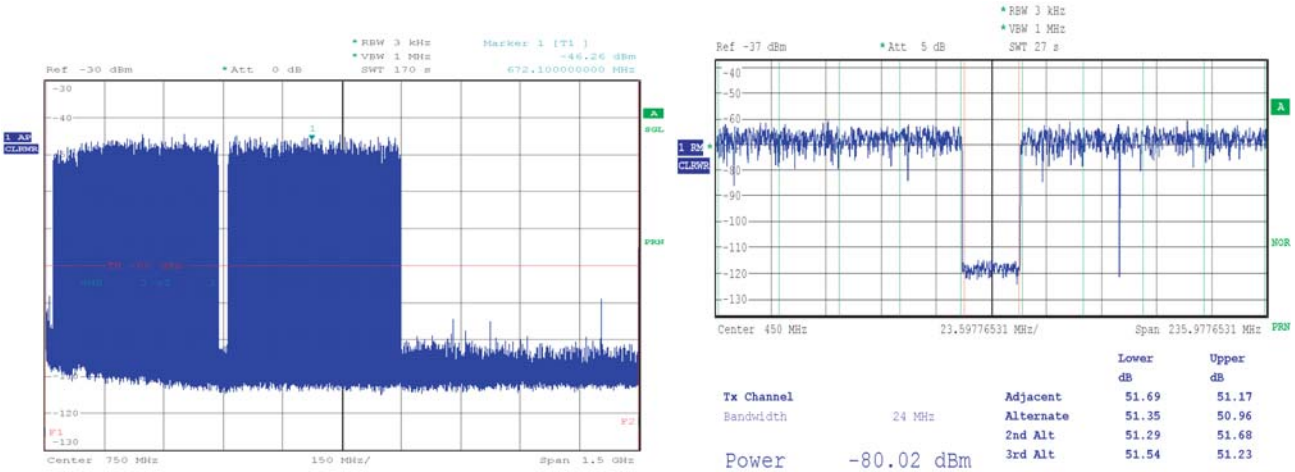
**Figure 7-41.** NPR in First Nyquist Zone, 20 MHz to 900 MHz Noise Pattern with a 25 MHz Notch Centered on 450 MHz, NRZ mode




Measured average NPR: 50.02 dB, therefore SNR = 61.02 dB and ENOB = 9.84 bit

Effects at low frequency are due to balun and pattern.

**Figure 7-42.** NPR in First Nyquist Zone, 20 MHz to 900 MHz Noise Pattern with a 25 MHz Notch Centered on 450 MHz, NRTZ Mode



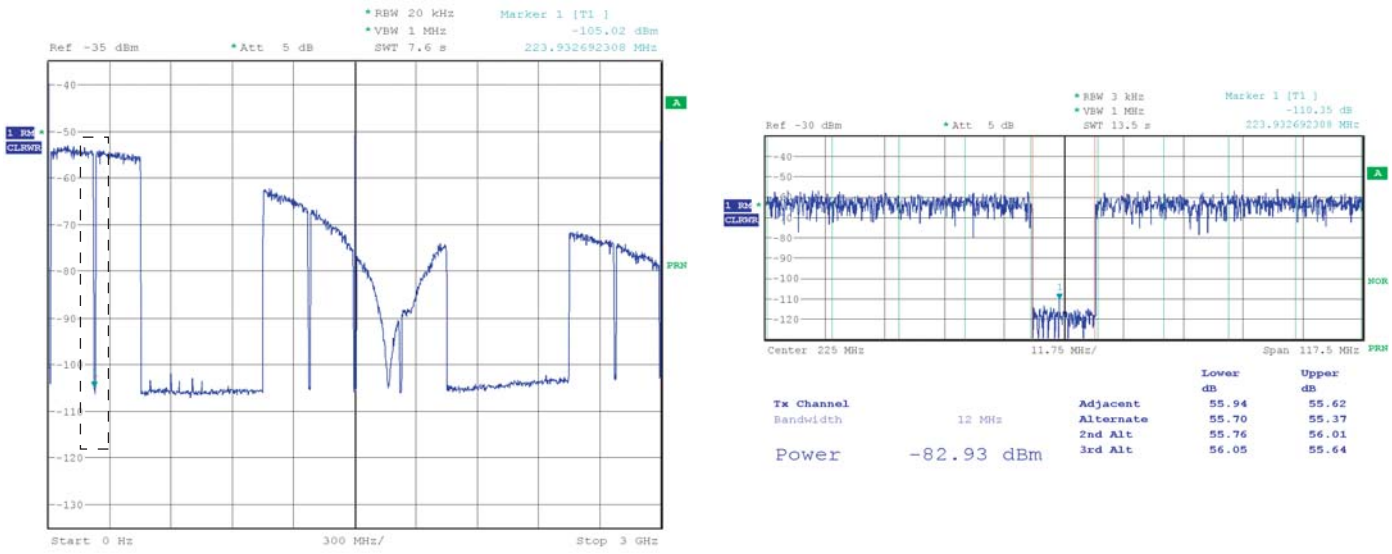

Measured average NPR: 51.36 dB, therefore SNR = 62.36 dB and ENOB = 10.07 bit.

Effects at low frequency are due to balun and pattern.



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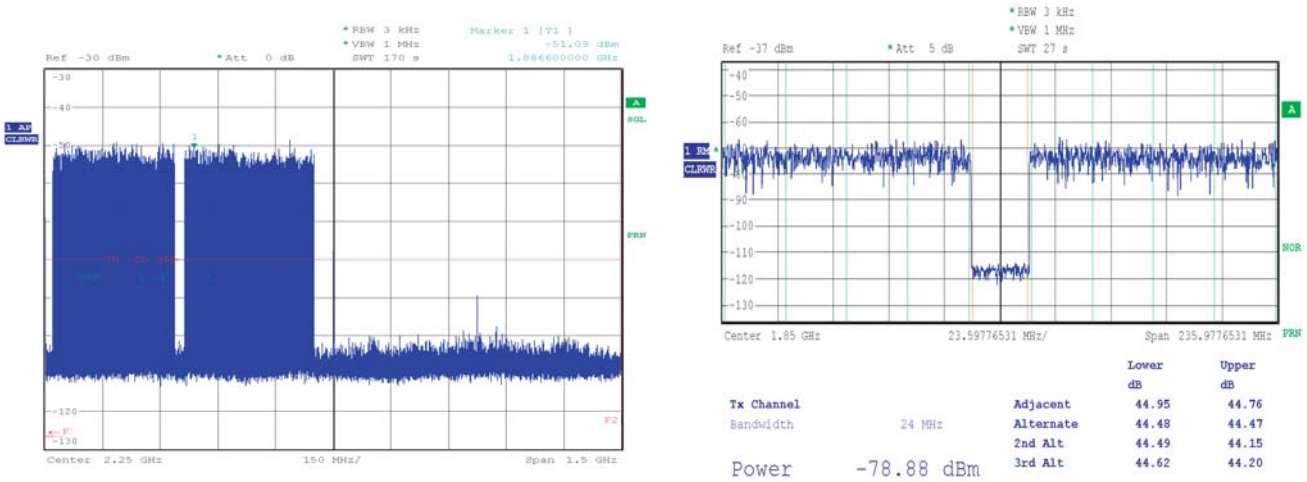
**Figure 7-43.** NPR in First Nyquist Zone, 10 MHz to 450 MHz Noise Pattern with a 12.5 MHz Notch centered on 225 MHz, NRTZ Mode at Fs = 1.5 Gsps




Measured average NPR: 55.7 dB, therefore SNR = 66.7 dB and ENOB = 10.8 bit.

Effects at low frequency are due to balun and pattern.

**Figure 7-44.** NPR in second Nyquist Zone, 1520 MHz to 2200 MHz Noise Pattern with a 25 MHz Notch centered on 1850 MHz, RTZ mode

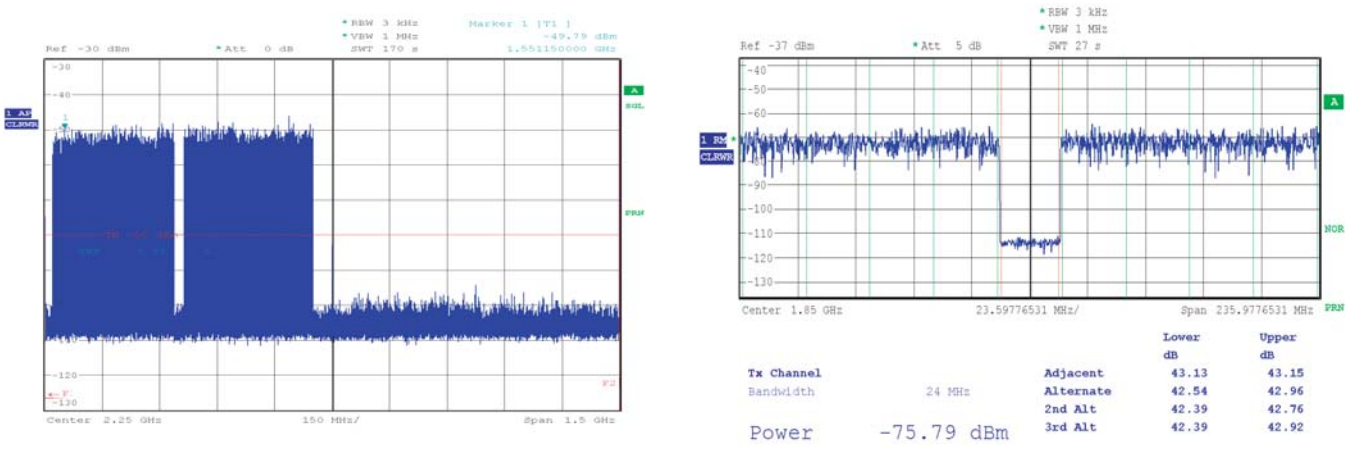



Measured average NPR: 44.6 dB, therefore SNR = 55.6 dB and ENOB = 8.94 bit



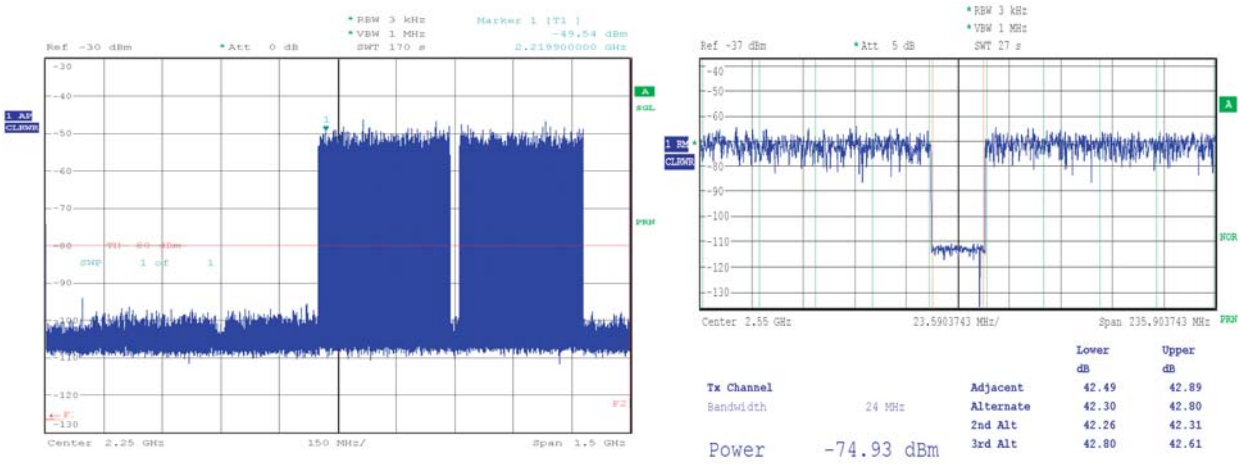
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**Figure 7-45.** NPR in second Nyquist Zone, 1520 MHz to 2200 MHz noise pattern with a 25 MHz notch centered on 1850 MHz, RF Mode




Measured average NPR: 42.78 dB, therefore SNR = 53.78 dB and ENOB = 8.64 bit

**Figure 7-46.** NPR in second Nyquist Zone, 2200 MHz to 2880 MHz Noise Pattern with a 25 MHz Notch centered on 2550 MHz, RF Mode

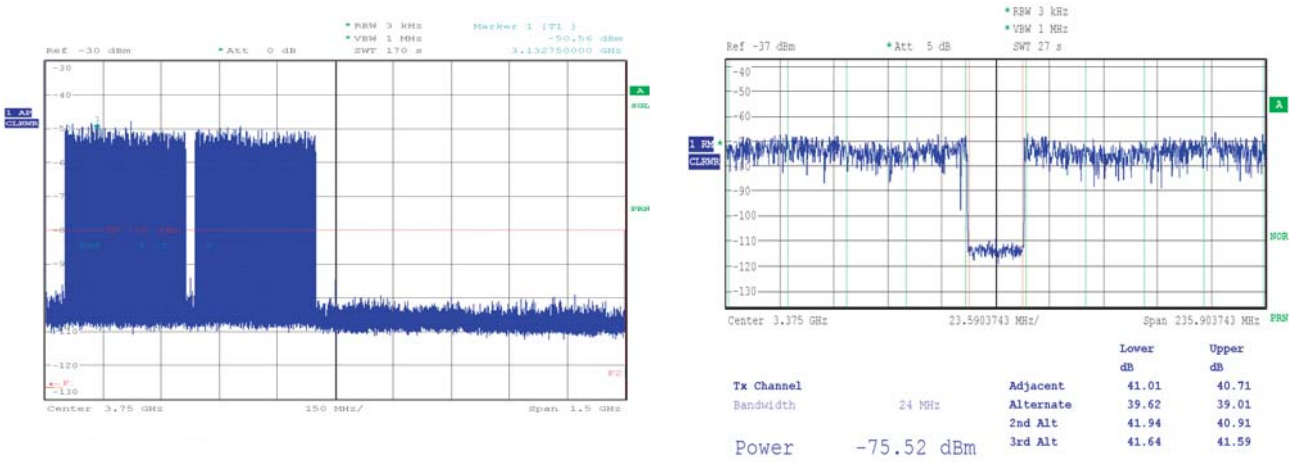



Measured average NPR: 42.56 dB, therefore SNR = 53.56 dB and ENOB = 8.6 bit.



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**Figure 7-47.** NPR in Third Nyquist Zone, 3050 MHz to 3700 MHz Noise Pattern with a 25 MHz Notch Centered on 3375 MHz, RF Mode

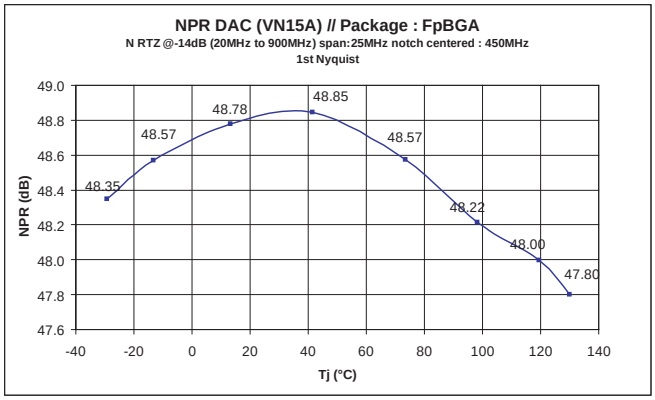


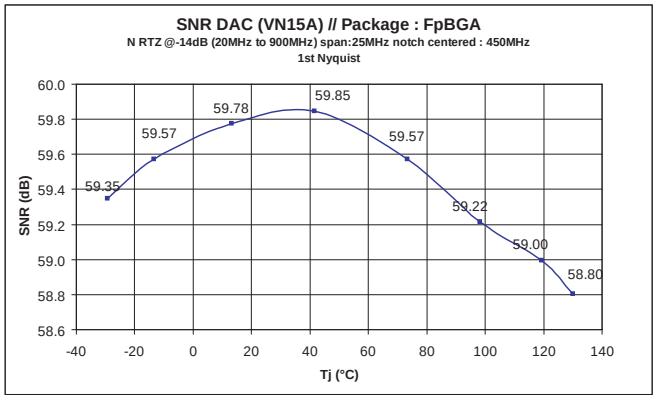

Measured average NPR: 40.08 dB, therefore SNR = 51.08 dB and ENOB = 8.19 bit

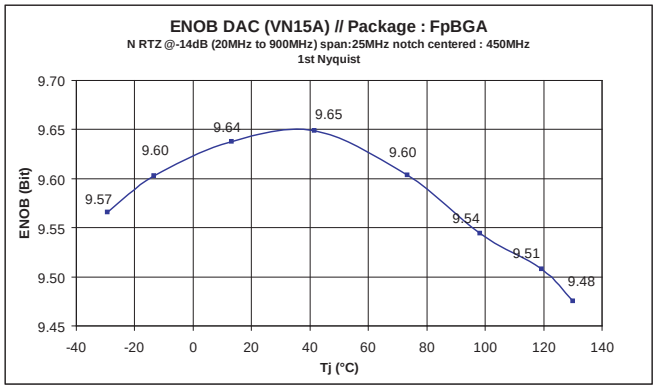
The following figures reflect the stability of NPR in first Nyquist in NRTZ mode (and therefore SNR and ENOB) versus temperature.

Measurements have been carried out at nominal power supply on an EV12DS130A/B, at 3 Gsps, with the FSU8 spectrum analyzer in RMS detection mode.

**Figure 7-48.** Drift of NPR and Associated SNR and ENOB in First Nyquist in NRTZ Mode from Tj = –30°C to Tj = 125°C



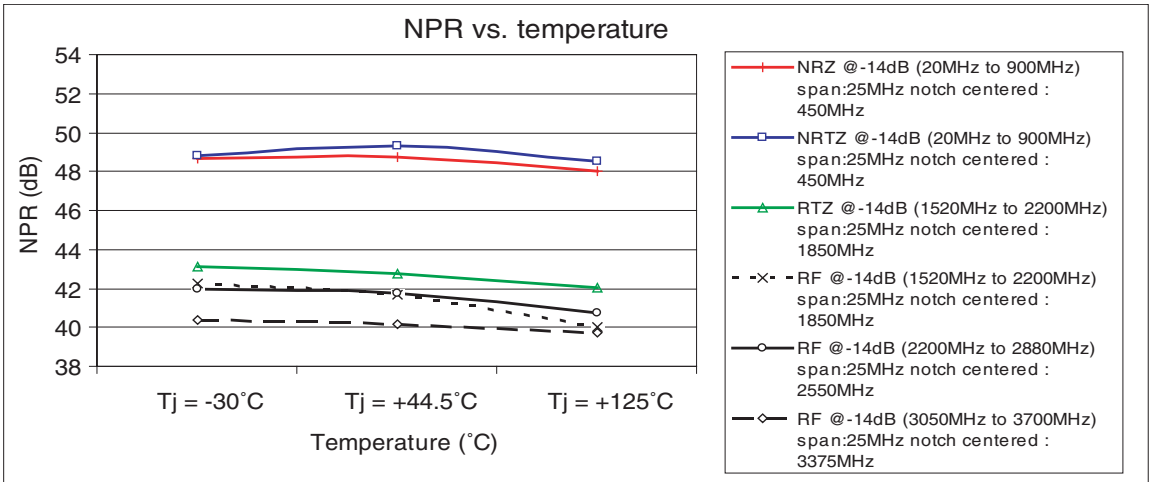



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Optimum is at Tj = 40°C, degradation over temp is within 1 dB (or 0.15 effective bit).

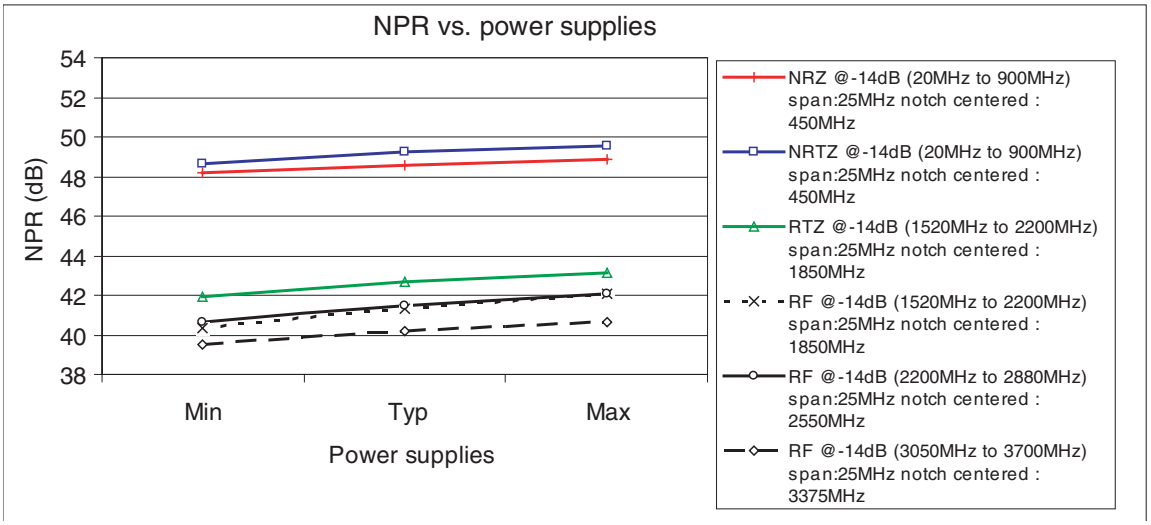
Measurements hereafter have been carried out on an EV12AS130AGS device at 3 Gsps, with the FSU8 spectrum analyzer in RMS detection mode.

**Figure 7-49.** Drift of NPR vs temperature in the 4 Output Modes at Nominal Supply




Conclusion: performances are stable in the four output modes against temperature.

**Figure 7-50.** NPR vs Power Supply Level in the 4 Output Modes at Room Temperature




Conditions: Typical, excepted: power supplies

Min: $V_{CCA}$: 4.75V // $V_{CCA3}$ = $V_{CCD}$ = 3.15V
Typ: $V_{CCA}$: 5.0V // $V_{CCA3}$ = $V_{CCD}$ = 3.3V
Max: $V_{CCA}$: 5.25V // $V_{CCA3}$ = $V_{CCD}$ = 3.45V.

Conclusion: performances are fairly stable against power supply.

Note: NPR performance at lower clock frequencies is affected by power up sequence. See application note 1087 for further details.



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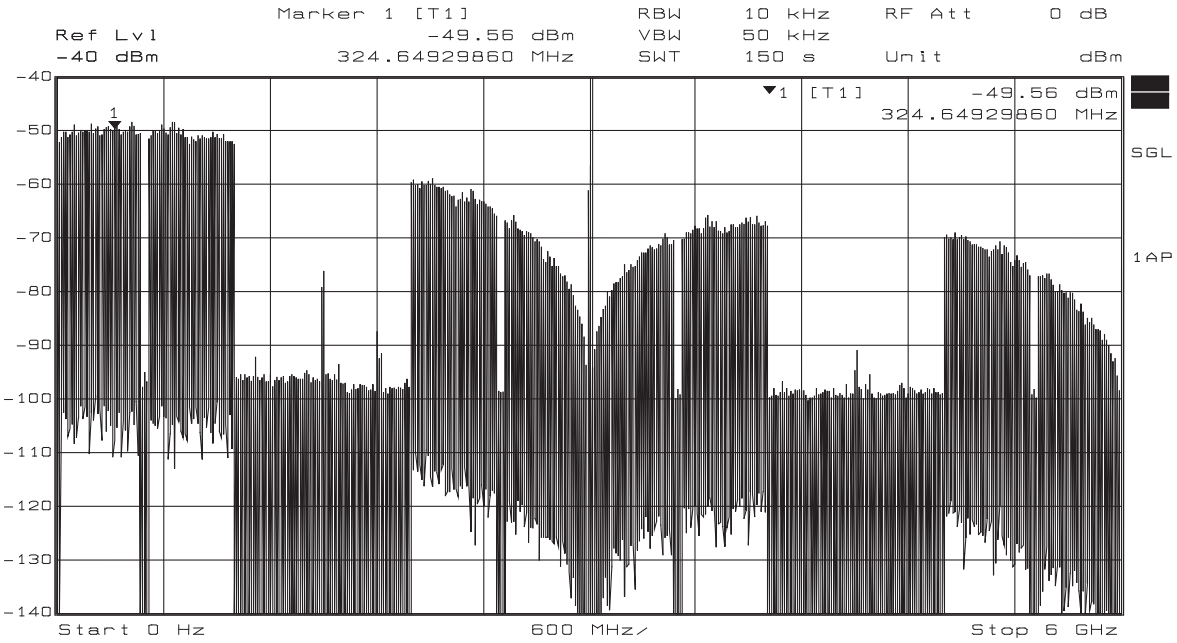
### 7.2.8 Spectrum over 4 Nyquist Zones in the Four Output Modes

Observation of a 1GHz broadband pattern with a 25 MHz notch centered on 500 MHz spectrum over 4 Nyquist zones at 3 Gsps (that is from DC to 6 GHz), measurements performed on an EV12DS130A/B device (CI-CGA 255 package, with an overall 6 GHz bandwidth limitation).

By periodisation of a sampled system each tone $F_i$ of the pattern in the 1st Nyquist zone is duplicated as follows:

- 2nd Nyquist Zone: tone at Fclock - $F_i$
- 3rd Nyquist Zone: tone at Fclock + $F_i$
- 4th Nyquist Zone: tone at 2*Fclock - $F_i$

**Figure 7-51.** Spectrum over 4 Nyquist Zones at 3 Gsps in NRZ Output Mode




First Zero of the sinc() function is at Fclock.



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**Figure 7-52.** Spectrum over 4 Nyquist Zones at 3 Gsps in NRTZ Output Mode

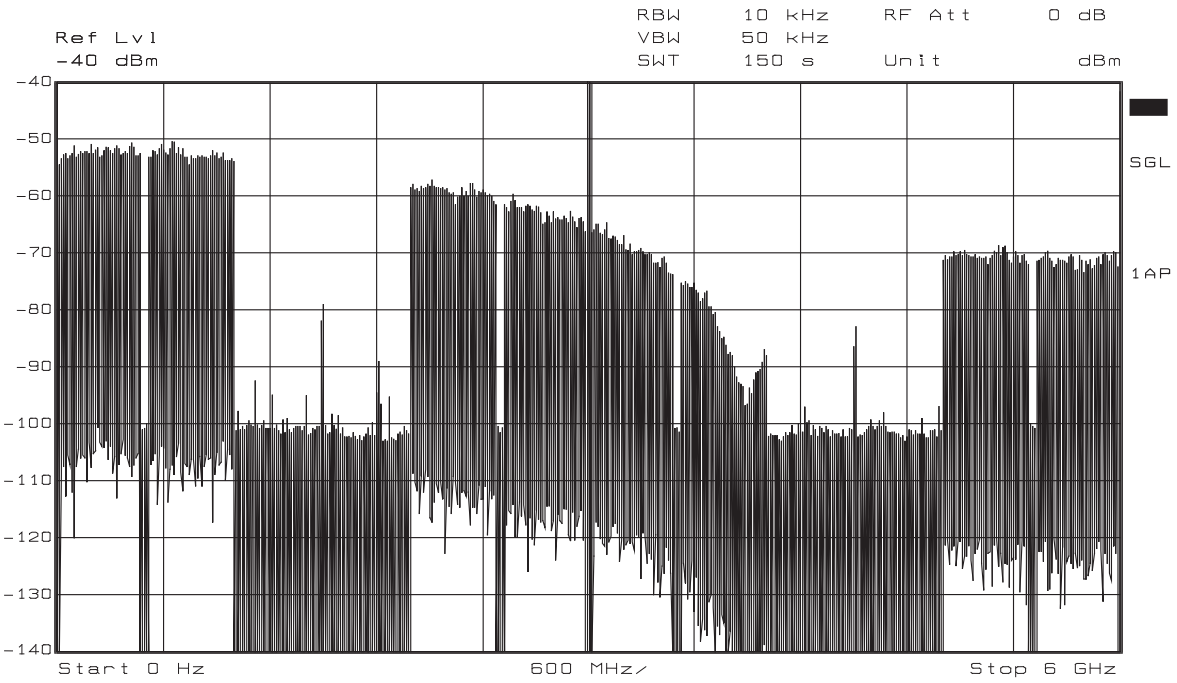
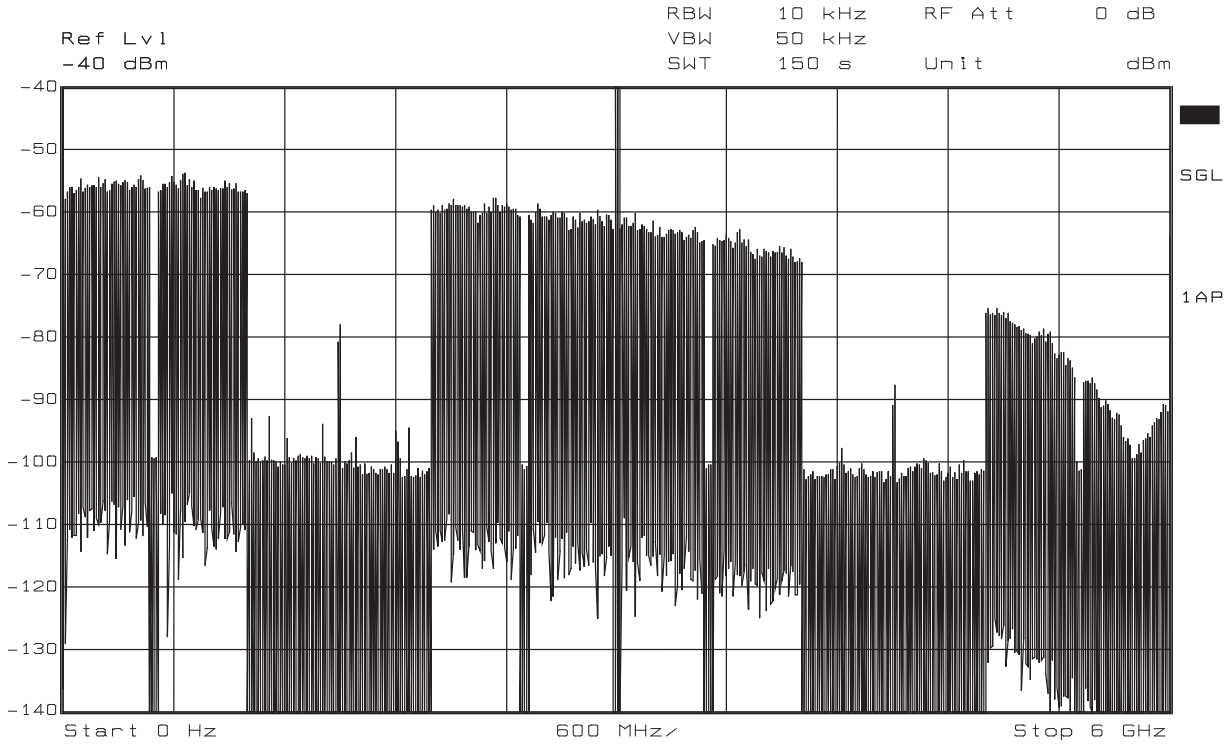



**Figure 7-53.** Spectrum over 4 Nyquist Zones at 3 Gsps in RTZ Output Mode

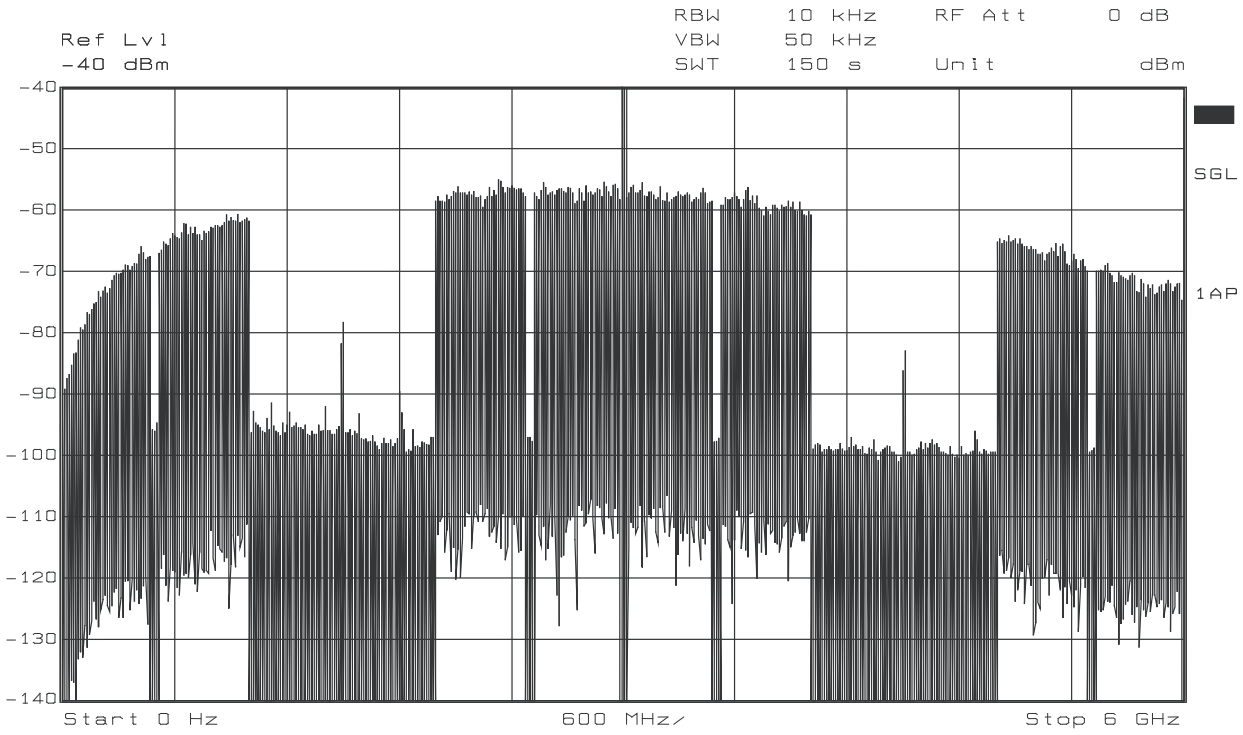





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First Zero of the sinc() function is slightly before 2*Fclock which indicates that the duty cycle of RTZ function is a little bit more than 50%, this is due to the balun which introduced some phase error beyond the 180 degrees between CLK and CLKN thus creating a duty cycle on the clock actually seen by the DAC.

**Figure 7-54.** Spectrum over 4 Nyquist Zones at 3 Gsps in RF Output Mode




Measurements are showing a pretty good fit with theory, see Section 5.3 on page 18.



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# 8. APPLICATION INFORMATION

For further details, please refer to application note 1087.

## 8.1 Analog Output (OUT/OUTN)

The analog output should be used in differential way as described in the figures below.

If the application requires a single-ended analog output, then a balun is necessary to generate a single-ended signal from the differential output of the DAC.

**Figure 8-1.** Analog Output Differential Termination

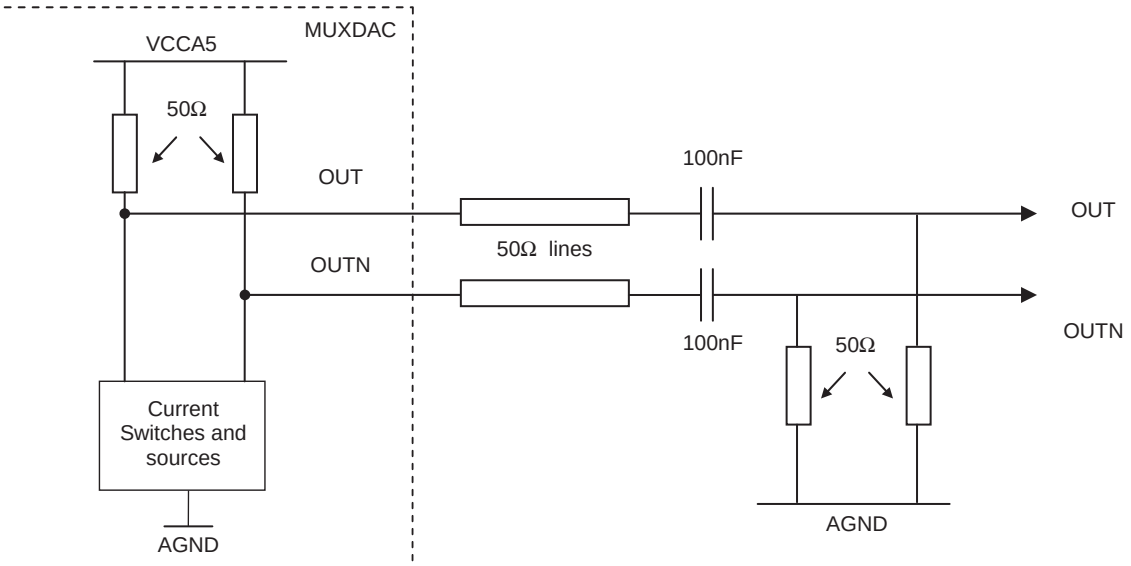
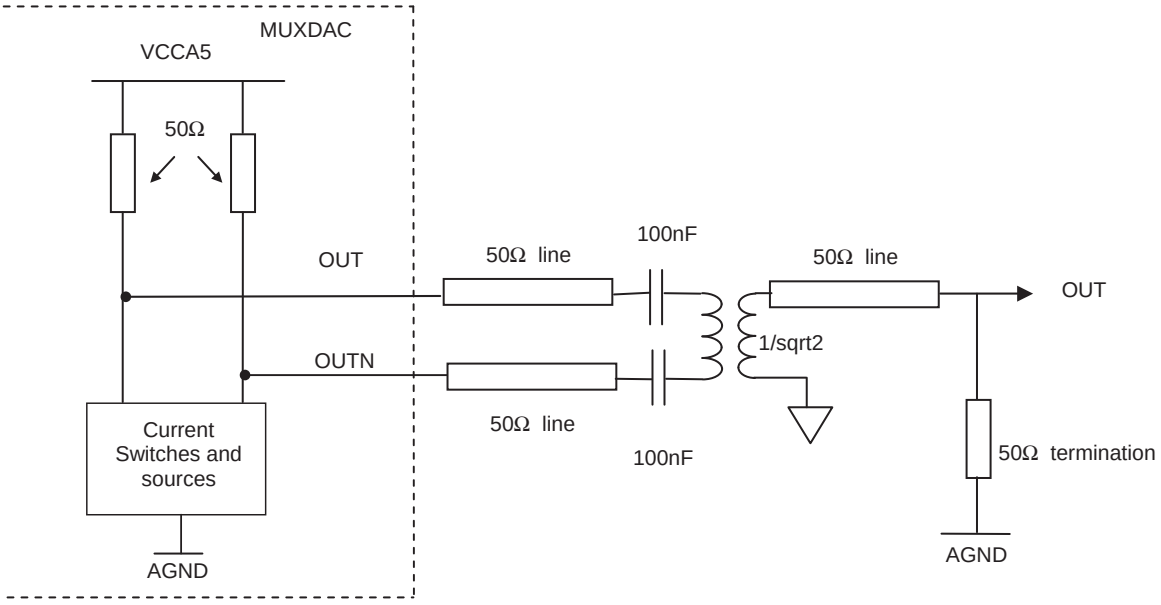



**Figure 8-2.** Analog Output Using a 1/ √2 Balun




Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

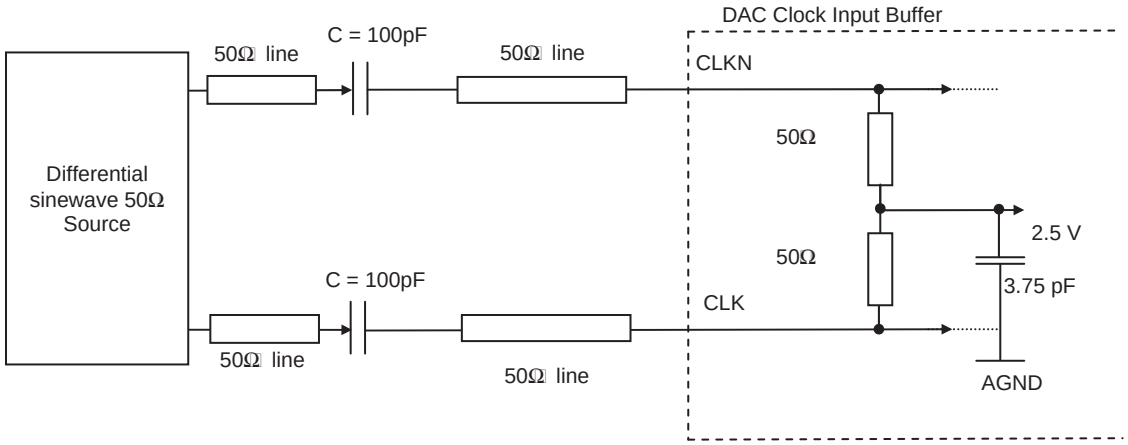


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## 8.2 Clock Input (CLK/CLKN)

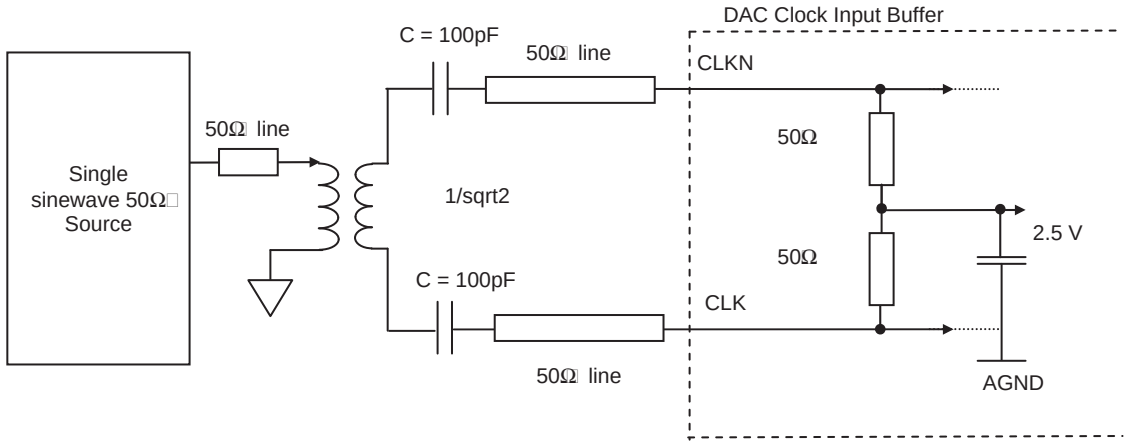
The DAC input clock (sampling clock) should be entered in differential mode as described in Figure 5-11.

**Figure 8-3.** Clock Input Differential Termination




Note: The buffer is internally pre-polarized to 2.5V (buffer between $V_{CC5}$ and AGND).

**Figure 8-4.** Clock Input Differential with Balun




Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

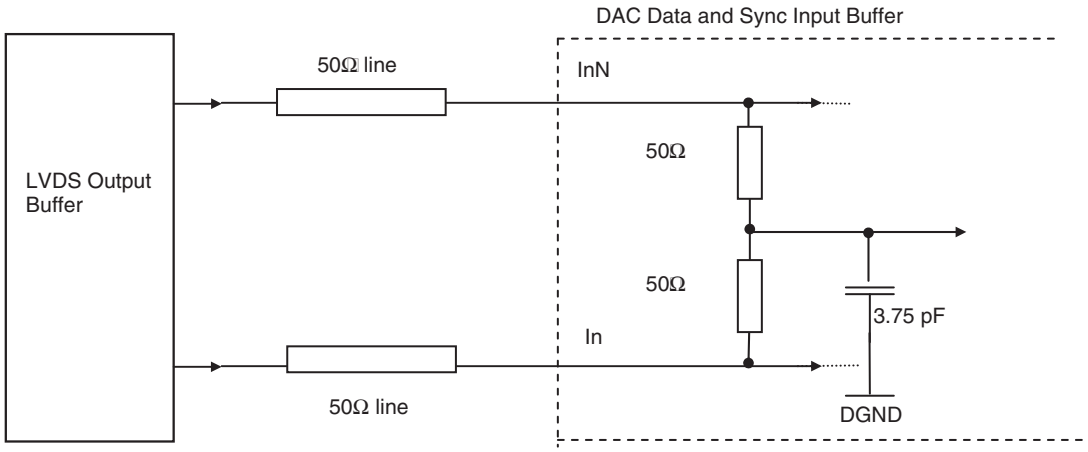

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## 8.3 Digital Data, SYNC and IDC Inputs

LVDS buffers are used for the digital input data, the reset signal (active high) and IDC signal.

They are all internally terminated by 2 × 50Ω to ground via a 3.75 pF capacitor.

**Figure 8-5.** Digital Data, Reset and IDC Input Differential Termination



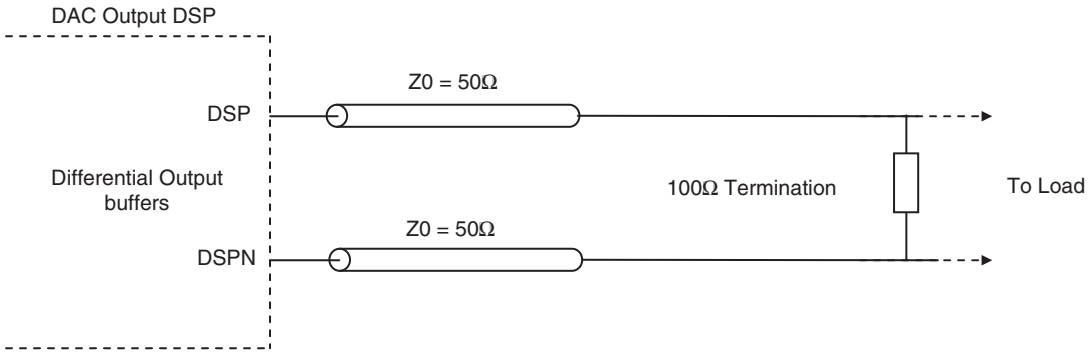

Notes:
1. In the case when only two ports are used (2:1 MUX ratio), then the unused data should be left open (no connect).
2. Data and IDC signals should be routed on board with the same layout rules and the same length than the data.
3. In case SYNC is not used, it is necessary to bias the SYNC to 1.1V and SYNCN to 1.4V on EV12DS130A.

## 8.4 DSP Clock

The DSP, DSPN output clock signals are LVDS compatible.

They have to be terminated via a differential 100Ω termination as described in Figure 5-13.

**Figure 8-6.** DSP Output Differential Termination





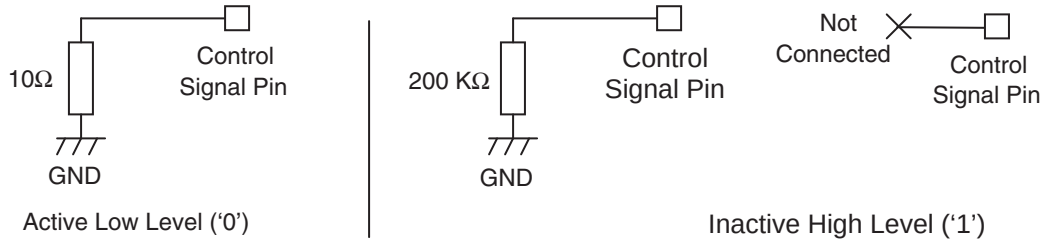

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## 8.5 Control Signal Settings

The MUX, MODE, PSS and OCDS control signals use the same static input buffer.

Logic “1” = 200 KΩ to Ground, or tied to $V_{CCD}$ = 3.3V or left open
Logic “0” = 10Ω to Ground or Grounded

**Figure 8-7.** Control Signal Settings




The control signal can be driven by FPGA.

**Figure 8-8.** Control Signal Settings with FPGA




Logic “1” > $V_{IH}$ or $V_{CCD}$ = 3.3V

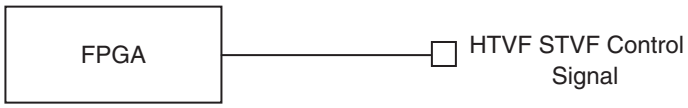
Logic “0” < $V_{IL}$ or 0V

## 8.6 HTVF and STVF Control Signal

The HTVF and STVF control signals is a 3.3V CMOS output buffer.

These signals could be acquired by FPGA.

**Figure 8-9.** Control Signal Settings with FPGA




In order to modify the $V_{OL}/V_{OH}$ value, pull up and pull down resistances could be used, or a potential divider.

## 8.7 GA Function Signal

This function allows adjustment of the internal gain of the DAC.

The gain of the DAC can be tuned with applied analog voltage from 0 to $V_{CCA3}$

This analog input signal could be generated by a DAC controlled by FPGA or microcontroller.

**Figure 8-10.** Control Signal Settings with GA






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## 8.8 Power Supplies Decoupling and Bypassing

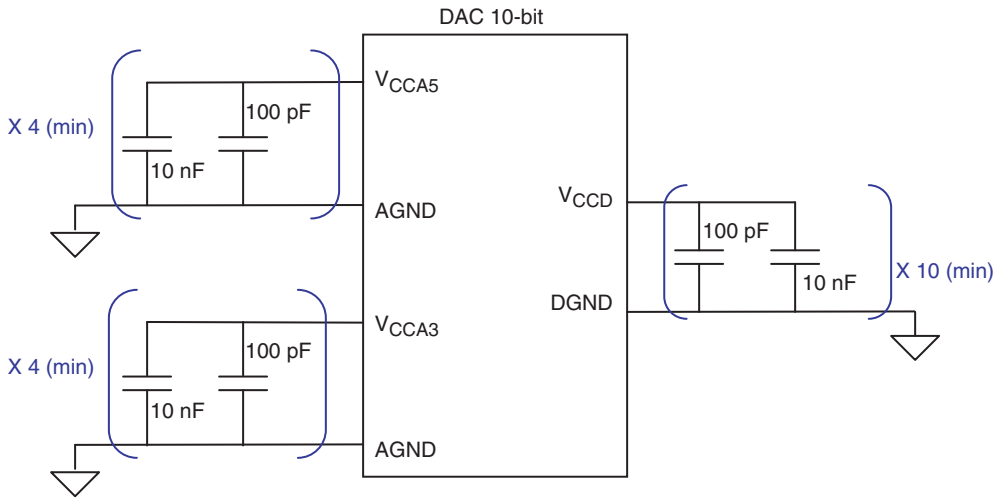
The DAC requires 3 distinct power supplies:

$V_{CCA5}$ = 5.0V (for the analog core)
$V_{CCA3}$ = 3.3V (for the analog part)
$V_{CCD}$ = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins.

4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of $V_{CCA5}$. 4 pairs for the $V_{CCA3}$ is the minimum required and finally, 10 pairs are necessary for $V_{CCD}$.

**Figure 8-11.** Power Supplies Decoupling Scheme




Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 22 µF capacitors (value depending of DC/DC regulators).

Analog and digital ground plane should be merged.



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## 8.9 Power Up Sequencing

**For EV12DS130B there is no forbidden power-up sequence, nor power supplies dependency requirement.**

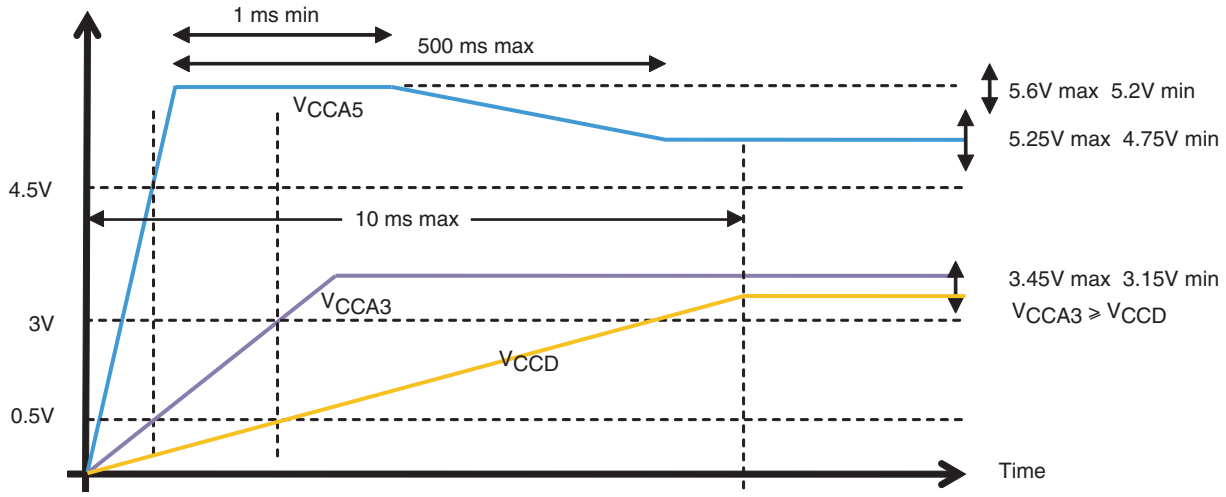
**For EV12DS130A the following instructions must be implemented:**

Power-up sequence:

It is necessary to raise $V_{CCA5}$ power supply within the range 5.20V up to a recommended maximum of 5.60V during at least 1ms at power up. Then the supply voltage has to settle within 500 ms to a steady nominal supply voltage within a range of 4.75V up to 5.25V.

A power-up sequence on $V_{CCA5}$ that does not comply with the above recommendation will not compromise the functional operation of the device. Only the noise floor will be affected.

**Figure 8-12.** Power-up Sequence




The rise time for any of the power supplies ($V_{CCA5}$, $V_{CCA3}$ and $V_{CCD}$) shall be ≤ 10 ms.

At power-up a SYNC pulse is internally and automatically generated when the following sequence is satisfied: $V_{CCD}$, $V_{CCA3}$ and $V_{CCA5}$. To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: $V_{CCA5}$, $V_{CCA3}$, $V_{CCD}$. (It is mandatory that $V_{CCD}$ is the last supply to rise and always remains behind $V_{CCA5}$ and $V_{CCA3}$). Any other sequence may not have a deterministic SYNC behaviour. See erratasheet (ref 1125) for specific condition of use relative to the SYNC operation.

Relationship between power supplies:
Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy.



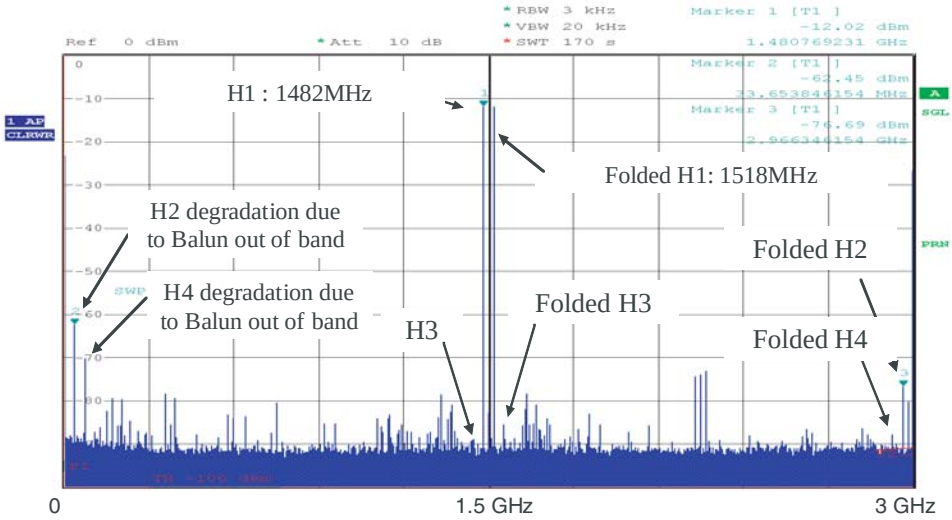
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## 8.10 Balun Influence

It is important to know that balun characteristic may influence significantly DAC output spectral response. Especially harmonic distortion can dramatically be degraded when part of the band of interest lies out of the specified domain of the balun.

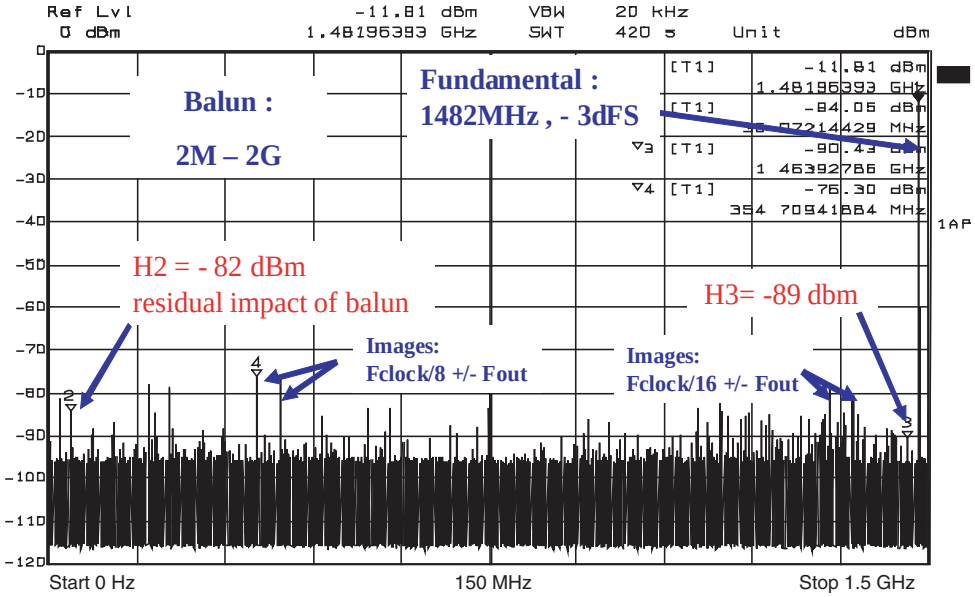
As depicted in the following figure an inappropriate balun choice can result in a strong increase in harmonic peaks amplitude, thus degrading performances. The balun used in this measurement covers only the 500MHz to 7GHz band so that the DC to 500MHz region of the first nyquist zone is distorted.

**Figure 8-13.** Observation of the 1st and 2nd nyquist zones in output mode RTZ with 0.5 GHz-7 GHz Balun




On the opposite, when appropriate balun is used the real device response is measured.

**Figure 8-14.** Spectrum of the 1st Nyquist Zone, Output Mode RTZ with a 2 MHz to 2GHz Bandwidth Balun



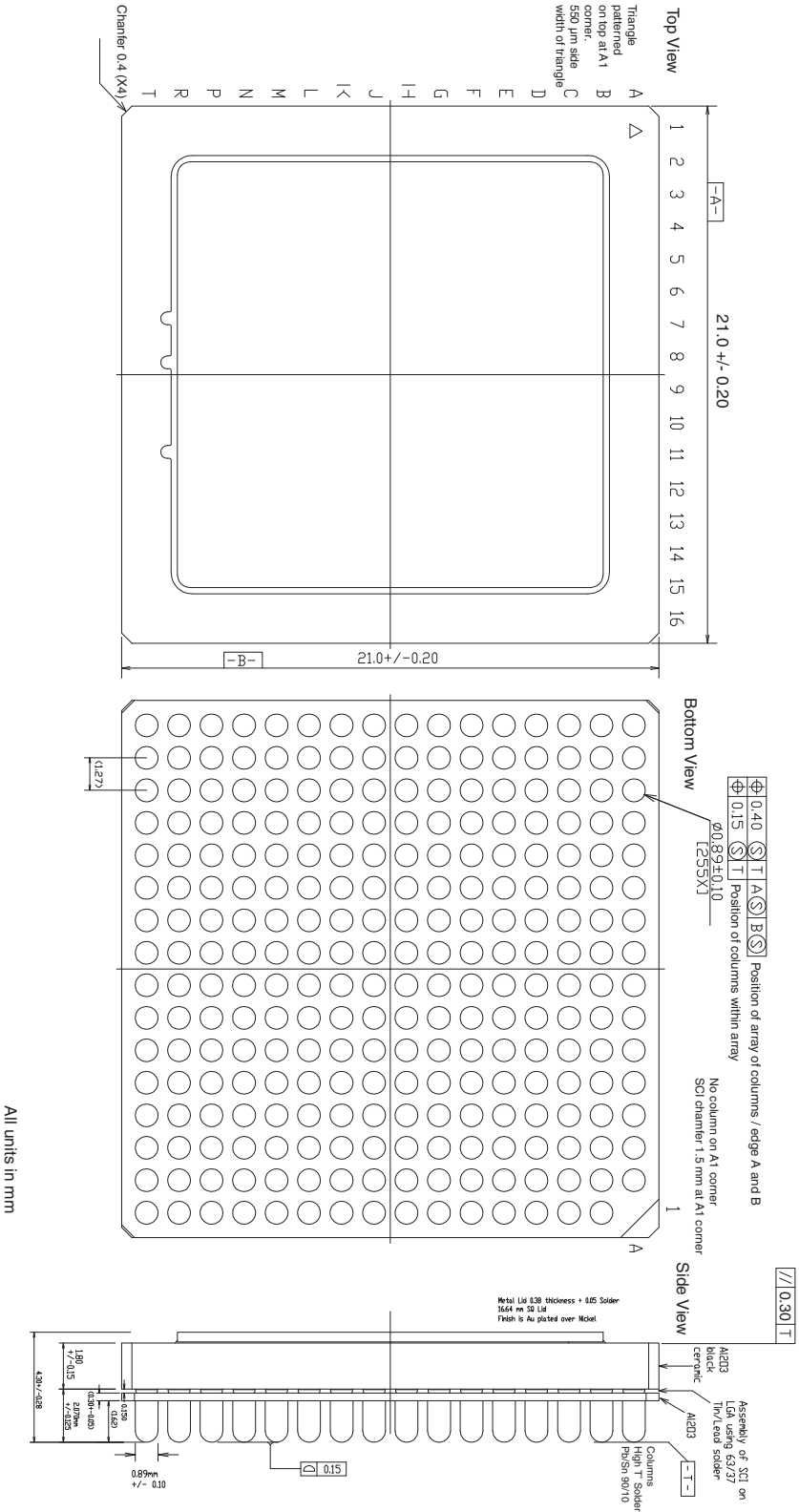

As a consequence, one must be aware that optimum performances can only be reached when using a balun optimal for the band of interest of the application. We specifically recommend selecting a balun which frequency domain covers the whole band of interest (for instance one whole Nyquist zone).



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# 9. PACKAGE DESCRIPTION

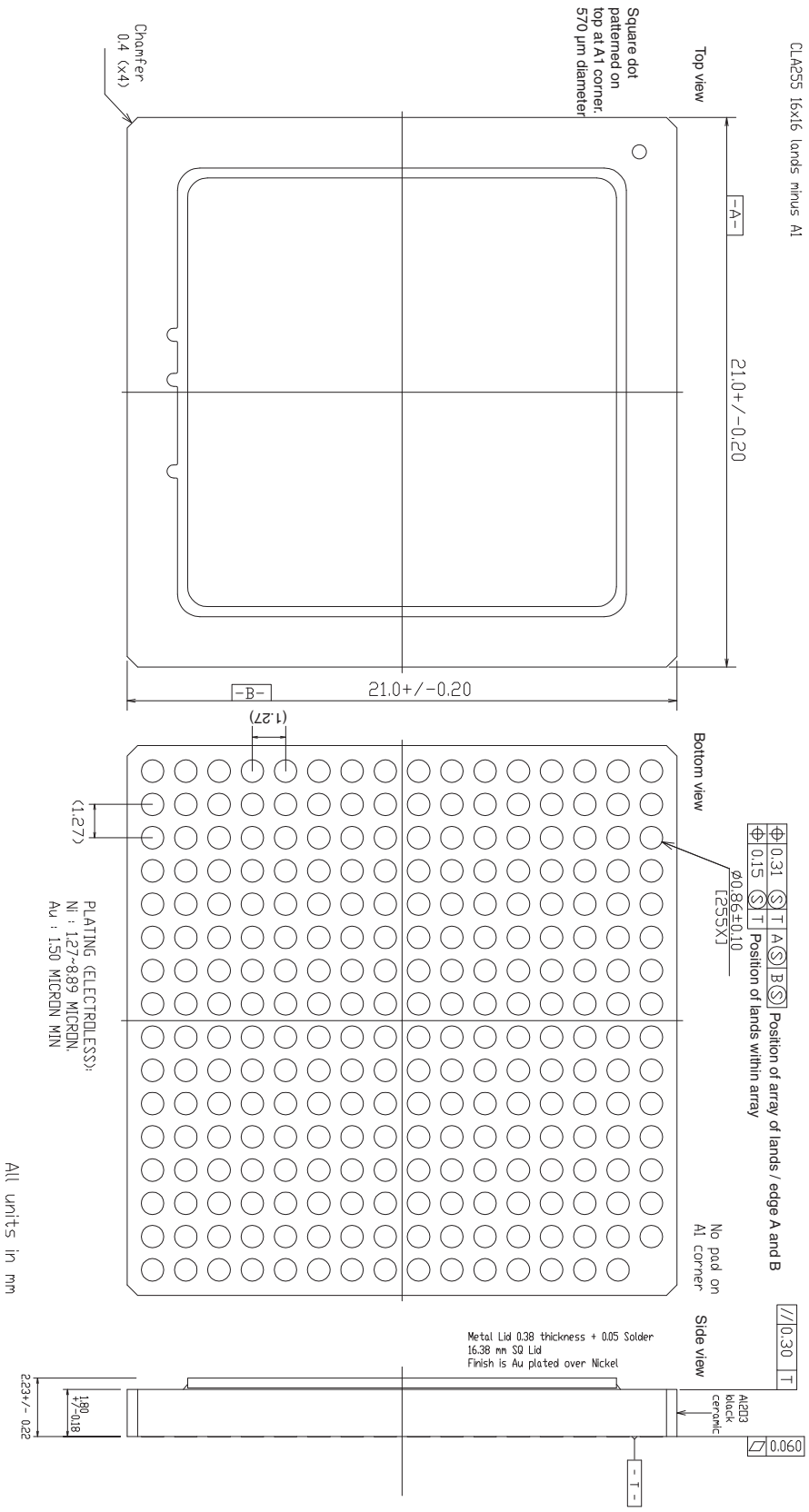
## 9.1 Ci-CGA255 Outline






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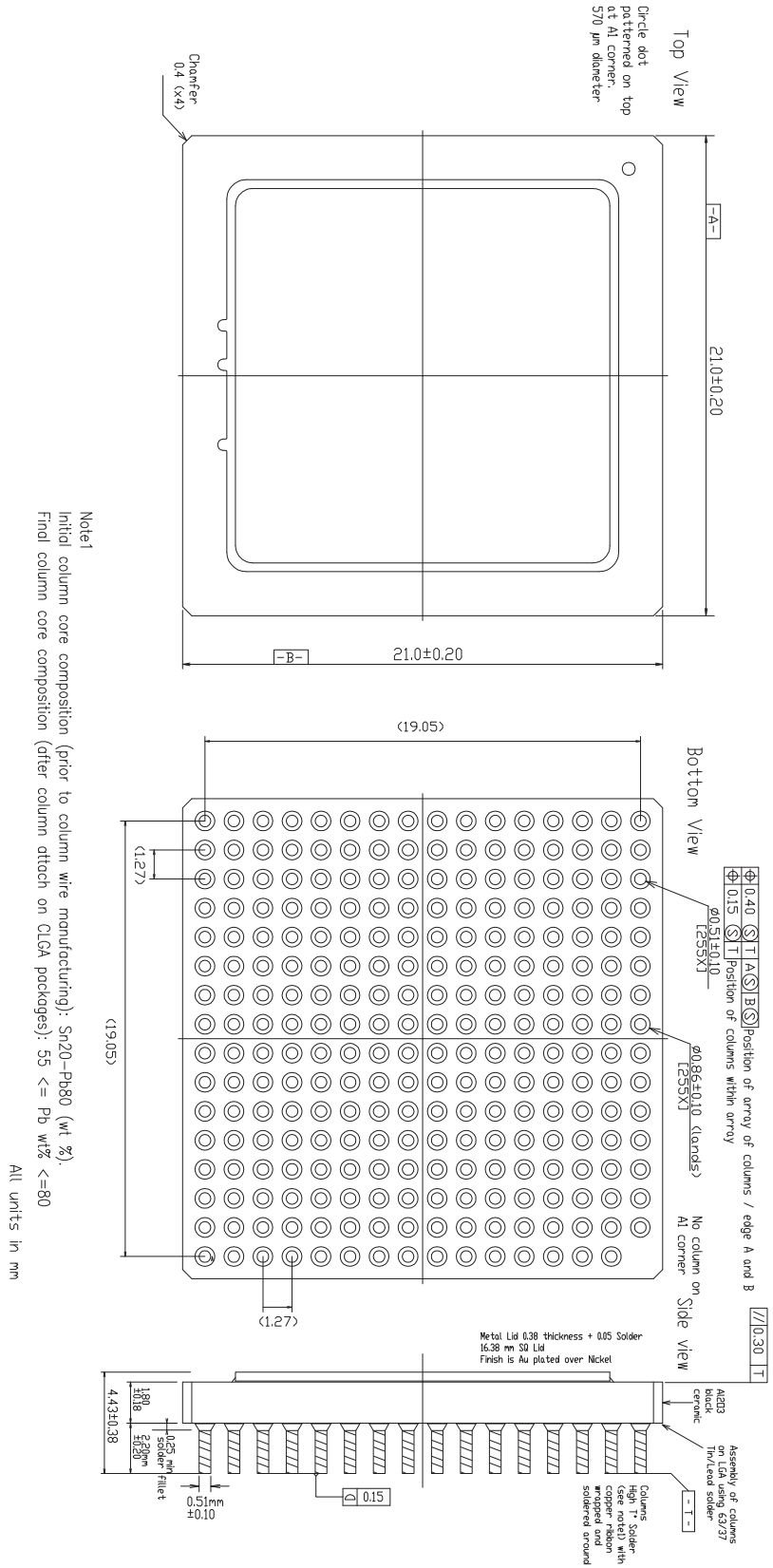
## 9.2 CLGA255 Outline






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## 9.3 CCGA255 Outline






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### 9.4 Thermal Characteristics

Assumptions:

- Die thickness = 300 µm
- No convection
- Pure conduction
- No radiation

| $R_{TH}$ | Heating zone | Ci CGA | CCGA | Unit |
|---|---|---|---|---|
| Junction-> Bottom of columns | 7.5% die area : 4580x4580 µm | 13.8 | 15.0 | °C/W |
| Junction-> Board ( JEDEC JESD51-8) Boad size = 39x39mm, 1.6 mm Thickness) | | 17.1 | 18.6 | °C/W |
| Junction -> Top of Lid | | 19.3 | 22.0 | °C/W |
| $T_{jhot\ spot} - T_{Jdiode}$ | | 3.3 | 3.3 | °C/W |

Typical Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Board size 114.3 × 76.2 mm, 1.6 mm thickness

| $R_{TH}$ | Heating zone | Ci CGA | CCGA | Unit |
|---|---|---|---|---|
| Junction -> Ambient | 18% die area : 4820x4820 µm | 29.5 | 29.4 | °C/W |
| $T_{jhot\ spot} - T_{Jdiode}$ | | 3.3 | 3.3 | °C/W |

## 10. DIFFERENCES BETWEEN EV12DS130A AND EV12DS130B

EV12DS130A and EV12DS130B exhibit the same dynamic performances.

EV12DS130B requires no specific dependency between power supplies nor power up sequences while the EV12DS130A does require specific power up sequences as described in Section 8.9 on page 75.

Maximum supported sampling frequency with DSP clock feature for EV12DS130B is 2.1GHz due to internal jitter. It is however possible to benefit from the EV12DS130B DAC performances up to 3GHz if specific system architecture is implemented. Please refer to application AN1141 for further information.



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No SYNC timing constraints (other than T1 T2) are required on EV12DS130B.

As a summary

When using EV12DS130A, please ensure your system fulfills those specific recommendations

- Power Up Sequence (See Section 8.9 on page 75)
- Power supplies dependency (see Section 8.9 on page 75)
- SYNC pin have to be driven in any case
- Please refer to errata sheet 1125

When using EV12DS130B, please ensure your system fulfills those specific recommendations

- In case sampling frequency is above 2.1 Gsps, please read the AN1141 “Using EV1xDS130B at sampling rate higher than 2.1GSps”

Please refer to application note AN1140 "Replacing EV1xDS130A with EV1xDS130B” for further details

## 11. ORDERING INFORMATION

Please refer to datasheet details and application notes before ordering.

**Table 11-1.** Ordering Information

| Part Number | SMD Number | Package | Temperature Range | Screening Level | Comments |
|---|---|---|---|---|---|
| **EV12DS130AG** | | | | | |
| EVX12DS130AGS | | CI-CGA255 | Ambient | Prototype | |
| EV12DS130AMGSD/T | | CI-CGA255 | –55°C < Tc,Tj < 125°C | EQM Grade | |
| EV12DS130AMGS9NB1 | | CI-CGA255 | –55°C < Tc,Tj < 125°C | Space Grade | |
| EV12DS130AGS-EB | | CI-CGA255 | Ambient | Prototype | Evaluation board |
| EVX12DS130ALG | | LGA255 | Ambient | Prototype | |
| EV12DS130AMLGD/T | | LGA255 | –55°C < Tc,Tj < 125°C | EQM Grade | |
| EV12DS130AMLG9NB1 | | LGA255 | –55°C < Tc,Tj < 125°C | Space Grade | |
| EVX12DS130AGC | | CCGA255 | Ambient | Prototype | |
| EV12DS130AMGC | | CCGA255 | –55°C < Tc,Tj < 125°C | Engineering model | |
| EV12DS130AMGCD/T | | CCGA255 | –55°C < Tc,Tj < 125°C | EQM Grade | |
| EV12DS130AMGC9NB1 | | CCGA255 | –55°C < Tc,Tj < 125°C | Space Grade | |
| EV12DS130AMLG-V | 5962-1522201VXC | LGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |
| EV12DS130AMGS-V | 5962-1522201VYF | CI-CGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |
| EV12DS130AMGC-V | 5962-1522201VZF | CCGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |



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**Table 11-1.** Ordering Information (Continued)

| Part Number | SMD Number | Package | Temperature Range | Screening Level | Comments |
|---|---|---|---|---|---|
| **EV12DS130BG** | | | | | |
| EVX12DS130BGS | | CI-CGA255 | Ambient | Prototype | |
| EV12DS130BGS-EB | | CI-CGA255 | Ambient | Prototype | Evaluation board |
| EVX12DS130BLG | | LGA255 | Ambient | Prototype | |
| EV12DS130BMLG | | LGA255 | –55°C < Tc,Tj < 125°C | Engineering model | Contact Marketing/pending qualification |
| EV12DS130BMLGD/T | | LGA255 | –55°C < Tc,Tj < 125°C | EQM Grade | Contact Marketing/pending qualification |
| EV12DS130BMLG9NB1 | | LGA255 | –55°C < Tc,Tj < 125°C | Space Grade | Contact Marketing/pending qualification |
| EVX12DS130BGC | | CCGA255 | Ambient | Prototype | |
| EV12DS130BMGC | | CCGA255 | –55°C < Tc,Tj < 125°C | Engineering model | Contact Marketing/pending qualification |
| EV12DS130BMGCD/T | | CCGA255 | –55°C < Tc,Tj < 125°C | EQM Grade | Contact Marketing/pending qualification |
| EV12DS130BMGC9NB1 | | CCGA255 | –55°C < Tc,Tj < 125°C | Space Grade | Contact Marketing/pending qualification |
| EV12DS130BMLG-V | 5962-1522202VXC | LGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |
| EV12DS130BMGS-V | 5962-1522202VYF | CI-CGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |
| EV12DS130BMGC-V | 5962-1522202VZF | CCGA255 | –55°C < Tc,Tj < 125°C | QML-V Grade MIL PRF 38535 | |



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## 12. REVISION HISTORY

This table provides revision history for this document.

**Table 12-1.** Revision History

| Rev. No | Date | Substantive Change(s) |
|---|---|---|
| 1080J | September 2016 | Table 11-1, “Ordering Information,” on page 81: Correction of EV12DS130B SMD Numbers 1522201 instead of 1522202 |
| 1080I | August 2016 | Table 11-1, “Ordering Information,” on page 81: Introduction of QML-V grade for EV12DS130B<br>Typo correction |
| 1080H | March 2016 | Introduction of QML-V grade and add EV12DS130AMGC |
| 1080G | December 2014 | Section 5.6 on page 28: OCDS [10] not allowed<br>Introduction and description of EV12DS130B<br>New Section 10. ”Differences between EV12DS130A and EV12DS130B” on page 80<br>Table 3-6, “AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)(2),” on page 10: Limits update<br>Table 3-9, “Coding Table (Theorical values),” on page 15: typo error on lines (RTZ) and (NRTZ)<br>Section 5.1 ”DSP Output Clock” on page 18 updated<br>Section 5.3 ”MODE Function” on page 18: equations updated<br>Section 5.5 ”PSS (Phase Shift Select Function)” on page 26 updated<br>Section 5.9 ”Synchronization functions for multi-DAC operation” on page 31 updated<br>Figure 7-5 on page 42 updated<br>Figure 7-13 on page 46 updated<br>New Section 7.2.3 ”Single tone measurements: typical spectra at 3Gsps” on page 50<br>New Section 8.10 ”Balun Influence” on page 76<br>Table 11-1, “Ordering Information,” on page 81 |
| 1080F | May 2014 | Table 3-3: Change max current ICCD limit (2:1 & 4:1 MUX mode)<br>Table 3-3: Output internal differential resistor is test level 1 & 6<br>Table 3-6: remove minimum limit on \|SFDR\| in 4:1 MUX mode<br>Fs = 3Gsps @ Fout = 1600MHz 0 dBFS (now test level 4)<br>Table 3-6: remove maximum limit on highest spur level in 4:1 MUX mode<br>Fs = 3Gsps @ Fout = 1600MHz 0 dBFS (now test level 4)<br>Table 3-8: provide min & max limits for Input data rate in 2:1 and 4:1 MUX mode.<br>Table 3-8: Delay TDP is renamed TPD. It is a typ value and not a max value<br>Section 4. ”Definition of Terms” on page 16:<br>- TOD definition is replace by TPD/TOD definition for clarification<br>- Typo correction on RTZ and NRTZ term<br>Figure 8-11: modification of power supplies decoupling scheme on VCCA3 and VCCD<br>Typo errors |



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**Table 12-1.** Revision History (Continued)

| Rev. No | Date | Substantive Change(s) |
|---|---|---|
| 1080E | December 2013 | Typo errors correction in formula of Section 5.3 ”MODE Function” on page 18 and Section 5.6 ”Output Clock Division Select Function” on page 28<br>Section 9.3 ”CCGA255 Outline” on page 79 CCGA Outline drawing<br>Table 3-2, “Recommended Conditions of Use,” on page 4: typo errors on note 2: $V_{CCA3} \geq V_{CCD}$<br>Table 3-3, “Electrical Characteristics,” on page 5: typo errors on note 7: $V_{CCA3} \geq V_{CCD}$ |
| 1080D | July 2013 | Typo errors<br>OCDS restrictions<br>HTVF STVF flag application clarification<br>Power sequencing modification. Sync operation clarification.<br>Add LGA and CCGA outline drawing |
| 1080C | July 2012 | Typo errors<br>absolute max rating clarifications<br>addition of pin equivalent schematic description<br>Power sequencing recommendation |
| 1080B | February 2012 | Typo errors<br>Rth adjustement. |
| 1080A | February 2012 | Initial Revision |



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