12-bit 500 Msps ADC
AT84AS001

Datasheet

1. Main Features

- 12-bit Resolution
- 500 Msps Sampling Rate
- Low Clock Latency (Two Clock Cycles)
- 1.1 Vpp Full Scale Analog input Range (Aids in Amplifier Interface)
- AC or DC Coupled Analog Input with External Control
- Constant Input Impedance
- Differential 100Ω PECL/LVDS Compatible Clock Inputs
- LVDS Output Compatibility (100Ω)
- 3-wire Serial Bus Programming Interface
  - 16-bit Data, 3-bit Address
  - Gain (–1.5 dB/+1.2 dB Full-scale) Digital Control
  - Offset Digital Control (±45 LSB)
  - Standby Mode
  - Internal Static Built-In Test (BIT)
- Synchronous Reset Input
- Low Power Consumption: 2.4W
- Power Supply: 5V (Analog), 3.3V (Digital, Output)
- EBGA 192 Package
- Evaluation Board AT84AS001TP-EB

2. Performances

- 1 GHz Full Power Input Bandwidth (–3 dB)
- Band Flatness 0.5 dB (from DC Up to 200 MHz)
- 9.8-bit ENOB (at F_{IN} = 250 MHz)
- Single Tone Performances (–1 dBFS)
  - SFDR = 75 dBc at Fs = 500 Msps, Fin = 250 MHz, –1 dB input level
  - SFDR = 73 dBc at Fs = 500 Msps, Fin = 394 MHz, –1 dB input level
  - SNR = 61 dBc at Fs = 500 Msps, Fin = 250 MHz, –1 dB input level
- Dual Tone Performances (–7 dBFS)
  - IMD3 = –78 dBFS at Fs = 500 Msps, Fin1 = 240 MHz, Fin2 = 250 MHz
- DNL = ±0.8 LSB; INL = ±2 LSB (Typical)
- Low Bit Error Rate (10^{-14}) at Fs = 500 Msps

3. Screening

- Temperature Range:
  - Commercial *C* Grade $0^\circ C < T_{amb} < 70^\circ C$
  - Industrial *V* Grade $-40^\circ C < T_{amb} < 85^\circ C$

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4. Applications

- **Test and Measurement Instrumentation**
- **Radar and Satellite Receiver Subsystems**
- **Wireless and Wired Communications Receivers**
- **Medical Imaging**
- **High-speed Data Acquisition**

5. Description

The AT84AS001 is a high-performance 12-bit 500 Msps ADC featuring low-power consumption and true 12-bit linearity for IF sampling applications. By using its on-chip S/H circuitry and advanced high-speed process technology, it allows conversion of wide-bandwidth signals up to 500 MHz of input frequency at 500 Msps. Its electrical performance is coupled with ease of integration into new or existing designs by such features as AC or DC coupled analog input, differential LVDS compatible output, 3-wire serial interface (gain and offset control, standby mode, Built-In Test), double data rate clock output and synchronous reset input.

6. Specifications

6.1 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Analog positive supply voltage	V_{CCA}		6	V
Digital positive supply voltage	V_{CCD}		3.6	V
Output supply voltage	V_{CCO}		3.6	V
Maximum difference between DV_{CCA} and V_{CCD}	DV_{CCA} to V_{CCD}		±2.5	V
Maximum difference between V_{CCD} and V_{CCO}	V_{CCD} to V_{CCO}		±1.5	V
Analog input voltages (AC) on each singled-ended input	V_{IN} or V_{INN}		±2	V peak
Digital input voltage (3WSI)	V_D		–0.3 to V_{CCO} + 0.3	V
Clock input voltage	V_{CLKI} or V_{CLKIN}		–0.3 to V_{CCD} + 0.3	V
Maximum difference between V_{CLKI} and V_{CLKIN}	V_{CLKI} - V_{CLKIN}		–2 to 2	V
RESET input voltage	V_{RESET} or V_{RESETN}		–0.3 to V_{CCD} + 0.3	V
Maximum difference between V_{RESET} and V_{RESETN}	V_{RESET} - V_{RESETN}		–2 to 2	V
Maximum junction temperature	T_J		125	°C
Storage temperature	T_{stg}		–65 to 150	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating might affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

6.2 Recommended Conditions of Use

Table 6-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended	Unit
Analog supply voltage	V_{CCA}		5	V
Digital supply voltage	V_{CCD}		3.3	V
Output supply voltage	V_{CCO}		2.5 (3.3 allowed)	V
Differential analog input voltage (full-scale)	V_{IN},V_{INN}		1.1	Vpp
Differential clock input level	V_{INCLK}, V_{INCLKN}		3	dBm
Operating temperature range	T_{amb}	Commercial *C* grade Industrial *V* grade	0° C < T_{amb} < 70° C –40° C < T_{amb}< 85° C	° C
Maximum operating junction temperature	T_J		110	° C

6.3 Electrical Characteristics

- V_{CCA} = 5V, V_{CCD} = 3.3V; V_{CCO} = 2.5V
- V_{IN} –V_{INN} = 1.1 Vpp full-scale differential input, digital outputs LVDS (100Ω)
- T_{amb} (typical) = 25° C unless otherwise specified

Table 6-3. Electrical Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Resolution				12		Bit
Power Requirements						
Power supply voltage Analog Digital Output and 3-wire serial interface	1	 V_{CCA} V_{CCD} V_{CCO}	 4.75 3.15 2.2	 5 3.3 2.5	 5.25 3.45 3.45	V
Power supply current Analog Digital Output and 3-wire serial interface	1	 I_{CCA} I_{CCD} I_{CCO}		 340 150 75	 380 180 90	mA
Power supply current (full standby mode) Analog Digital Output and 3-wire serial interface	1	 I_{CCA} I_{CCD} I_{CCO}		 26 15 20	 35 25 30	mA
Power dissipation Full power Standby	1	 P_D		 2.4 235	 2.6 300	 W mW

Table 6-3. Electrical Characteristics (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Analog Input						
Input voltage range (differential mode only) to obtain full scale with no gain adjust	1	V_{IN} V_{INN}		±275 ±275		mV
Input common mode	1	V_{IN} V_{INN} V_{CSH}		2.15		V
Analog input power capacitance (die)	4	C_{IN}			2	pF
Input resistance	1	R_{IN}		2000		Ω
Clock Input						
Logic compatibility			PECL/ECL/LVDS (providing AC coupling)			
Clock Input power level (50Ω single-ended or 100Ω differential)	4	P_{CLK}	–4		10	dBm
Clock Input common mode voltage	4			2 x V_{CCD}/3		V
Clock Input swing (differential mode on each clock input)	4	$V_{CLK,}$ V_{CLKN}		±320		mV
Clock input swing (single-ended mode with C_{LKN} 50Ω to GND)	4	V_{CLK} , V_{CLKN}		±450		mV
Clock input capacitance	4	C_{CLK}			2	pF
Clock input resistance Differential	4	R_{CLK}		100		Ω
Digital Inputs (Serial Interface)						
Maximum clock frequency (sclk)	4		50			MHz
Logic compatibility			CMOS (V_{CCO} = 2.5V)			
Control input voltages Logic low Logic high	1	 V_{IL} V_{IH}	 –0.3 V_{CCO} – 0.3	 0 2.5	 0.3 V_{CCO} +0.3	 V
Input leakage current	1	I_{IL} I_{IH}		±10		µA
Digital Outputs and CLKO						
Logic compatibility			LVDS			
Output levels (LVDS) Logic low Logic high Swing Common mode	1	 V_{OL} V_{OH} $V_{OH} – V_{OL}$ V_{OCM}	 0.925 1.25 250 1.125	 1.1 1.4 300 1.25	 1.25 1.375 400 1.375	 V V mV V
Output impedance (LVDS)	4	R_O	30	50	70	Ω
Output current (shorted output) (LVDS)	4				12	mA
Output current (grounded output) (LVDS)	4				30	mA
Output level drift with temperature (LVDS)	4			–1.1		mV/°C

Table 6-3. Electrical Characteristics (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Reset Input						
Logic compatibility for RESET input				PECL/LVDS		
2.5V PECL differential logical level Logic *0* voltage Logic *1* voltage Swing (peak-to-peak)	4	 V_{IL} V_{IH} $\|V_{IL} - V_{IH}\|$	 0.5 1.3	 0.68 1.48 0.8	 1 1.9	 V V V
3.3V PECL differential logical level Logic *0* voltage Logic *1* voltage Swing (peak-to-peak)	4	 V_{IL} V_{IH} $\|V_{IL} - V_{IH}\|$	 1.3 2	 1.48 2.28 0.8	 1.9 2.6	 V V V
LVDS differential logical level Logic *0* voltage Logic *1* voltage Swing (peak-to-peak)	1	 V_{IL} V_{IH} $\|V_{IL} - V_{IH}\|$	 0.925 1.3	 1.1 1.4 0.3	 1.2 1.475	 V V V
Differential logical levels compatibility Logic *0* voltage Logic *1* voltage Swing (peak-to-peak)	4	 V_{IL} V_{IH} $\|V_{IL} - V_{IH}\|$	 0 1.3 0.2		 V_{CCD} –0.1 V_{CCD} +0.1 V_{CCD} +0.1	 V V V

Table 6-4. DC Accuracy

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
DC Accuracy						
No missing code	1		Guaranteed over specified temperature range			
Differential non-linearity (no missing code guaranteed)	1	DNL		0.8		LSB
Integral non-linearity	1	INL		± 2		LSB
Amplitude error (part-to-part) for output code = 4096 (FS = input full-scale)	1				±5	%FS
Gain error drift vs.V_{CCA}	1			10		LSB/V
Gain error drift vs.temperature	4			20		mLSB/°C
Input offset code	1			2048		LSB
Input offset code drift over temperature range	4			±4		LSB

Table 6-5. AC Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Characteristics						
Full power input bandwidth (–3 dB)	1	FPBW		>1.0		GHz
Gain flatness (±0.5 dB)	4	GF		200		MHZ
Analog Input equivalent Thermal noise with 1.1 Vpp input level	4	Vnoise		1		LSB rms
Input voltage standing wave ratio (DC to 300 MHz)	4	VSWR		1.2		
AC Performance						
Differential input (–1dBFS analog input level) and clock mode, 60/40 clock duty cycle (CLKI,CLKIN) Internal DC adjustment = 50 mV						
Signal-to-noise Ratio						
Fs = 500 Msps Fin = 10 MHz	1		61	63		
Fs = 500 Msps Fin = 197 MHz	1		59.5	61.5		
Fs = 500 Msps Fin = 250 MHz	4	SNR	59	61		dB
Fs = 500 Msps Fin = 394 MHz	1			60		
Fs = 500 Msps Fin = 498 MHz	4			58.5		
Effective Number of Bits						
Fs = 500 Msps Fin = 10 MHz	1		9.8	10.1		
Fs = 500 Msps Fin = 197 MHz	1		9.7	9.85		
Fs = 500 Msps Fin = 250 MHz	4	ENOB	9.65	9.8		Bits
Fs = 500 Msps Fin = 394 MHz	1			9.5		
Fs = 500 Msps Fin = 498 MHz	4			9.3		
Spurious Free Dynamic Range						
Fs = 500 Msps Fin = 10 MHz	1		67	75		
Fs = 500 Msps Fin = 197 MHz	1		67	75		
Fs = 500 Msps Fin = 250 MHz	4	|SFDR|	67	75		dBc
Fs = 500 Msps Fin = 394 MHz	1		65	73		
Fs = 500 Msps Fin = 498 MHz	4			71		
Total Harmonic Distortion						
Fs = 500 Msps Fin = 10 MHz	1			67		
Fs = 500 Msps Fin = 197 MHz	1			66		
Fs = 500 Msps Fin = 250 MHz	4	|THD|		65		dB
Fs = 500 Msps Fin = 394 MHz	1			65		
Fs = 500 Msps Fin = 498 MHz	4			64		
Two-tone Inter-Modulation Distortion Fs = 500 Msps Fin1 = 240 MHz, Fin2 = 250 MHz (–7 dBFS each tone)	1	IMD3	-68	-78		dBFS

Note: AC performance is measured with a test bench of 350 Fs rms equivalent jitter (including external jitter noise of 200 Fs rms on $V_{IN.}$)

Table 6-6. Timing Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
T**ransient Performance**						
Bit error rate	4	BER		1e–14		Error /sample
ADC step response rise/fall time (10% to 90%)	4			400		ps
Switching Performance and Characteristics						
Maximum clock frequency	1	Fs MAX	500			Msps
Minimum clock frequency (operating)	4	Fs MIN			2	Msps
Minimum clock frequency (testing)	4	Fs MIN	1			Ksps
Minimum clock pulse width (high)	4	TC1	0.9	1.25		ns
Minimum clock pulse width (low)	4	TC2	0.9	1.25		ns
Aperture delay	4	TA		1		ns
Aperture uncertainty (Fc = 500 Msps) ADC only	4	Jitter		80		fs rms
Output fall time for data (20% to 80%) with 10 pF load	4	TF		0.6	1	ns
Output rise/fall time for CLKO (20% to 80%) with 10 pF load	4	TR/TF		0.6	1	ns
CLKO jitter	4				± 50	ps
Data output delay (Fc = 500 Msps)	4	TOD		2.9		ns
Data ready output delay	4	TDR		3.1		ns
	4	|TOD –TDR|		200		ps
Output data to data ready propagation delay (Fc = 500 Msps)	4	TD1		1.05		ns
Data ready to output data propagation delay (Fc = 500 Msps)	4	TD2		0.95		ns
Output data pipeline delay	4	TPD		2		Clock cycles
Data ready reset delay	4	TRDR		8.2		ns
RESETN recommended pulse width	4		4			ns
RESETN to CLK (setup)	4	Tsu	50			ps
CLK to RESETN (hold)	4	Thold	50			ps
Switching Performance for Standby Mode						
Time ON to OFF	4	Toff		550		ns
Time OFF to ON	4	Ton		620		ns

Note: The switching performance and characteristics are given for an output load of 10 pF in parallel to 50Ω

6.4 Digital Output Coding (Nominal Setting)

Differential Analog input	Voltage level	Digital output Binary
+550 mV	Positive full-scale +1/2 LSB	1 1 1 1.. 1 1 1 1
+549,75 mV	Positive full-scale –1/2 LSB	1 1 1 1.. 1 1 1 0
+0.245 mV	Bipolar zero + 1/2 LSB	1 0 0 0.. 0 0 0 0
–0.245 mV	Bipolar zero –1/2 LSB	0 1 1 1.. 1 1 1 1
–549,75 mV	Negative full-scale +1/2 LSB	0 0 0 0.. 0 0 0 1
–550 mV	Negative full-scale –1/2 LSB	0 0 0 0.. 0 0 0 0

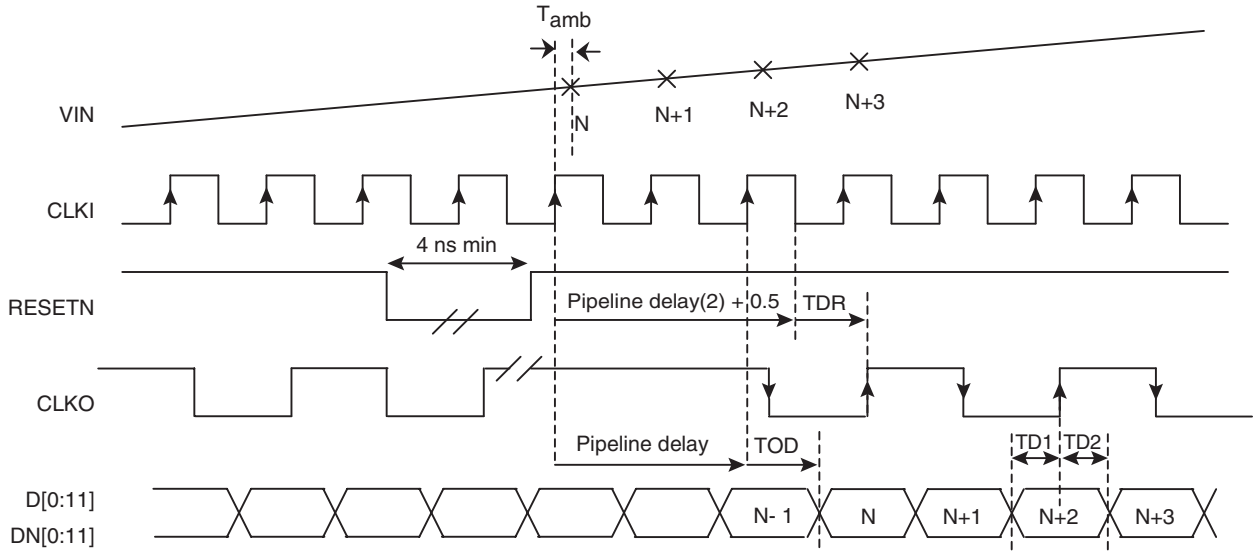
6.5 Timing Diagrams

The following timing diagrams are given for a clock input frequency of 500 Msps.

6.5.1 Outputs Timing

Each edge of the data ready output clock (CLKO) corresponds to a valid data.

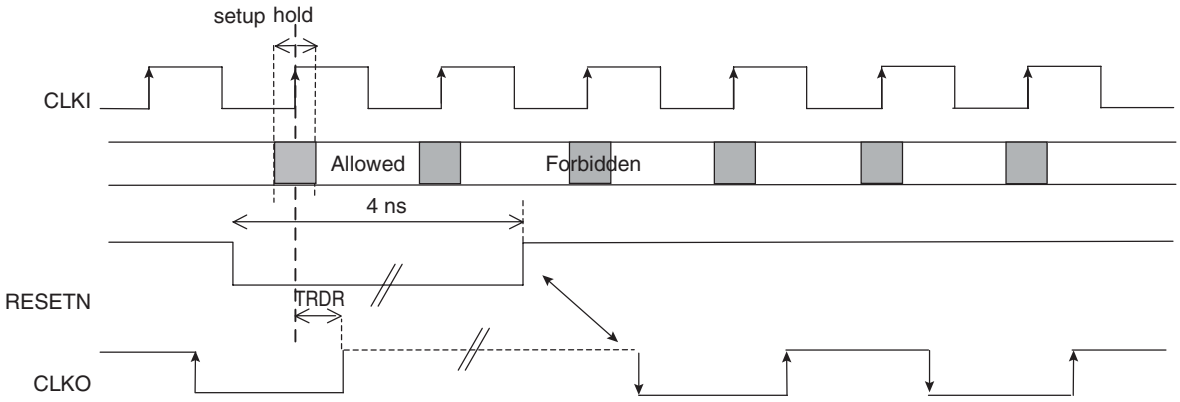
Figure 6-1. Timing Diagram



Note: The rising edge and the falling edges of the differential data ready signal occur in the middle of the output data valid window.

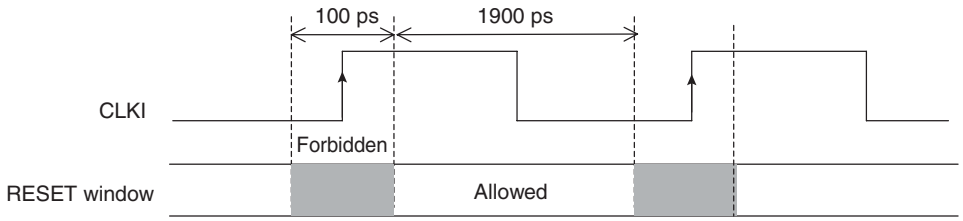
6.5.2 ADC Reset Timing

Figure 6-2. RESETN

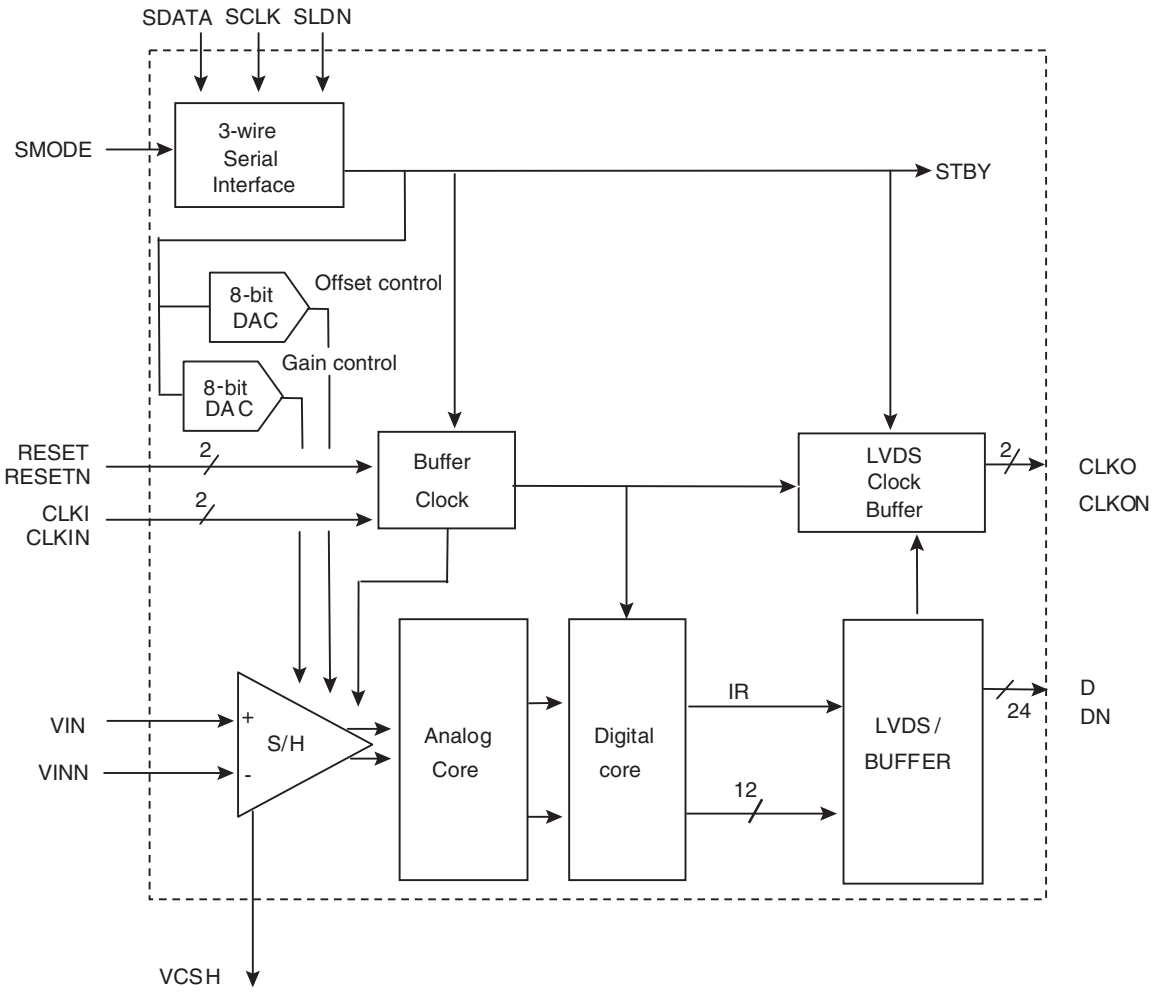


Note: It is recommended to apply the reset with respect to the input clock CLKI falling edge.

Figure 6-3. RESET Allowed and Forbidden Zones



7. Block Diagram



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8. Typical Characteristics

Figure 8-1. SFDR Performance versus Fin at Fs = 500 Msps (–1 dBFS Input Signal)

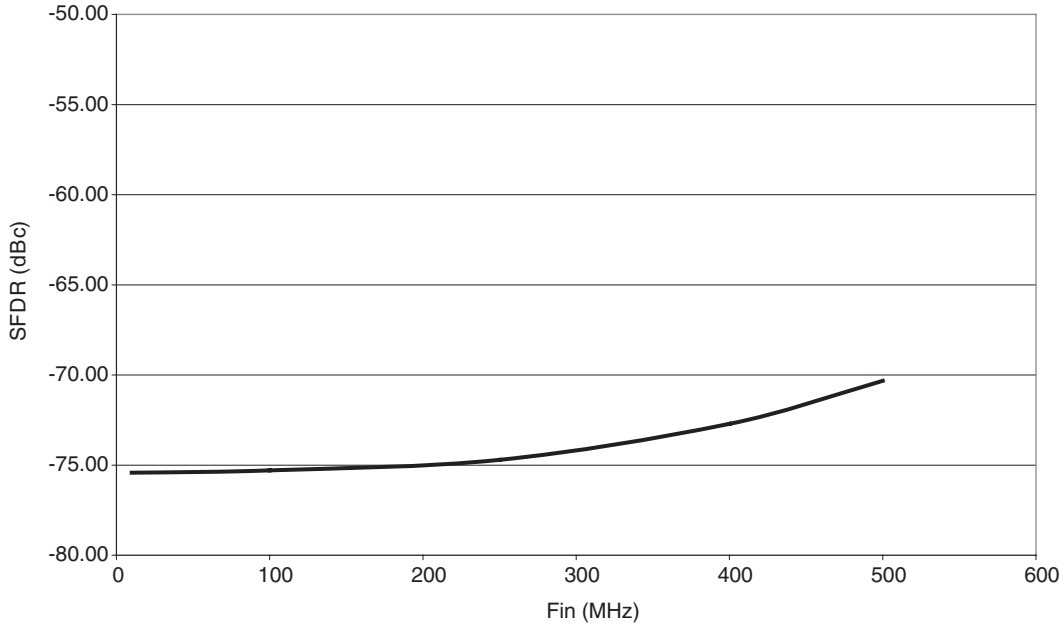


Figure 8-2. Single-tone Spectrum in First Nyqusit, Fs = 500 Msps, Fin = 248 MHz , –1 dBFS Input Signal

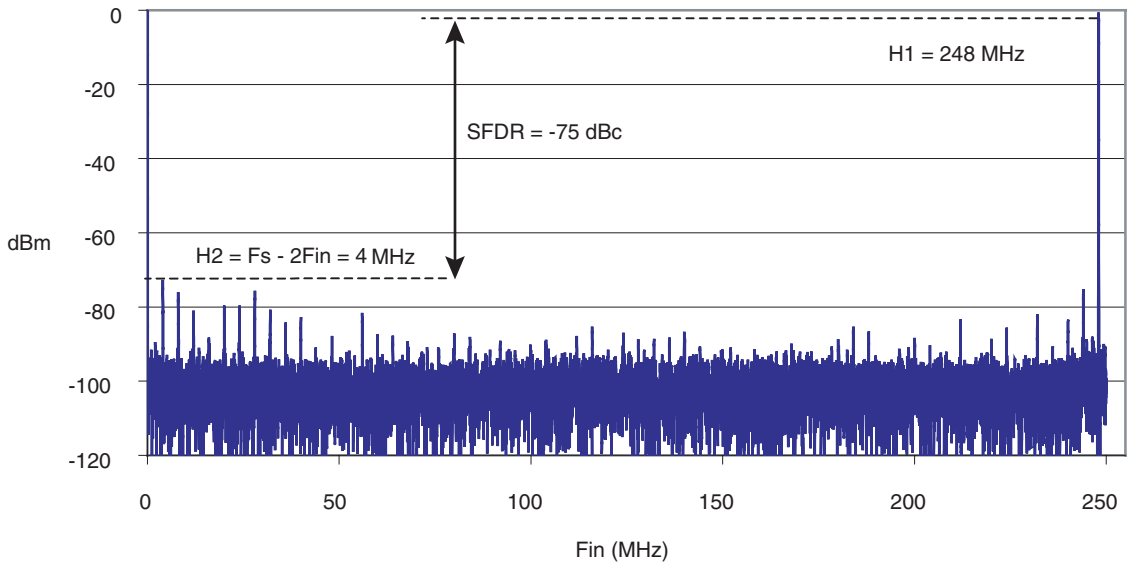


Figure 8-3. Single-tone Spectrum In Second Nyqusit, Fs = 500 Msps, Fin = 498 MHz, –1 dBFS Input

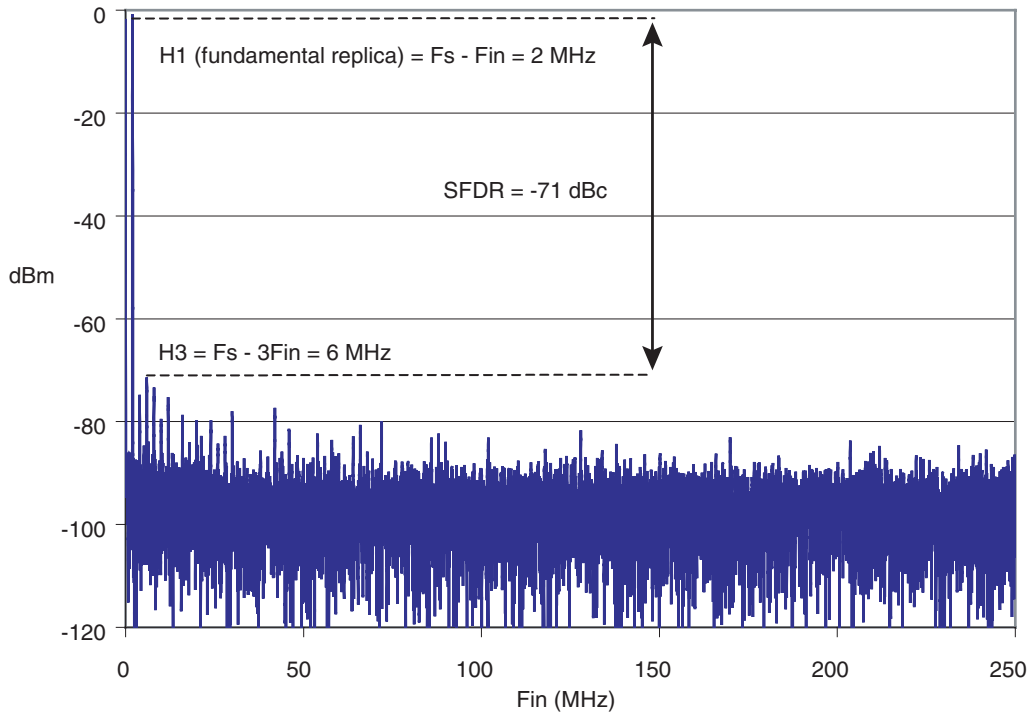


Figure 8-4. Dual tone spectrum in first Nyqusit (IMD3) Fs = 500 Msps, Fin1 = 197 MHz, Fin2 = 203 MHz, -7 dBFS input signal

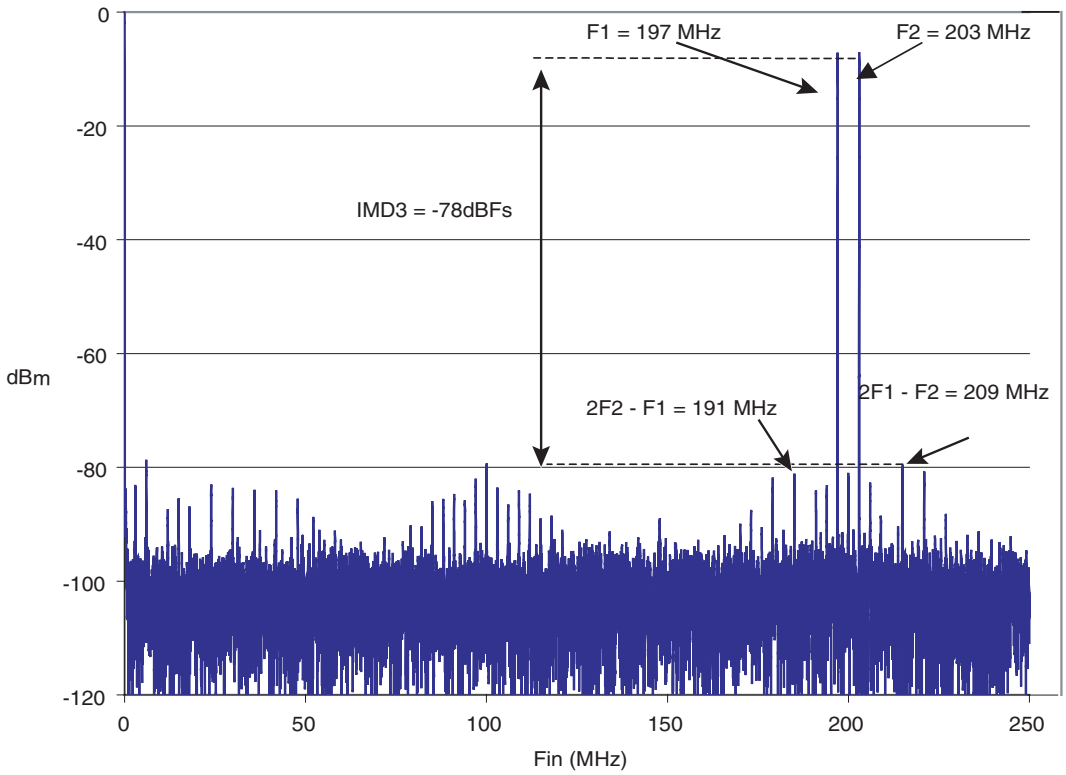


Figure 8-5. DNL

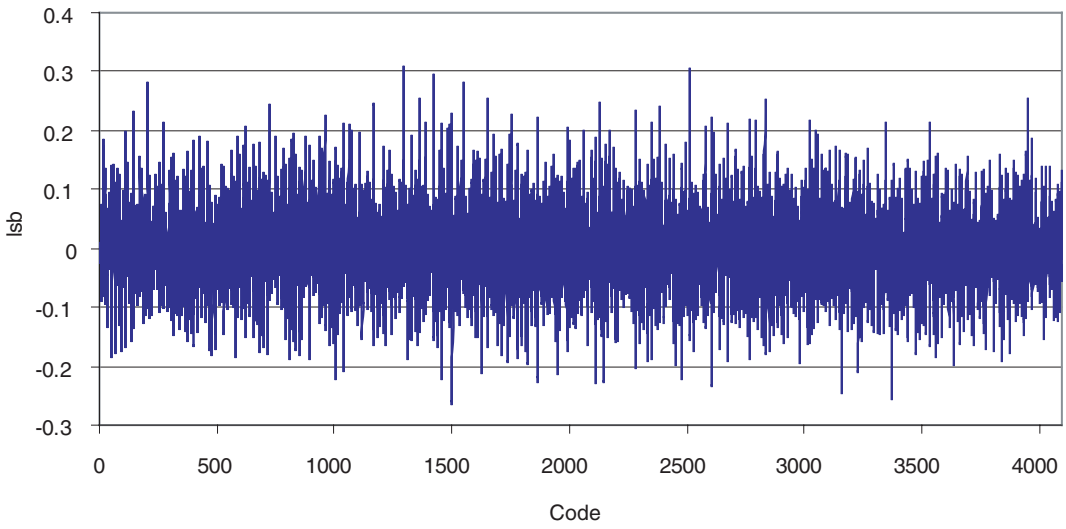


Figure 8-6. INL

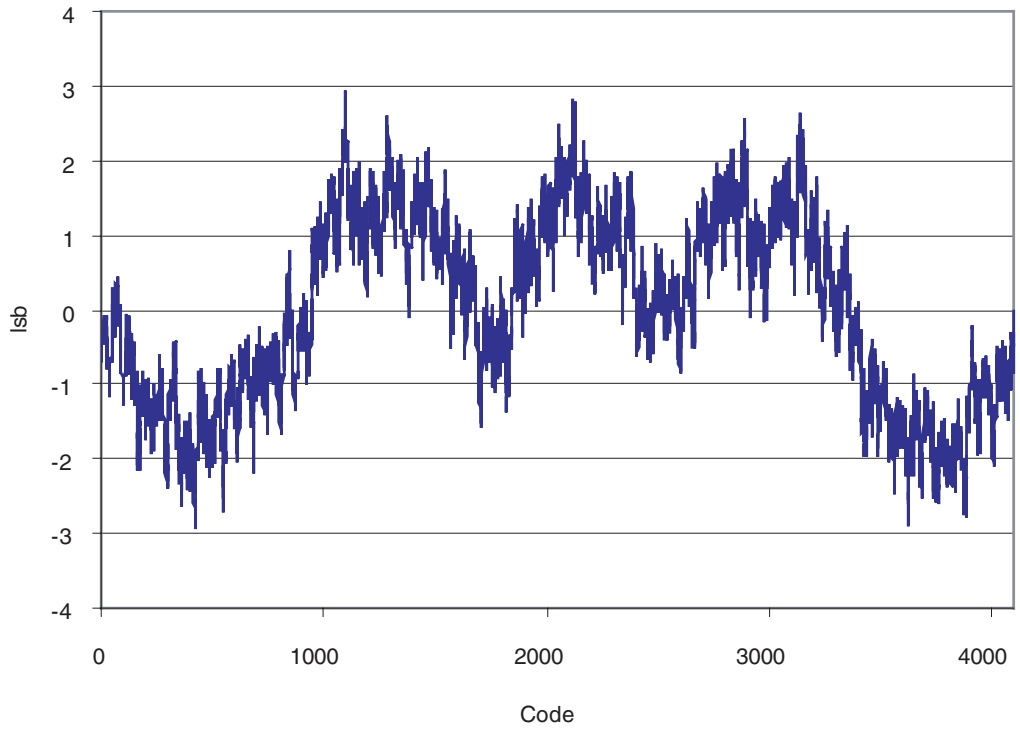


Figure 8-7. Noise Histogram

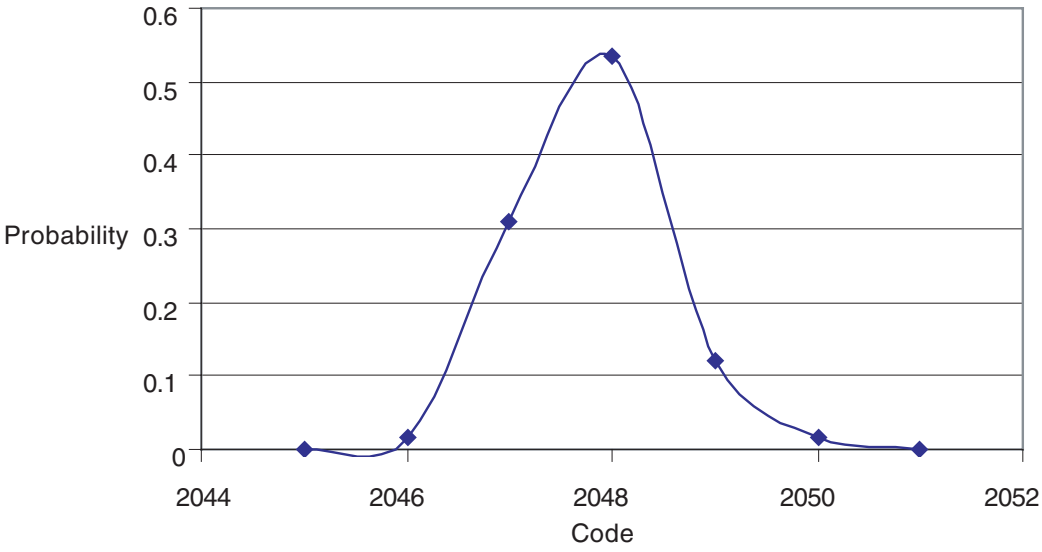


Figure 8-8. SFDR Performance versus Junction Temperature, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS Input Signal

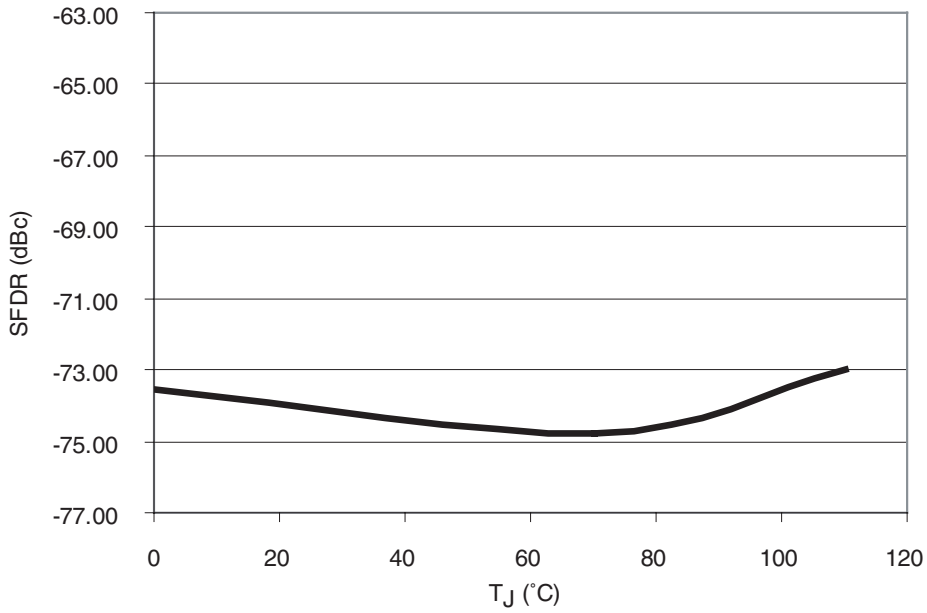
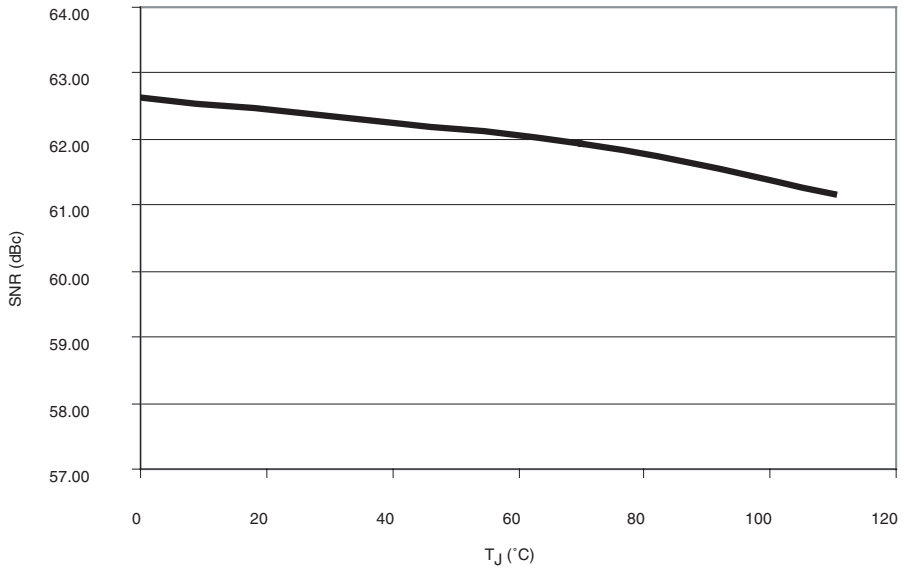


Figure 8-9. SNR Performance versus Junction Temperature, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS Input Signal



Note: SNR is measured with test bench of 350 Fs rms equivalent jitter.

Figure 8-10. SFDR Performance versus Analog Input Power, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS Input Signal

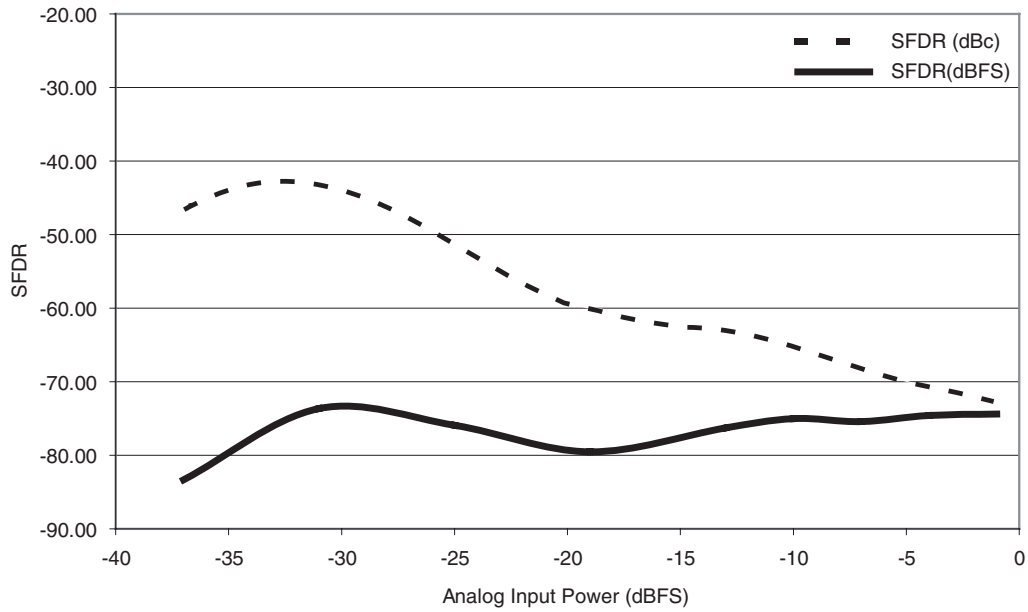


Figure 8-11. SNR Performance versus Clock Input Level, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS input signal

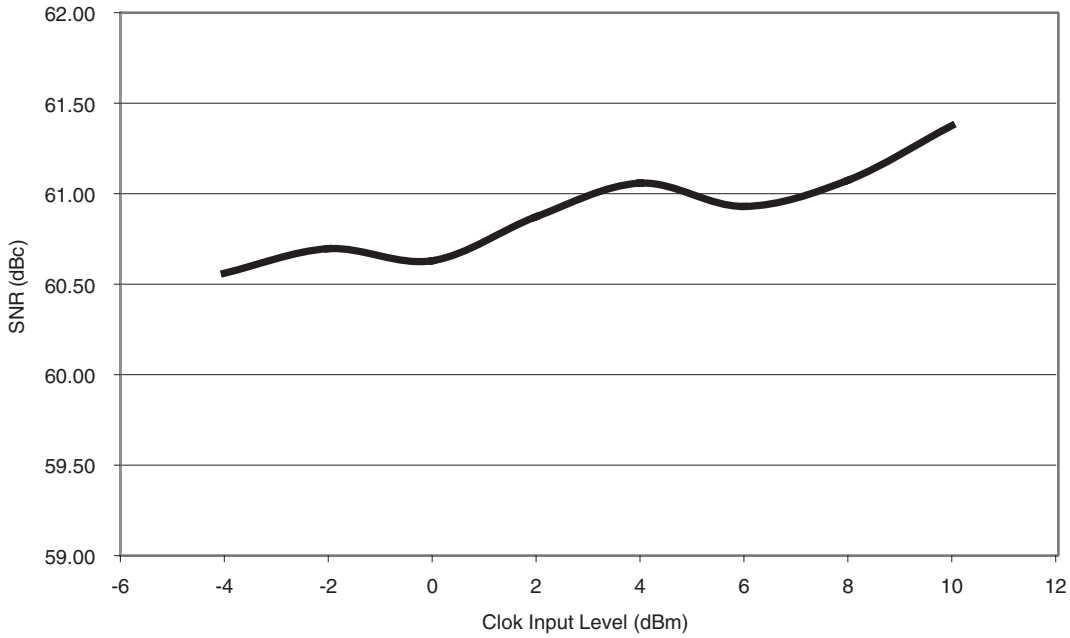


Figure 8-12. SFDR Performance versus Control Gain, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS Input Signal

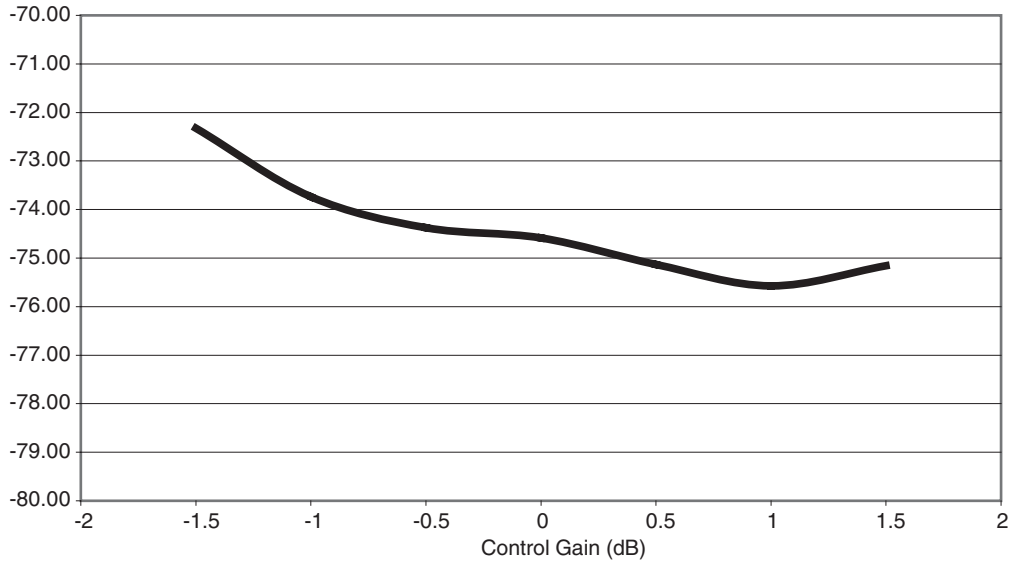
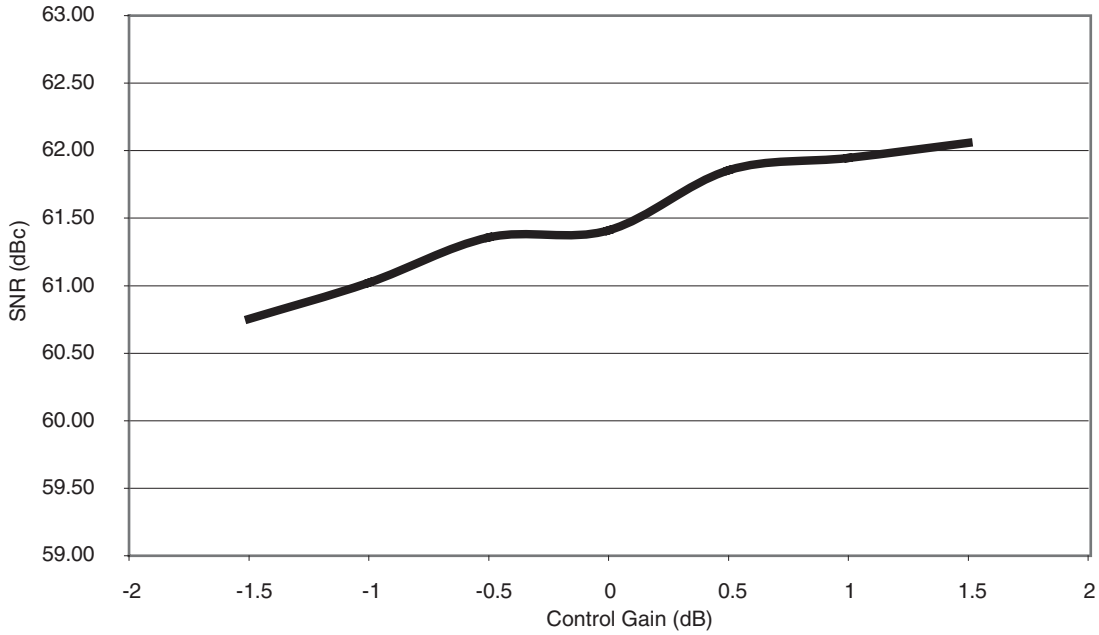


Figure 8-13. SNR performance versus Control Gain, Fs = 500 Msps, Fin = 248 MHz, –1 dBFS Input Signal



9. Functional Description

The AT84AS001 is a monolithic 12-bit 500 Msps ADC.

The circuit includes an on-chip sample and hold (S/H), and a 12-bit analog to digital converter core.

The output data are LVDS (100Ω) compliant.

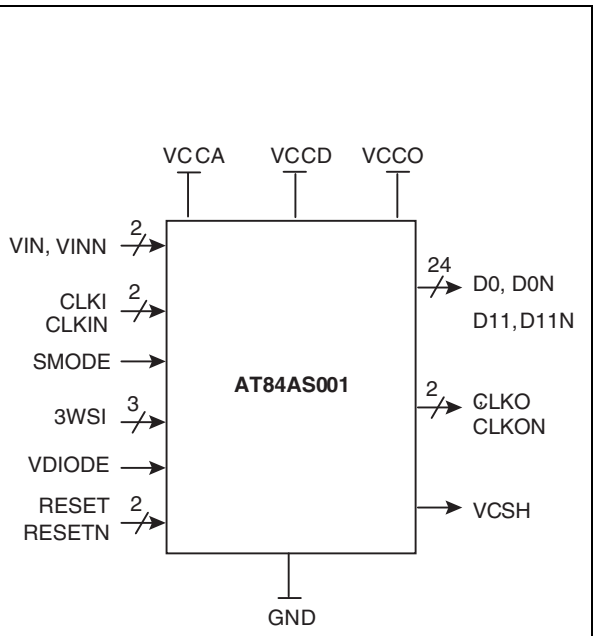
A 3-wire serial interface (3-bit Address, 16-bit data) is included to provide several adjustments and controls:

- Gain: –1.5 dB/ +1.2 dB full-scale digital control (8-bit-control)
- Offset: ±45 LSB digital control (8-bit control)
- Standby mode for power save

The AT84AS001 features a full power input bandwidth of more than 1.0 GHz.

Table 9-1. Functional Description

Name	Function
V_{CCA}	Positive analog power supply 5V
V_{CCD}	Positive digital power supply 3.3V
V_{CCO}	Positive output power supply 2.5V or 3.3V
GND	Ground
VIN, VINN	Differential analog inputs
CLKI, CLKIN	Differential clock inputs
CLKO, CLKON	Differential data ready output
<D0:D11>	Positive output data mode LVDS
<D0N:D11N>	Negative output data mode LVDS
RESET, RESETN	Synchronous reset input signal
VDIODE	Diode for die junction temperature monitoring
3WSI	3-wire serial bus interface
VCSH	Common sample and hold voltage
SMODE	3-wire serial bus interface selection

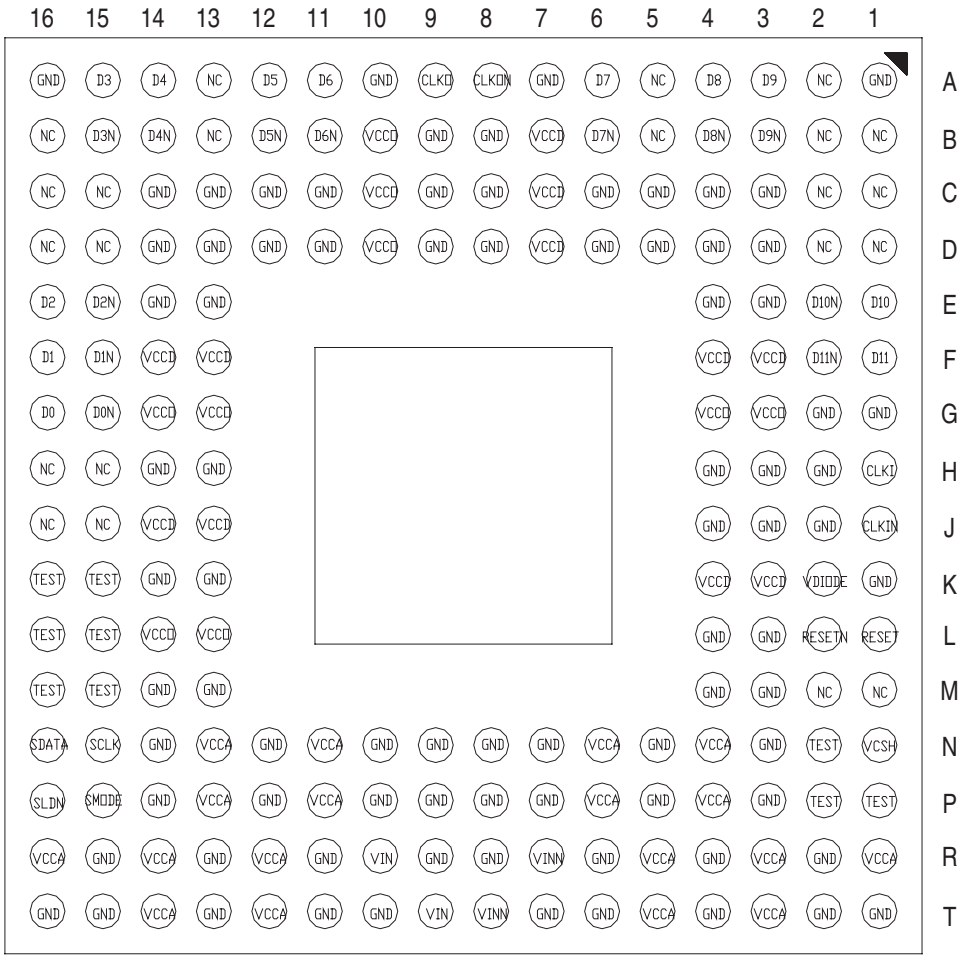


10. AT84AS001 Pinout

Table 10-1. Pinout Table

Pin Number	Symbol	Function
Power Supplies		
A1, A7, A10, A16, B8, B9, C3, C4, C5, C6, C8, C9, C11, C12, C13, C14, D3, D4, D5, D6, D8, D9, D11, D12, D13, D14, E3, E4, E13, E14, G1, G2, H2, H3, H4, H13, H14, J2, J3, J4, K1, K13, K14, L3, L4, M3, M4, M13, M14, N3, N5, N7, N8, N9, N10, N12, N14, P3, P5, P7, P8, P9, P10, P12, P14, R2, R4, R6, R8, R9, R11, R13, R15, T1, T2, T4, T6, T7, T10, T11, T13, T15, T16	GND	Ground
N4, N6, N11, N13, P4, P6, P11, P13, R1, R3, R5, R12, R14, R16, T3, T5, T12, T14	V_{CCA}	Analog power supply 5V
B7, C7, D7, F3, F4, F13, F14, J13, J14, K3, K4	V_{CCD}	Digital power supply 3.3V
B10, C10, D10, G3, G4, G13, G14, L13, L14	V_{CCO}	Output and 3WSI power supply 3.3V or 2.5V
Inputs		
H1, J1	CLKI, CLKIN	Input clock
T9	VIN	In-phase analog input (signal)
T8	VINN	Out-of-phase analog input (signal)
R10	VIN	In-phase analog input (50Ω reverse termination)
R7	VINN	Out-of-phase analog input (50Ω reverse termination)
Outputs		
G16, F16, E16, A15, A14, A12, A11, A6, A4, A3, E1, F1	D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11	In-phase digital output data (D11 is the MSB)
G15, F15, E15, B15, B14, B12, B11, B6, B4, B3, E2, F2	D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N, D10N, D11N	Out-of-phase digital output data (D11N is the MSB)
A9, A8	CLKO, CLKON	Output clock
N1	VCSH	Input common mode
Functions Inputs		
L1, L2	RESET, RESETN	Differential synchronous RESET signal
K2	VDIODE	Diode for die junction temperature monitoring
P15	SMODE	Selection bit for 3WSI (SMODE = 1) or normal mode (SMODE = 0)
P16	SLDN	Beginning and end of register line for 3WSI
N16	SDATA	Input data for 3WSI
N15	SCLK	Input clock for 3WSI
Other		
A2, A5, A13, B1, B2, B5, B13, B16, C1, C2, C15, C16, D1, D2, D15, D16, H15, H16, J15, J16, M1, M2	NC	Non-connected pins These pins can be used as thermal pads when connected to ground
K15, K16, L15, L16, M15, M16, N2, P1, P2	TEST	e2v internal test pins They must be left unconnected (floating)

Figure 10-1. Pinout Diagram (Bottom View)



11. Test and Control Features

11.1 3- wire Serial Interface Control Setting

Table 11-1. 3-Wire Serial Interface Control Setting

SMODE =1 (2.5V)	3-wire serial bus interface activated
SMODE = 0 (0V) *SMODE pin* can be used as a Reset pin for serial interface registers initialization	3-wire serial bus interface inactivated nominal settings (reset values): 0 dB gain; 0 Offset BIT OFF ISA = 0 ps No Standby Internal DC adjustment = 0 mV Duty cycle = 50/50 T/H transparent mode OFF

Note: To achieve high performance we recommend a duty cycle of 60/40 and internal DC adjustment = 50 mV

11.1.1 3WSI Timing Description

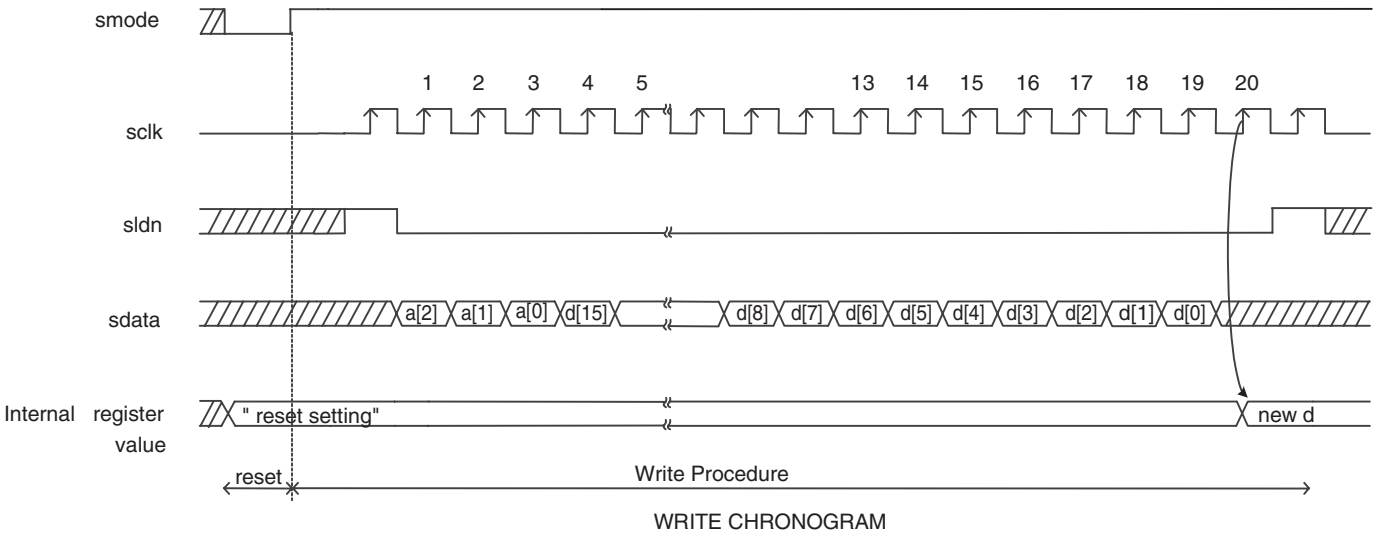
The 3WSI is a synchronous write only serial interface made of 3 wires:

- *sclk*: serial clock input
- *sldn*: serial load enable input
- *sdata*: serial data input

The 3WSI gives a write only access to up to 8 different internal registers of up to 16 bits each. The input format is fixed with always 3 bits of register address followed by always16 bits of data. Data and address are entered MSB first.

The write procedure is fully synchronous with clock rising edge of *sclk* and described in the write chronogram, Figure 11-1 on page 22. *sldn* and *sdata* are sampled on each rising clock edge of *sclk* (clock cycle). *sdn* must be set at *1* when no write procedure is done.

Figure 11-1. Write Procedure



A minimum of one clock rising edge (clock cycle) with *sldn* at *1* is required for a correct start of the write procedure. A write starts on the first clock cycle with *sldn* at *0*. *sldn* must stay at *0* during the complete write procedure. In the first three clock cycles with *sldn* at *0*, 3 bits of register address from MSB (a[2]) to LSB (a[0]) are entered.

In the next 16 clock cycles with *sldn* at *0*, 16 bits of data from MSB (d[15]) to LSB (d[0]) are entered. An additional clock cycle with *sldn* at *0* is required for parallel transfer of the serial data d[15:0] in the register addressed with address a[2:0]. This gives 20 clock cycles with *sldn* at *0* for a normal write procedure.

A minimum of one clock cycle with *sldn* returned at *1* is requested to close the write procedure and before the interface is ready for a new write procedure. Any clock cycle with *sldn* at *1* before the write procedure is completed interrupts this procedure at no data transfer to internal registers is done.

Additional clock cycles with *sldn* at *0* after the parallel data transfer to the register (done at 20th consecutive clock cycle with *sldn* at *0*) does not affect the write procedure and is ignored. It is possible to have only one clock cycle with *sldn* at *1* between two following write procedures. 16 bits of data must always be entered even if the internal addressed register has less than 16 bits. Unused bits (usually MSB's) are ignored.

Notes:
1. SMODE signal has to be toggled once at ADC power-up.
2. Resetting registers:
   Even when 3WSI is used the *SMODE* pin can be used as a reset pin for serial interface registers initialization.
3. The RESETN signal is a timing reset that has no influence on register settings.

Timings related to the 3-wire serial interface are given in Table 11-2 on page 23. Definition of these timings are shown in the timing chronogram Figure 11-2 on page 23.

Table 11-2. 3-Wire Serial Interface Timings

Name	Parameter	Min	Typ	Max	Unit
Tsclk	Period of sclk	20			ns
Twsclk	High or low time of sclk	5			ns
Tssldn	Setup time of sldn before rising edge of sclk	4			ns
Thsldn	Hold time of sldn after rising edge of sclk	2			ns
Tssdata	Setup time of sdata before rising edge of sclk	4			ns
Thsdata	Hold time of sdata after rising edge of sclk	2			ns
Twlsmode	Minimum low pulse width of smode	5			ns
Tdsmode	Minimum delay between an edge of smode and the rising edge of sclk	10			ns

11.1.2 3WSI: Address and Data Description

This 3-wire bus is activated with the control bit SMODE equal to one (1).

The length of the word is 18 bits: 16 for the data and 3 for the address. The maximum clock frequency for SCLK is 54 MHz.

Table 11-3. Address and Data Description

Address	Settings	Default Value
000	Control register: Standby T/H transparent mode BIT Mode	0x40 No Standby T/H Transparent mode OFF BIT mode OFF
001	Analog Gain Adjustment	0x800 dB Gain
010	Offset Adjustment	0x800 LSB Offset
011	Not Used	
100	Internal Settling Adjustment	0x1410 0mV DC adjustment 0 ps ISA 50/50 Duty cycle
101	BIT (Built-In Test)	0x00

Table 11-4. General Control Register Mapping (Address 000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Unused								BIT	Unused		0	T/H	0	0	STBY

Table 11-5. General Control Register Description (Address 000)

Bit Label	Value	Description
STBY	0	No standby
	1	Full standby(Note:)
T/H	0	Transparent T/H Mode OFF
	1	Transparent T/H Mode ON
BIT	0	BIT mode OFF
	1	BIT mode ON

Note: When Standby mode is activated, the registers values are unchanged.
When leaving Standby mode, it is recommended to apply a RESET via RESET, RESETN signal in order to ensure the synchronization of CLKO.

11.1.3 Analog Gain Adjustment (Address 001)

It is possible to adjust the analog gain of the ADC by –1.5 dB to +1.2 dB by 256 steps.

The default and reset value of the analog gain register (address 001) is 10000000 (0x80) and corresponds to a default gain adjustment of 0 dB (that is, the analog gain of the ADC corresponds to the intrinsic gain of the device).

Table 11-6. Gain Adjustment Register Mapping (Address 001)

Setting for Address: 001	D15-D8	D7-D0
Gain adjustment	Unused	Gain <7:0>

Table 11-7. Gain Adjustment Register Description (Address 001)

Bit Label	Value	Description
Gain <7.0>	00000000	–1.5 dB (variation on the input scale)
	10000000	0 dB (reset value)
	11111111	+1.2 dB (variation on the input scale)

11.1.4 Offset Adjustment

It is possible to adjust the offset of the ADC by 90 LSB (± 45 LSB) by 256 steps of 0.35 LSB.

The default and reset value of the offset register (address 010) is 10000000 (0x80) and corresponds to a default offset adjustment of 0 LSB (that is, the offset of the ADC corresponds to the intrinsic offset of the device).

Table 11-8. Offset Adjustment Register (Address 010)

Setting for Address: 001	D15-D8	D7-D0
Offset adjustment	Unused	Offset <7:0>

Table 11-9. Offset Adjustment Register Description (Address 001)

Bit Label	Value	Description
Gain <7.0>	01111111	+45 LSB
	00000001	+0.35 LSB
	10000000	0 LSB (Reset Value)
	10000001	–0.35 LSB
	11111111	–45 LSB

11.1.5 Internal Settling and DC Adjustments

Internal adjustments are provided to optimize the ADC performance:

– DC adjustment (DC internal offset adjustment)

– ISA (Internal Settling Adjustment)

– Duty Cycle (for Track and Hold mode)

Table 11-10. Internal adjustments register Mapping (Address 100)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Duty<2:0>			Unused						ISA<1:0>		DC<4:0>				

Table 11-11. Internal Adjustments Register Description (Address 100)

Bit Label	Value	Description
DC<4:0>	00000	–100 mV Internal DC offset adjustment
	10000	0mV Internal DC offset adjustment (Reset value)
	11111	93.5 mV Internal DC offset adjustment
ISA<1:0>	00	0 ps ISA
	01	50 ps ISA
	10	100 ps ISA
	11	150 ps ISA
Duty<2:0>	000	50/50 Internal Duty cycle (50% Track, 50% Hold)
	010	40/60 Internal Duty Cycle (40% Track, 60% Hold)

11.1.6 Built-In Test (Address 101)

A Built-In Test (BIT) function is available to allow the user to test rapidly the device I/O by applying a defined static pattern to the ADC. This function is controlled via the 3-wire bus interface at the address 000.

The BIT is active when Data7 = 0 at address 000.

The BIT is inactive when Data7 = 1 at address 000.

When the BIT is activated (Data7 = 1 at address 000), the user can write any 12-bit pattern by defining Data0 to Data11 bits at address 101.

Table 11-12.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Unused				BIT<11:0>											

The ADC will then output a 12-bit pattern equal to Data0...Data11 on D0...D11 and to NOT (Data0…Data11) on D0N…D11N.

An example is given below.

Example:

Address = 101

Data =

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Then, one should obtain 101010101010 on D0…D11 and 010101010101 on D0N…D11N.

11.1.7 Die Junction Temperature Monitoring Function

For operation in the extended temperature range, forced convection is required, to maintain the device junction temperature below the specified maximum value (T_J max = 125°C).

A die junction temperature measurement setting is available, for max junction temperature monitoring (hot point measurement).

The measurement method consists in forcing a 1mA current into a diode mounted transistor.

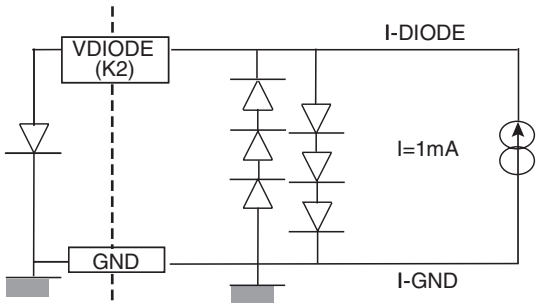
Caution:

Respect the current source polarity.

In all case, make sure that the maximum voltage compliance of the current source is limited to maximum 1 Volt or use resistor mounted in series with the current source to avoid damages, which may occur to the transistor device (this may occur for instance if current source is connected in reverse).

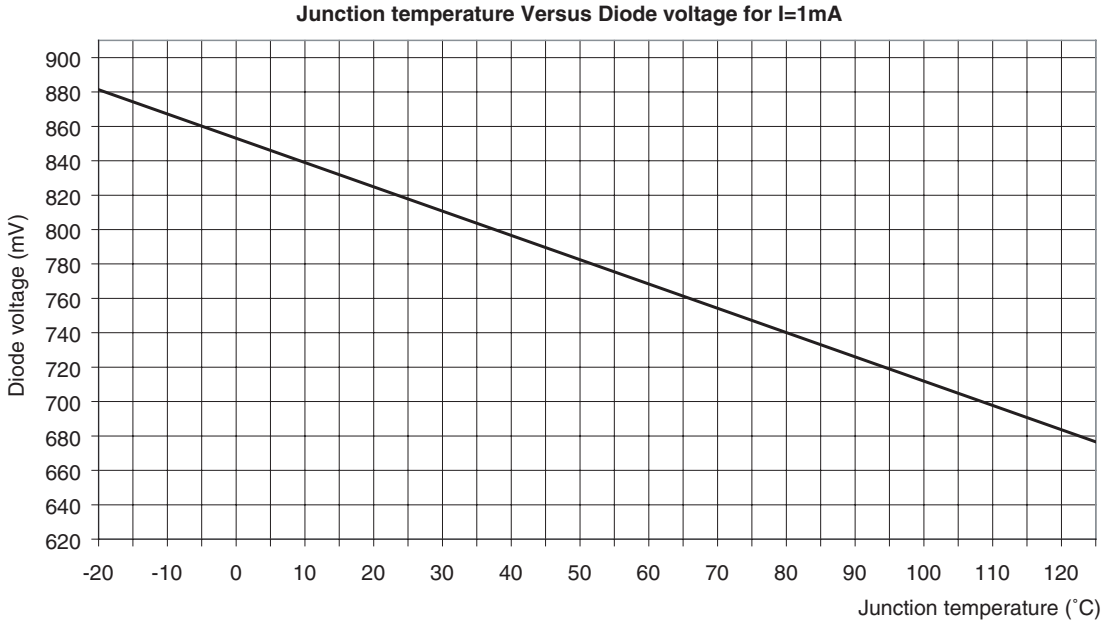
The measurement setup is described in Figure 11-2.

Figure 11-2. Die Junction Temperature Monitoring Setup



Note: The characteristic of the diode VBE forward voltage versus junction temperature (in steady state conditions) is provided below.

Figure 11-3.

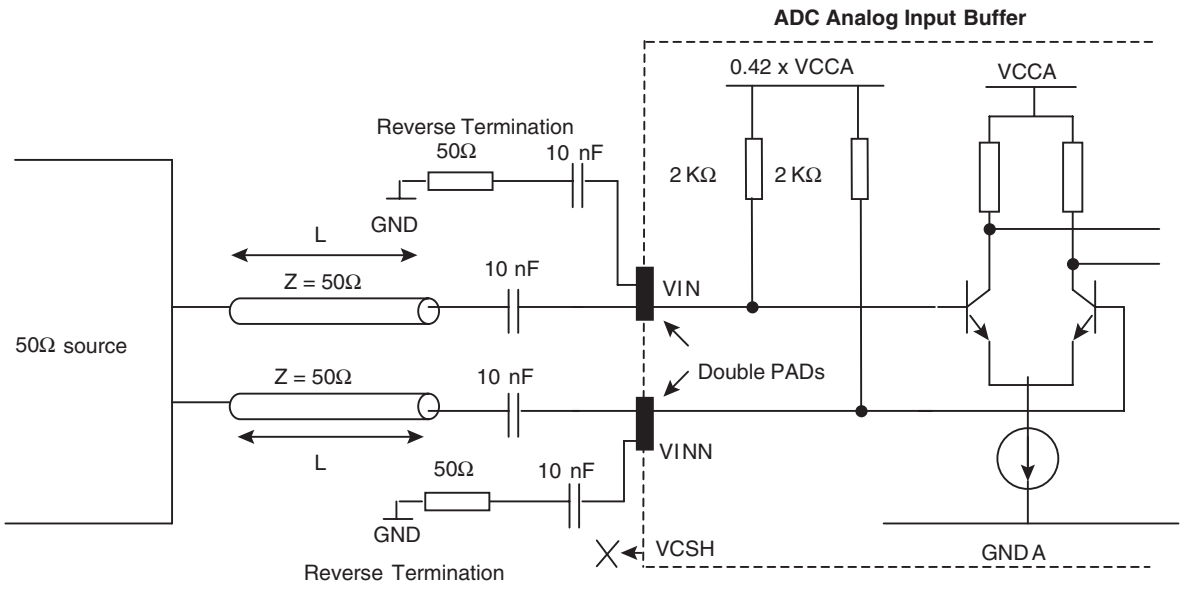


12. Implementing the AT84AS001 ADC

12.1 Analog Input Implementation in AC Coupled Mode

The analog inputs of the ADC were designed with a double pad implementation as illustrated in Figure 12-1 below. The reverse pad for each input should be tied to ground via a capacitor of 10 nF and a 50Ω resistor. In this mode, the VCSH output pin is left open.

Figure 12-1. AC Analog Inputs Termination Methods

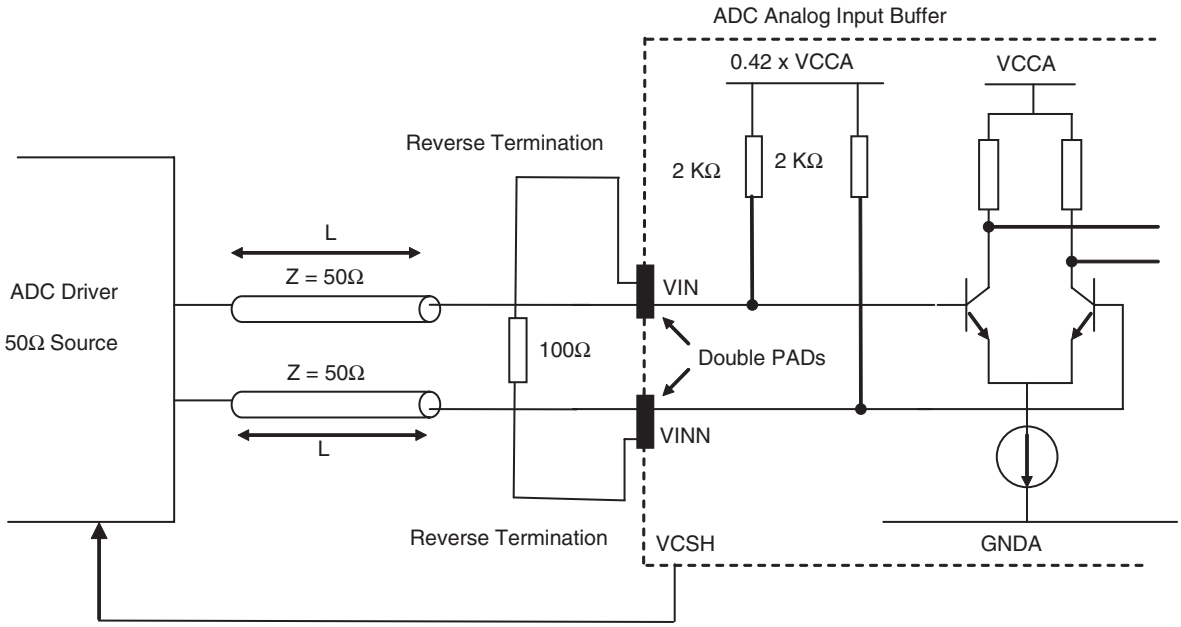


12.2 Analog Input Implementation in DC Coupling Configuration.

In order to set DC analog input voltage, the VCSH output pin must be used as described in Figure 12-2.

The double pad is connected to 100Ω resistance in differential configuration.

Figure 12-2. DC Coupling Configuration



Note: The VCSH value is equal to 0.42 $V_{CCA.}$

Table 12-1. Definition of Terms

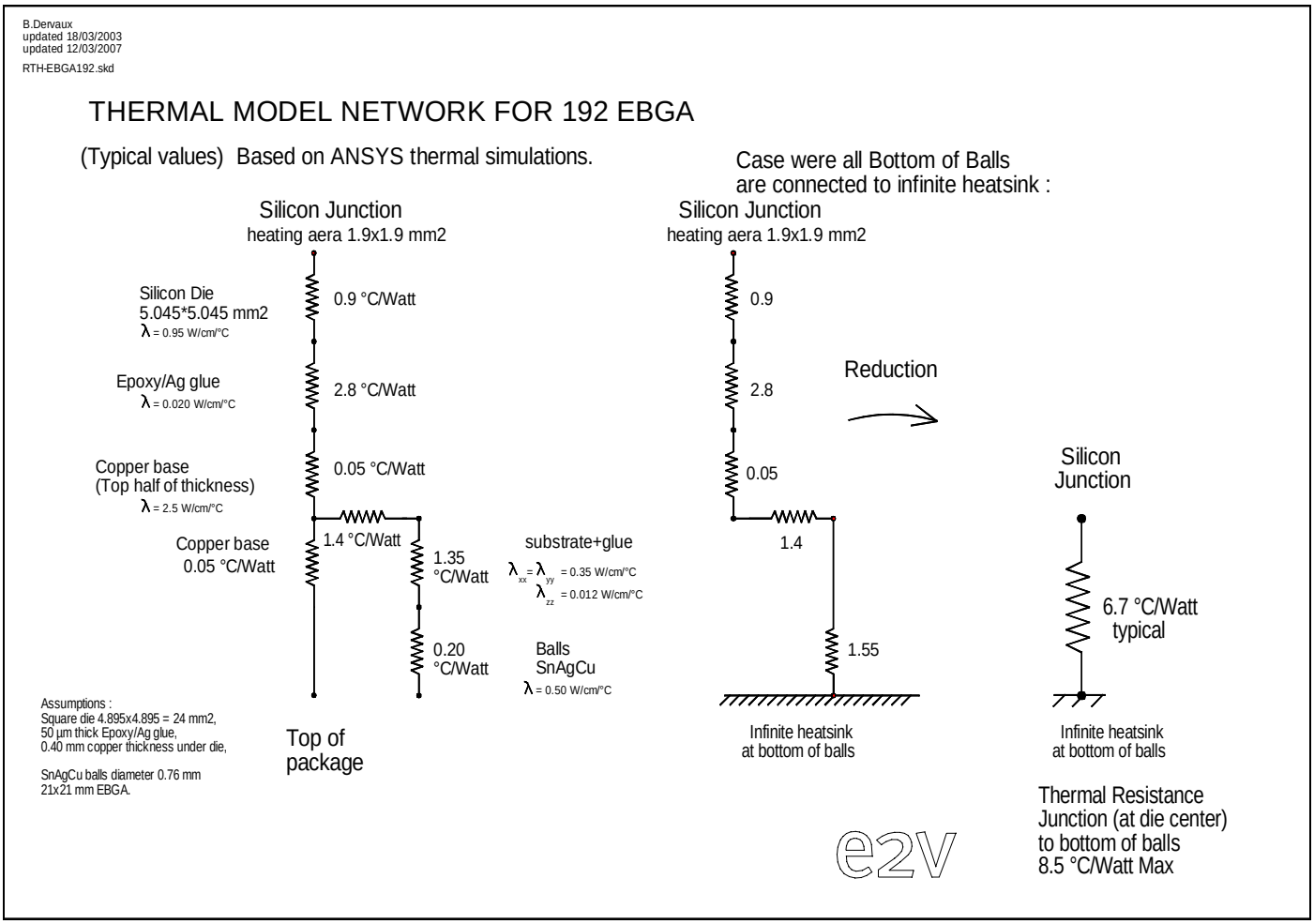
(BER)	Bit Error Rate	Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than ±4 LSB from the correct code.
(FPBW)	Full Power Input Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale.
(SINAD)	Signal-to-noise and Distortion Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components, including the harmonics except DC and jitter.
(SNR)	Signal-to-noise Ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the five first harmonics.
(THD)	Total Harmonic Distortion	Ratio expressed in dBc of the RMS sum of the first 25 harmonic components, to the RMS value of the measured fundamental spectral component.
(SFDR)	Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (radar systems, digital receiver, network analyzer, etc.). It may be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (i.e. always related back to converter full-scale).
(Multitone SFDR)	Multitone Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the next highest spectral component (peak spurious spectral component). This peak spurious component may or may not be an IMD product. SFDR is the key parameter for selecting a converter to be used in a frequency domain application (radar systems, digital receiver, network analyzer, etc.). It may be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (i.e. always related back to converter full-scale).
(ENOB)	Effective Number of Bits	$ENOB = \frac{SINAD - (1 \cdot 76) + 20 \log(A/V/2)}{6 \cdot 02}$ Where A is the actual input amplitude and V is the full-scale range of the ADC under test
(DNL)	Differential Non-Linearity	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	Integral Non Linearity	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(DG)	Differential Gain	The peak gain variation (in percent) at five different DC levels for an AC signal of 20% full-scale peak-to-peak amplitude.
(DP)	Differential Phase	Peak phase variation (in degrees) at five different DC levels for an AC signal of 20% full-scale peak-to-peak amplitude.
(TA)	Aperture Delay	Delay between the rising edge of the differential clock inputs (CLKI,CLKIN) (zero crossing point), and the time at which (V_{IN},V_{INN}) is sampled.
(JITTER)	Aperture Uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	Settling Time	Time delay to achieve 0.2 % accuracy at the converter output when a 80% full-scale step function is applied to the differential analog input.
(ORT)	Overvoltage Recovery Time	Time to recover 0.2 % accuracy at the output, after a 150 % full-scale step applied on the input is reduced to mid-scale.
(TOD)	Digital Data Output Delay	Delay from the falling edge of the differential clock inputs (CLKI,CLKIN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TD1)	Time Delay from Data to Data Ready	Time delay from data transition to data ready.
(TD2)	Time Delay from Data Ready to Data	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period.

Table 12-1. Definition of Terms (Continued)

(TC)	Encoding Clock Period	TC1 = minimum clock pulse width (high) TC = TC1 + TC2 TC2 = minimum clock pulse width (low)
(TPD)	Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TR)	Rise Time	Time delay for the output signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall Time	Time delay for the output data signals to fall from 80% to 20% of delta between low level and high level.
(PSRR)	Power Supply Rejection Ratio	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	Non Return to Zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	Intermodulation Distortion	The two-tones Intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at - 7dB full-scale.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.

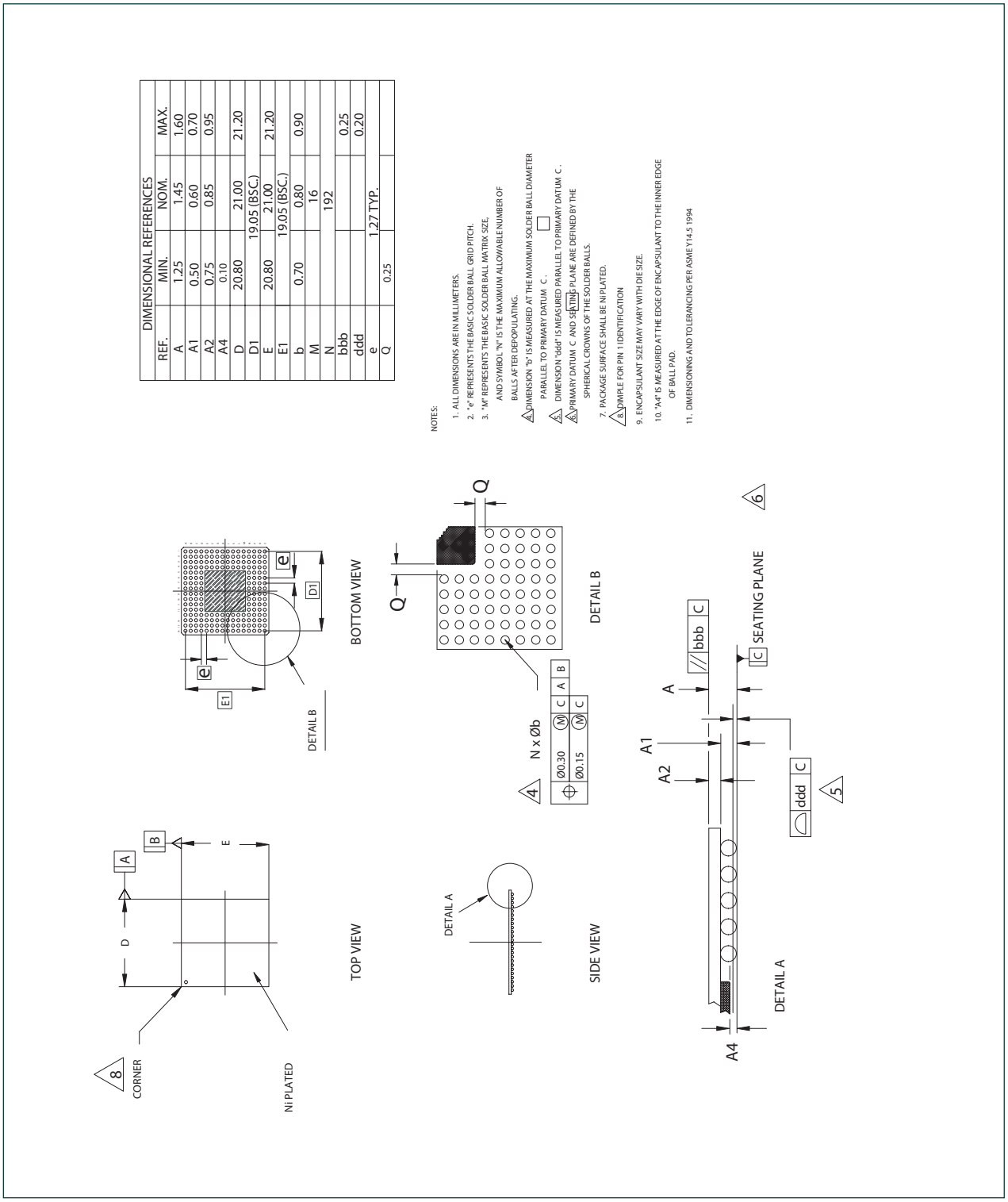
13. EBGA192 Thermal Model

Figure 13-1. Thermal Resistance from Junction to Bottom of Balls



14. Package Information

14.1 EBGA192 Mechanical Drawing



15. Ordering Information

Table 15-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84AS001CTPY	EBGA 192	RoHS compliant Commercial *C* grade $0° C < T_{amb} < 70° C$	Standard	For availability please contact your local sales office
AT84AS001VTPY	EBGA 192	RoHS compliant Industrial *V* grade $–40° C < T_{amb} < 85° C$	Standard	For availability please contact your local sales office
AT84AS001TP-EB	EBGA192	Ambient	Prototype	Evaluation board

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