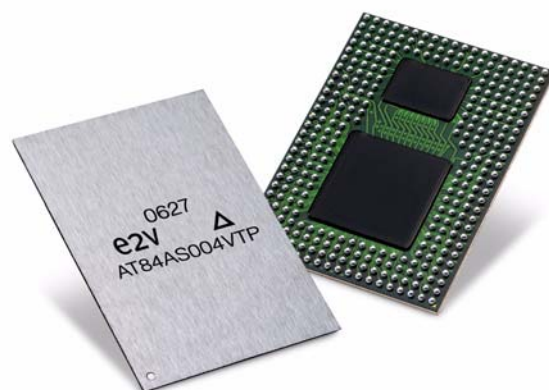


## Datasheet

### Features

- 10-bit Resolution
- 2 Gsps Sampling Rate
- Selectable 1:2 or 1:4 Demultiplexed Output
- 500 mVpp Differential 100 $\Omega$  or Single-ended 50 $\Omega$  Analog Input
- 100 $\Omega$  Differential or Single-ended 50 $\Omega$  Clock Input
- LVDS Output Compatibility
- Functions:
  - ADC Gain Adjust
  - Sampling Delay Adjust
  - 1:4 Demultiplexed Simultaneous or Staggered Digital Outputs
  - Data Ready Output with Asynchronous Reset
  - Out-of-range Output Bit (11th Bit)
- Power Consumption: 6.5W
- Power Supplies: -5V, -2.2V, 3.3V and  $V_{PLUSD}$  Output Power Supply
- Package
  - Cavity Down EBGA 317 (Enhanced Ball Grid Array)
  - 25 × 35 mm Dimensions



### Performances

- 3 GHz Full Power Analog Input Bandwidth
- -0.5 dB Gain Flatness from DC up to 1.5 GHz
- Single-tone Performance at  $F_s = 2$  Gsps, Full First and Second Nyquist (-1 dBFS)
  - ENOB = 7.8 Effective Bits,  $F_{IN} = 1000$  MHz
  - SNR = 51 dBc, SFDR = -55 dBc,  $F_{IN} = 1000$  MHz
  - ENOB = 7.5 Effective Bits,  $F_{IN} = 2$  GHz
  - SNR = 50 dBc, SFDR = -54 dBc,  $F_{IN} = 2$  GHz
- Dual-tone Performance (IMD3) at  $F_s = 2$  Gsps (-7 dBFS Each Tone)
  - $F_{in1} = 945$  MHz,  $F_{in2} = 955$  MHz: IMD3 = -60 dBFS
  - $F_{in1} = 1545$  MHz,  $F_{in2} = 1555$  MHz: IMD3 = -60 dBFS

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for the latest version of the datasheet

## Screening

- Temperature Range:
  - $T_{amb} > 0^{\circ}\text{C}$ ;  $T_J < 90^{\circ}\text{C}$  (Commercial C Grade)
  - $T_{amb} > -40^{\circ}\text{C}$ ;  $T_J < 110^{\circ}\text{C}$  (Industrial V Grade)

## Applications

- Direct RF Down Conversion
- Broadband Digital Receivers
- Test Instrumentation
- High Speed Data Acquisition
- High Energy Physics

## 1. Description

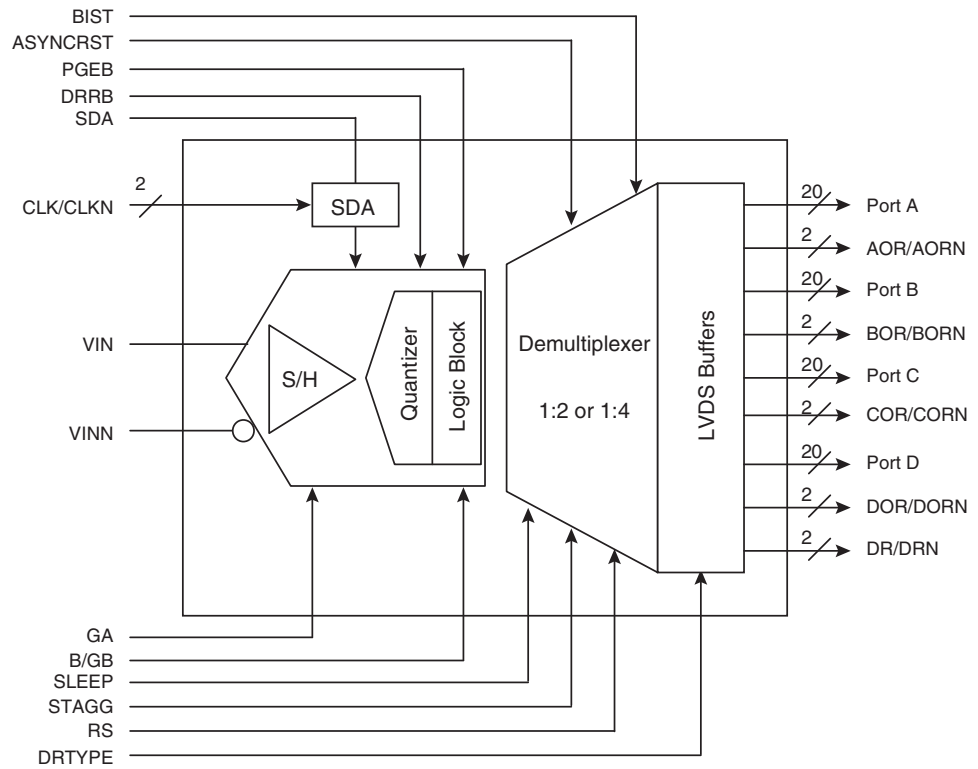
The AT84AS004 combines a 10-bit 2 Gsps analog-to-digital converter with a 1:4 DMUX, designed for accurate digitization of broadband signals in either first or second Nyquist zone. It features 7.8 Effective Number of Bits (ENOB) and –55 dBFS Spurious Free Dynamic Range (SFDR) at 2 Gsps over the full first Nyquist zone and 7.5-bit with 54 dB SFDR over full second Nyquist.

The 1:4 demultiplexed digital outputs are LVDS logic compatible, allowing easy interfacing with standard FPGAs or DSPs. The AT84AS004 operates at up to 2 Gsps.

The AT84AS004 comes in a 25 × 35 mm EBGA317 package. This package has the same TCE as FR4 boards, offering excellent reliability when subjected to large thermal shocks.

## 2. Block Diagram

Figure 2-1. Block Diagram



## 3. Functional Description

The AT84AS004 is a 10-bit 2 Gsps ADC combined with a 1:4 demultiplexer (DMUX) allowing to lower the 11 bit output data stream (10-bit data and one out-of-range bit) by a selectable factor of 4 or 2. The ADC works in fully differential mode from analog input through to digital outputs.

The ADC should be 50Ω reverse terminated, as close as possible to the EBGA Package input pin (1 mm maximum). The ADC Clock input is on-chip 100Ω differentially terminated. The output clock and the output data are LVDS logic compatible, and should be 100Ω differentially terminated.

The AT84AS004 ADC features two asynchronous resets:

- DRRB, which ensures that the first digitized data corresponds to the first acquisition.
- ASYNCRST, which ensures that the first digitized data will be output on port A of the DMUX.

The ADC gain can be tuned-in to unity gain by the means of the GA analog control input A Sampling Delay Adjust function (SDA analog control input, activated via the SDAEN signal) may be used to fine-tune the ADC aperture delay by  $\pm 120$  ps around its center value. The SDA function may be of interest for interleaving multiple ADCs. The control pin B/GB is provided to select either a binary or gray data output format.

A tunable delay cell (controlled via CLKDACTRL) is integrated between the ADC and the DMUX on the clock path to fine tune the data vs. clock alignment at the interface between the ADC and the DMUX. This delay can be tuned from  $-275$  to  $275$  ps around default center value, featuring a 550 ps typical delay tuning range. An extra standalone delay cell is also provided, (controlled via DACTRL analog control input and activated via DAEN). The tuning range is typically 550 ps.

A pattern generator (PGEB) is integrated in the ADC part for debug or acquisition setup. Similarly, a Built-in Self Test (BIST) is provided for quick debug of the DMUX part. The output demultiplexing 1:4 or 1:2 ratio can be selected by the means of RS digital control input.

Two modes for the output clock (via DRTYPE) can be selected:

- DR mode: only the output clock rising edge is active, the output clock rate is the same as the output data rate
- DR/2 mode: both the output clock rising and falling edges are active, the output clock rate is half the output data rate

The data outputs are available at the output of the AT84AS004 in two different modes:

- Staggered: even and odd bits come out with half a data period delay
- Simultaneous: even and odd bits come out at the same time

A Power reduction mode (SLEEP control input) is provided to reduce the DMUX power consumption.

The ADC junction temperature monitoring is made possible through the DIODE input by sensing the voltage drop across 1 diode implemented on the ADC close to chip hot point.

The AT84AS004 is delivered in an Enhanced Ball Grid Array (EBGA), very suitable for applications subjected to large thermal variations (thanks to its TCE which is similar to FR4 material TCE).

**Table 3-1.** Functions Description

Name	Function		
V <sub>CCA</sub>	Analog 3.3V power supply		
V <sub>CCD</sub>	Digital 3.3 V power supply		
V <sub>EE</sub>	Analog –5V power supply		
V <sub>PLUSD</sub>	Output 2.5 V power supply		
V <sub>MINUSD</sub>	Output –2.2V power supply		
AGND	Analog ground		
DGND	Digital ground		
CLK, CLKN	Input clock signals		
VIN, VINN	Analog input data		
DRRB	ADC reset		
ASYNCRST	DMUX asynchronous reset		
DR/DRN	Output clock signals		
A0...A9 A0N...A9N	Output data port A		
AOR/DRAN, AORN/DRA	Out Of Range bit port A or Output Clock in staggered mode for port A	<b>Name</b>	<b>Function</b>
B0...B9 B0N...B9N	Output data port B	DAI, DAIN	Input signals for standalone delay cell
BOR/DRBN, BORN/DRB	Out Of Range bit port B or Output clock in staggered mode for port B	DAO, DAON	Output signals for standalone delay cell
C0...C9 C0N...C9N	Output data port C	GA	ADC gain adjust
COR/DRCN, CORN/DRC	Out Of Range bit port C or Output clock in staggered mode for port C	SDAEN	ADC SDA enable
		SDA	ADC sampling delay adjust
D0...D9 D0N...D9N	Output data port D	PGEB	ADC pattern generator
		B/GB	Binary or gray output code selection
		SLEEP	Sleep mode selection signal
DOR/DRDN, DORN/DRD	Out Of Range bit port D or Output clock in staggered mode for port D	STAGG	Staggered mode selection for data outputs
RS	DMUX ratio selection signal	CLKTYPE	Input clock type selection signal (to be connected to V <sub>CCD</sub> or left floating)
CLKDACTRL	Control signal for clock delay cell	DRTYPE	Output clock type selection signal
DACTRL	Control signal for standalone delay cell	BIST	Built-in Self Test
DAEN	Enable signal for standalone delay cell	DIODE ADC	Diode for die junction temperature monitoring (ADC)

## 4. Specifications

### 4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Analog positive supply voltage	$V_{CCA}$	GND to 6	V
Digital positive supply voltage	$V_{CCD}$	GND to 3.6	V
Analog negative supply voltage	$V_{EE}$	GND to -5.5	V
Digital positive supply voltage	$V_{PLUSD}$	GND to 3	V
Digital negative supply voltage	$V_{MINUSD}$	GND to -3	V
Maximum difference between $V_{PLUSD}$ and $V_{MINUSD}$	$V_{PLUSD} - V_{MINUSD}$	5	V
Analog input voltages	$V_{IN}$ or $V_{INN}$	-1.5 to 1.5	V
Maximum difference between $V_{IN}$ and $V_{INN}$	$V_{IN} - V_{INN}$	-1.5 to 1.5	V
Clock input voltage	$V_{CLK}$ or $V_{CLKN}$	-1 to 1	V
Maximum difference between $V_{CLK}$ and $V_{CLKN}$	$V_{CLK} - V_{CLKN}$	-1 to 1	V
Control input voltage	GA, SDA	-1 to 0.8	V
Digital input voltage	SDAEN, B/GB, PGEB, DECB	-5 to 0.8	V
ADC reset voltage	DRRB	-0.3 to $V_{CCA} + 0.3$	V
DMUX function input voltage	RS, CLKTYPE, DRTYPE, SLEEP, STAGG, BIST, DAEN	-0.3 to $V_{CCD} + 0.3$	V
DMUX asynchronous reset	ASYNCRST	-0.3 to $V_{CCD} + 0.3$	
DMUX input voltage	DAI, DAIN	-0.3 to $V_{CCD} + 0.3$	V
DMUX control voltage	CLKDACTRL, DACTRL	-0.3 to $V_{CCD} + 0.3$	V
Maximum input voltage on DIODE	DIODE ADC	700	mV
Maximum input current on DIODE	DIODE ADC	1	mA
Junction temperature	$T_J$	135	°C

- Notes:
1. Absolute maximum ratings are short term limiting values (referenced to GND = 0 V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.
  2. All integrated circuits have to be handled with appropriate care to avoid damage due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

**Table 4-2.** Recommended Condition of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive supply voltage	$V_{CCA}$		3.3	V
Positive supply voltage	$V_{CCD}$		3.3	V
Negative supply voltage	$V_{EE}$		-5.0	V
Positive negative supply voltage	$V_{MINUSD}$		-2.2	V
Differential analog input voltage	$V_{IN} - V_{INN}$		500	mVpp
Differential clock input level	$V_{inclk}$	50Ω single-ended ( $V_{INN}$ grounded through 50Ω)	±125 500	mV mVpp
Clock input power level (ground common mode)	$P_{CLK} P_{CLKN}$	50Ω single-ended clock input or 100Ω differential clock (recommended)	0	dBm
ADC control input voltage	GA, SDA		-0.5 to 0.5	V
ADC functions	SDAEN, B/GB, PGEB, DECB		GND or VEE	V
ADC reset	DRRB		GND to 3.3V	V
DMUX standalone delay cell inputs	DAI, DAIN		GND to 3.3V	V
DMUX control inputs	SLEEP, STAGG, ASYNCRST, BIST, RS, DAEN, DRTYPE, CLKDACTRL, DACTRL		GND to 3.3V	V
Operating temperature range	$T_C; T_J$	Commercial C grade industrial V grade	$0^{\circ}\text{C} < T_{amb}; T_J < 90^{\circ}\text{C}$ $-40^{\circ}\text{C} < T_{amb}; T_J < 110^{\circ}\text{C}$	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$		-55 to 125	$^{\circ}\text{C}$
Maximum junction temperature	$T_J$		125	$^{\circ}\text{C}$

## 4.2 Electrical Operating Characteristics

- $V_{CCA} = V_{CCD} = 3.3V$ ,  $V_{EE} = -5V$ ,  $V_{MINUSD} = -2.2V$
- $V_{IN} - V_{INN} = -1$  dBFS ( single-ended driven with VINN connected to ground via 50Ω)
- $P_{CLK} = 0$  dBm (differential driven)

**Table 4-3.** DC Electrical Characteristics at Ambient Temperature and Hot Temperature (TJ Max)

Parameter		Test Level	Symbol	Min	Typ	Max	Unit
Resolution					10		Bit
Power Requirements							
Positive Supply Voltages	-analog -digital -digital outputs	1	V <sub>CCA</sub> V <sub>CCD</sub> V <sub>PLUSD</sub>	3.15 3.15 2.4	3.3 3.3 2.5	3.45 3.45 2.6	V V V
Positive Supply Current	-analog V <sub>CCA</sub> = 3.3V -digital V <sub>CCD</sub> = 3.3V (1:2 DMUX) -digital V <sub>CCD</sub> = 3.3V (1:4 DMUX) -output V <sub>PLUSD</sub> = 2.5V (1:2 DMUX) -output V <sub>PLUSD</sub> = 2.5V (1:4 DMUX)	1	I <sub>VCCA</sub> I <sub>VCCD</sub> I <sub>VCCD</sub> I <sub>VPLUSD</sub> I <sub>VPLUSD</sub>		80 535 565 440 460	100 590 620 470 490	mA mA mA mA mA
Negative supply voltage V <sub>EE</sub>		1	V <sub>EE</sub>	−5.25	−5	−4.75	V
Negative supply current			I <sub>VEE</sub>		620	660	mA
Negative supply voltage			V <sub>MINUSD</sub>	−2.3	−2.2	−2.1	V
Negative supply current			I <sub>VMINUSD</sub>		190	200	mA
Power Dissipation (1:2 DMUX)			P <sub>D</sub>		6.5	7.1	W
Analog Inputs							
Full-scale input voltage range		4	V <sub>IN</sub>	−125		125	mV
Differential mode 0V common mode voltage			V <sub>INN</sub>	−125		125	mV
Full-scale input voltage range			V <sub>IN</sub> , V <sub>INN</sub>	−250	0	250	mV
Single-ended input option							
0V common mode voltage							
Analog input power level (50Ω single-ended)			P <sub>IN</sub>		−2		dBm
Analog input capacitance (die)			C <sub>IN</sub>		0.3		pF
Input leakage current			I <sub>IN</sub>		10		μA
Input resistance		4	R <sub>IN</sub>	49	50	51	Ω
- single-ended - differential			R <sub>IN</sub> , I <sub>NN</sub>	98	100	102	Ω



**Table 4-3.** DC Electrical Characteristics at Ambient Temperature and Hot Temperature (TJ Max) (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Clock Inputs						
Logic common mode compatibility for clock inputs	4		Differential ECL to LVDS (AC coupling)			
Clock input common voltage range (V <sub>CLK</sub> or V <sub>CLKN</sub> ) (0V common mode)		V <sub>CM</sub>	−1.2	0	0.3	V
Clock input power level (low-phase noise sinewave input) 50Ω single-ended or 100Ω differential		P <sub>CLK</sub>	−4	0	4	dBm
Clock input swing (single ended with CLKN = 50Ω to GND)		V <sub>CLK</sub>	±200	±320	±500	mV
Clock input swing (differential voltage) on each clock input		V <sub>CLK</sub> , V <sub>CLKN</sub>	±141	±226	±354	mV
Clock input capacitance (die)		C <sub>LK</sub>		0.3		pF
Clock input resistance						
- Single-ended		R <sub>CLK</sub>	45	50	55	Ω
- Differential ended	R <sub>CLK</sub> , R <sub>CLKN</sub>	90	100	110	Ω	
Digital Data Outputs						
Logic compatibility			LVDS			
50Ω transmission lines, 100Ω (2 × 50Ω) differential termination)	1					
- Logic low		V <sub>OL</sub>	−	1.075	1.25	V
- Logic high		V <sub>OH</sub>	1.25	1.425	−	V
- Differential output		V <sub>ODIFF</sub>	250	350	500	mV
- Common mode		V <sub>OCM</sub>	1.125	1.25	1.375	V
Control Function Inputs						
DRRB and ASYNCRST	1					V
- Logic low		V <sub>IL</sub>	0		1.0	V
- Logic high		V <sub>IH</sub>	1.6		3.3	V
RS, DRTYPE, SLEEP, STAGG, BIST, DAEN	4				0.5	V
- Logic low		V <sub>IL</sub>			10	Ω
		R <sub>IL</sub>	0			V
- Logic high		V <sub>IH</sub>	2		Infinite	Ω
		R <sub>IH</sub>	10 K			
SDAEN, PGEB, B/GB	1					
- Logic low		V <sub>IL</sub>		V <sub>EE</sub>	−3	V
- Logic high		V <sub>IH</sub>	−2	0	0	V
DAI, DAIN	1					
- Differential input		V <sub>IDIFF</sub>	1	1.25	1.6	V
- Common mode		V <sub>ICM</sub>	100	350	−	mV

**Table 4-3.** DC Electrical Characteristics at Ambient Temperature and Hot Temperature (TJ Max) (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
GA, SDA	1		−0.5		0.5	V
CLKDACTRL, DACTRL	1		$1/3 \times V_{CCD}$		$2/3 \times V_{CCD}$	V
DC accuracy						
DNLrms <sup>(1)</sup>	1	DNLrms		0.2	0.3	LSB
Differential nonlinearity <sup>(1)</sup>	1	DNL <sup>−</sup>	−0.8			LSB
Differential nonlinearity <sup>(1)</sup>	1	DNL <sup>+</sup>		0.8	1.5	LSB
Integral nonlinearity <sup>(1)</sup>	1	INL <sup>−</sup>	−4	−2		LSB
Integral nonlinearity <sup>(1)</sup>	1	INL <sup>+</sup>		2	4	LSB
Gain central value <sup>(2)</sup>	1		0.95	1	1.05	
Gain error drift	4			23	35	ppm/ °C
Input offset voltage	1		−10		10	mV

Notes: 1. Histogram testing at  $F_s = 1.4$  Gsps  $F_{in} = 695$  MHz.  
2. This range of gain can be set to 1 thanks to the gain adjust function.

**Table 4-4.** AC Electrical Characteristics at Ambient Temperature and Hot Temperature (T<sub>J</sub> Max)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Analog Inputs						
Full power input bandwidth <sup>(1)</sup>	4	FPBW		3		GHz
Small signal input bandwidth (10% full-scale) <sup>(1)</sup>		SSBW		3.3		GHz
Gain flatness <sup>(2)</sup>		BF		−0.5		dB
Input voltage standing wave ration <sup>(3)</sup>		VSWR		1.1: 1	1.2: 2	
AC Performance: Nominal Condition						
−1 dBFS single-ended input mode (unless otherwise specified); 50% clock duty cycle; 0 dBm differential clock (CLK,CLKN) binary output data format.						
Effective Number of Bits						
Fs = 1 Gsps      Fin = 100 MHz	1	ENOB	7.4	8		Bit
Fs = 1.5 Gsps      Fin = 750MHz	1		7.4	8		
Fs = 2 Gsps      Fin = 1000 MHz	4		7.3	7.8		
Fs = 2 Gsps      Fin = 2 GHz	4		7.1	7.5		
Signal to Noise Ratio						
Fs = 1 Gsps      Fin = 100 MHz	1	SNR	50	52		dBc
Fs = 1.5 Gsps      Fin = 750MHz	1		49	52		
Fs = 2 Gsps      Fin = 1000 MHz	4		48	51		
Fs = 2 Gsps      Fin = 2 GHz	4		48	50		
Total Harmonic Distortion						
Fs = 1 Gsps      Fin = 100 MHz	1	THD	46	52		dBc
Fs = 1.5 Gsps      Fin = 750MHz	1		46	52		
Fs = 2 Gsps      Fin = 1000 MHz	4		45	49		
Fs = 2 Gsps      Fin = 2 GHz	4		45	49		
Spurious Free Dynamic Range						
Fs = 1 Gsps      Fin = 100 MHz	1	SFDR	50	58		dBc
Fs = 1.5 Gsps      Fin = 750MHz	1		50	58		
Fs = 2 Gsps      Fin = 1000 MHz	4		48	55		
Fs = 2 Gsps      Fin = 2 GHz	4		48	54		
Two-tone Third-order Intermodulation Distortion						
Fs = 2 Gsps		IIMD3				dBFS
Fin1 = 945 MHz, Fin2 = 955 MHz [−7 dBFS]	4			60		
Fin1 = 1545 MHz, Fin2 = 1555 MHz [−7 dBFS]	4			60		

- Notes: 1. See “Definitions of Terms” on page 42.  
2. From DC to 1.5 GHz.  
3. Specified from DC up to 2.5 GHz input signal. Input VSWR is measured on a soldered device. It assumes an external 50Ω ± 2Ω controlled impedance line, and a 50Ω driving source impedance (S<sub>11</sub> ≤ 30 dB).

**Table 4-5.** Transient and Switching Performances

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Transient Performance						
Bit error rate <sup>(1)</sup>	4	BER	10 <sup>-11</sup>			Error/sample
ADC setting time (V <sub>IN</sub> -V <sub>INN</sub> = 400 mVpp)	4	TS		400		ps
Overvoltage recovery time	4	ORT			500	ps
ADC step response rise/fall time (10 –90%)	4			80	100	ps
Overshoot	5			4		%
Ringback	5			2		%
Switching Performance and Characteristics						
Maximum clock frequency <sup>(2)</sup>	4	F <sub>S</sub> Max	2			Gsps
Minimum clock frequency <sup>(2)</sup>		F <sub>S</sub> Min			200	Msps
Maximum clock pulse width (high)		TC1	0.25		2.5	ns
Minimum clock pulse width (low)		TC2	0.25		2.5	ns
Aperture delay <sup>(2)</sup>		TA		160		ps
Aperture uncertainty		Jitter		150		fs rms
DRRB pulse width			1			ns
ASYNCRST pulse width			1			ns
Output Data						
Data Output Delay <sup>(3)</sup>	4	TOD		7.2		ns
Data output delay Skew		T <sub>skew</sub>			400	ps
Data pipeline delay - Synchronized 1:2 ratio - Synchronized 1:4 ratio - Staggered 1:2 ratio - Staggered 1:4 ratio		TPD		5.5 7.5 4.5/5.5 4.5/5.5/6.5/7.5		Clock cycles
Data output rise/fall time (20% to 80%)		TR/TF			650	ps
Output Clock						
Output clock delay <sup>(3)</sup>	4	TDR		6.6		ns
Output clock rise/fall time (20% –80%)		TR/TF			650	ps
Output data to output clock propagation delay		TD2-TD1 TOD-TDR	200	500	600	ps

**Table 4-5.** Transient and Switching Performances (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
<b>Standalone Delay Cell (DACTRL) and Tunable Delay cell (CLKDACTRL)<sup>(4)</sup></b>						
Input frequency	4	FMSDA	600			MHz
Input duty cycle		DCYCSDA	40	50	60	%
Propagation delay with CLKDACTRL or DACTRL = $V_{CCD}/3$	4	TSDAMIN	1.70	2.00	2.30	ns
Propagation delay with CLKDACTRL or DACTRL = $2 \times V_{CCD}/3$	4	TSDAMAX	2.1	2.50	2.90	ns
Tuning range <sup>(4)</sup>	4	SDARANGE	400	550	600	ps

- Notes:
1. Output error amplitude <  $\pm 32$  LSB.  $F_s = 2$  Gsps  $T_J = 110^\circ\text{C}$ .
  2. See “Definitions of Terms” on page 42.
  3. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only. See “Definitions of Terms” on page 42.
  4. The delay cell used in both standalone delay cell and input clock path (DR) has a characteristic that is not linear with junction temperature. The largest tuning range is obtained near ambient temperature.

### 4.3 Explanation of Test Levels

Level	Comments
1	100% production tested at 25°C (for <i>C</i> Temperature range ).
2	100% production tested at 25°C, and sample tested at specified temperatures (for <i>V</i> temperature range).
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only guaranteed by design only

Note: Unless otherwise specified:  
Only minimum and maximum values are guaranteed (typical values are issued from characterization results).

## 4.4 Digital Coding

Differential Analog Input	Voltage Level	Digital Output			
		Binary (B/GB = GND or floating) MSB...LSB out-of-range		GRAY (B/GB = V <sub>EE</sub> ) MSB.....LSB out-of-range	
> 250.25 mV	>Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1	1	1 0 0 0 0 0 0 0 0 0	1
250.25 mV	Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1	0	1 0 0 0 0 0 0 0 0 0	0
249.75 mV	Top end of full-scale - ½ LSB	1 1 1 1 1 1 1 1 1 0	0	1 0 0 0 0 0 0 0 0 1	0
125.25 mV	3/4 full-scale + ½ LSB	1 1 0 0 0 0 0 0 0 0	0	1 0 1 0 0 0 0 0 0 0	0
124.75 mV	full-scale - ½ LSB	1 0 1 1 1 1 1 1 1 1	0	1 1 1 0 0 0 0 0 0 0	0
0.25 mV	Mid scale + ½ LSB	1 0 0 0 0 0 0 0 0 0	0	1 1 0 0 0 0 0 0 0 0	0
-0.25 mV	Mid scale - ½ LSB	0 1 1 1 1 1 1 1 1 1	0	0 1 0 0 0 0 0 0 0 0	0
- 124.75 mV	1/4 full-scale + ½ LSB	0 1 0 0 0 0 0 0 0 0	0	0 1 1 0 0 0 0 0 0 0	0
- 124.25 mV	1/4 full-scale - ½ LSB	0 0 1 1 1 1 1 1 1 1	0	0 0 1 0 0 0 0 0 0 0	0
- 249.75 mV	Bottom end of full-scale + ½ LSB	0 0 0 0 0 0 0 0 0 1	0	0 0 0 0 0 0 0 0 0 1	0
- 250.25 mV	Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0	0
≤250.25 mV	< Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0 0 0	1

A0 = B0 = C0 = D0 = LSB

A9 = B9 = C9 = D9 = MSB

## 5. Characterization Results

### 5.1 Nominal Conditions

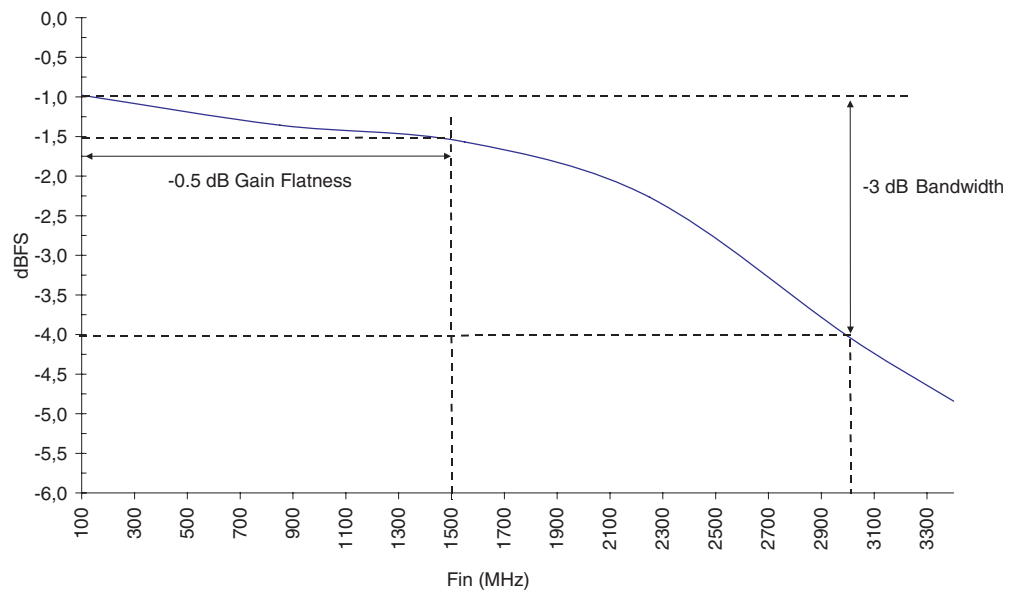
Unless otherwise specified:

- $V_{CCA} = 3.3V$ ,  $V_{CCD} = 3.3V$ ,  $V_{EE} = -5V$ ,  $V_{PLUSD} = 2.5V$ ,  $V_{MINUSD} = -2.2V$
- $T_J = 80^\circ C$
- 50% clock duty cycle, binary output data format
- -1 dBFS analog input

### 5.2 Full Power Input Bandwidth

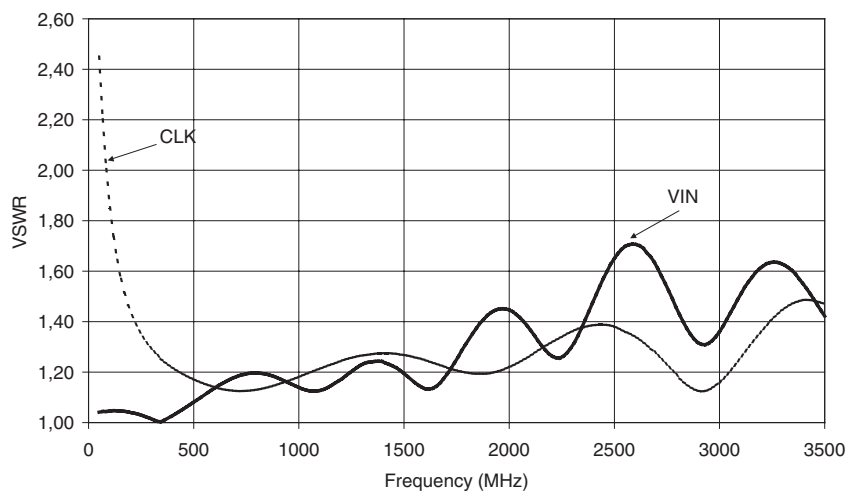
- Analog input level = -1 dBFS
- Gain flatness at -0.5 dB from DC to 1.5 GHz

**Figure 5-1.** Full Power Input Bandwidth at -3 dB



### 5.3 VSWR versus Input Frequency

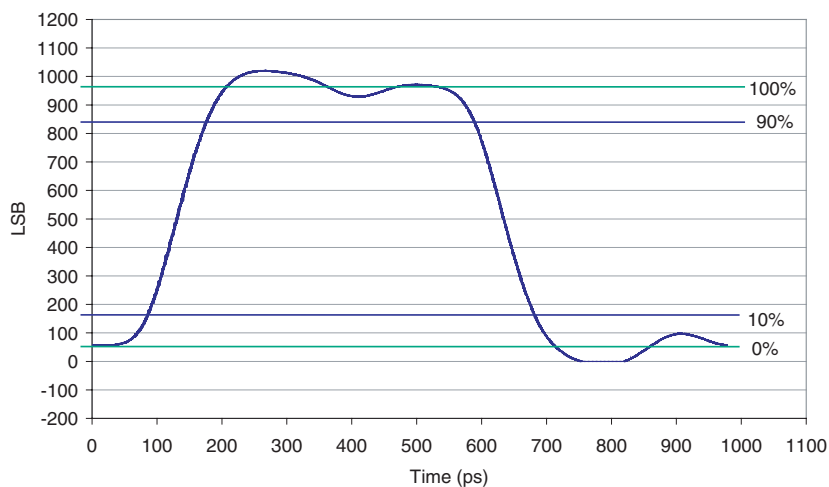
Figure 5-2. VSWR Curve for the Analog Input (VIN) and Clock (CLK)



### 5.4 Step Response

- $T_r \text{ measured} = 114.8 \text{ ps} = \sqrt{(T_{r\text{PulseGenerator}})^2 + (T_{r\text{ADC}})^2}$
- $T_{r\text{PulseGenerator}}$  (estimated) = 41 ps
- Actual  $T_{r\text{ADC}} = 107 \text{ ps}$

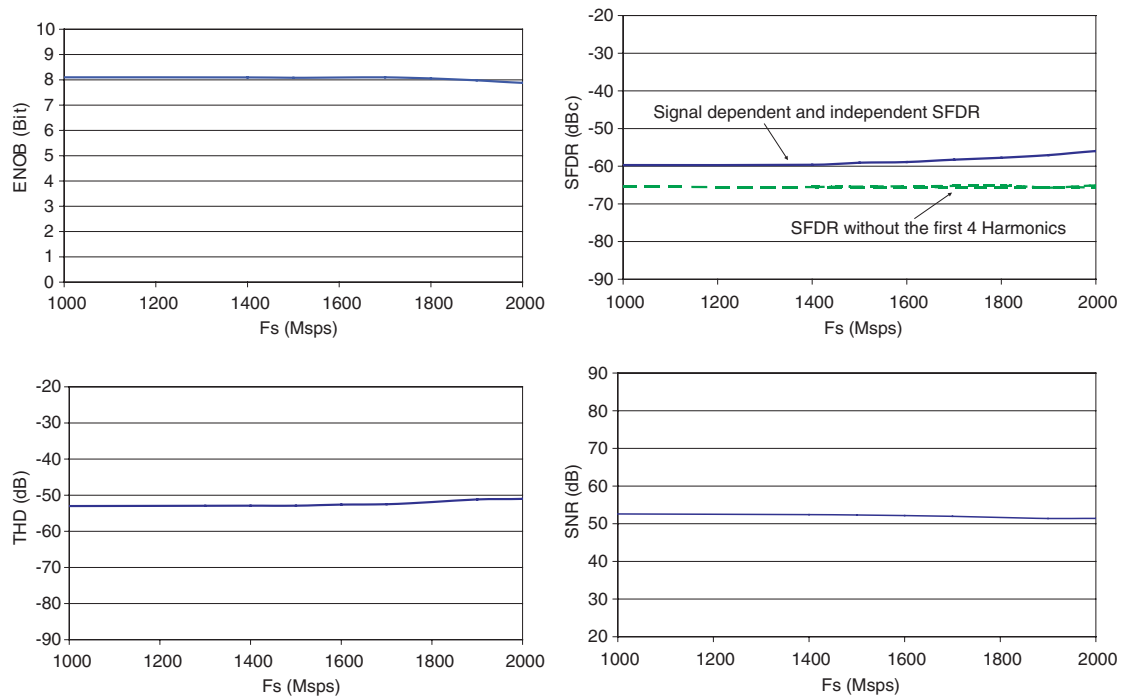
Figure 5-3. Step Response Rise Time ( $F_s = 2 \text{ Gsps}$ ,  $F_{in} = 1 \text{ GHz}$ )





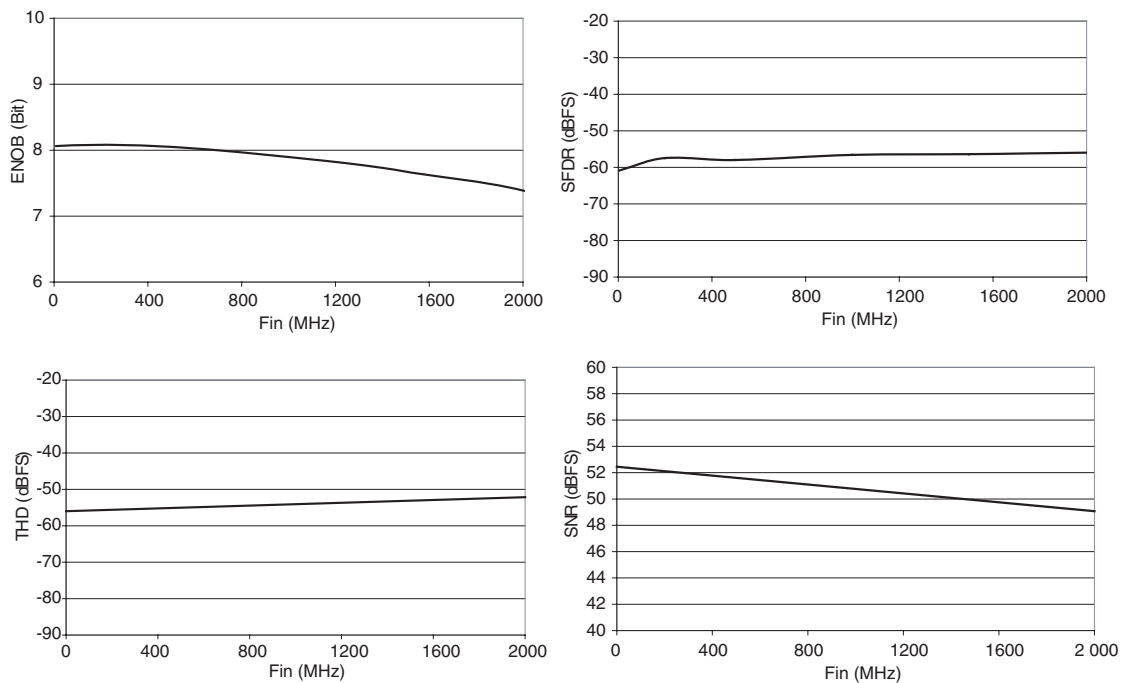
## 5.5 Dynamic Performance versus Sampling Frequency

**Figure 5-4.** Dynamic Parameters versus Sampling Frequency in Nyquist Conditions ( $F_{in} = F_s/2$ )



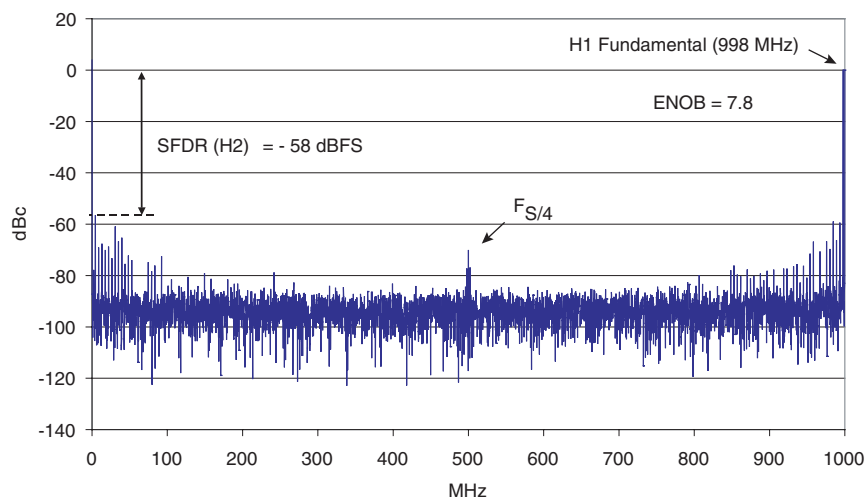
## 5.6 Dynamic Performance versus Input Frequency

**Figure 5-5.** Dynamic Parameters versus Input Frequency at  $F_s = 2$  Gps

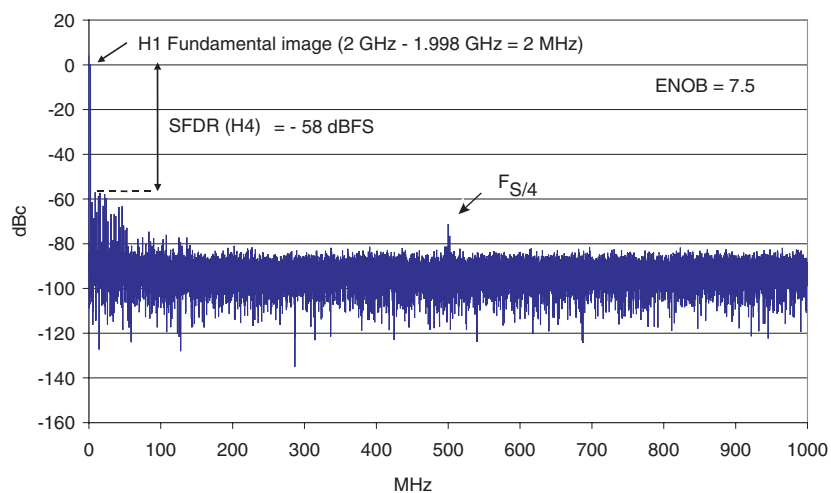


## 5.7 Signal Spectrum

**Figure 5-6.**  $F_s = 2$  Gsps,  $F_{in} = 998$  MHz  $-1$  dBFS Analog Input, 1:4 Demultiplexing Factor, 32 kpoint FFT

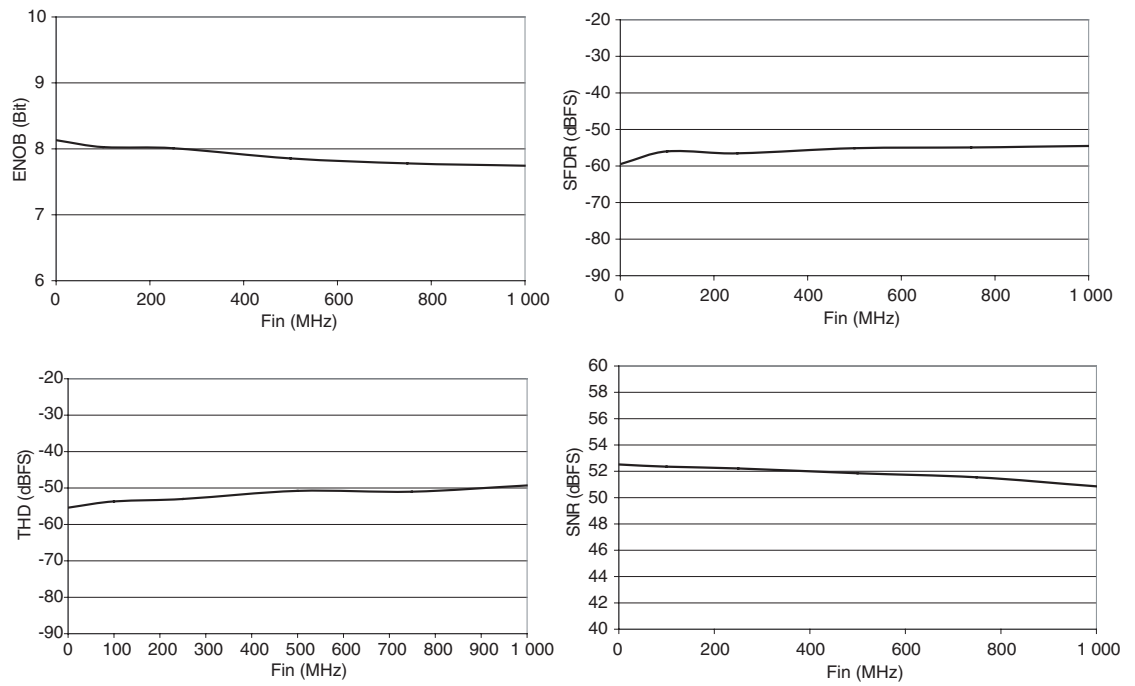


**Figure 5-7.**  $F_s = 2$  Gsps,  $F_{in} = 1998$  MHz  $-1$  dBFS Analog Input, 1:4 Demultiplexing Factor, 32 kpoint FFT

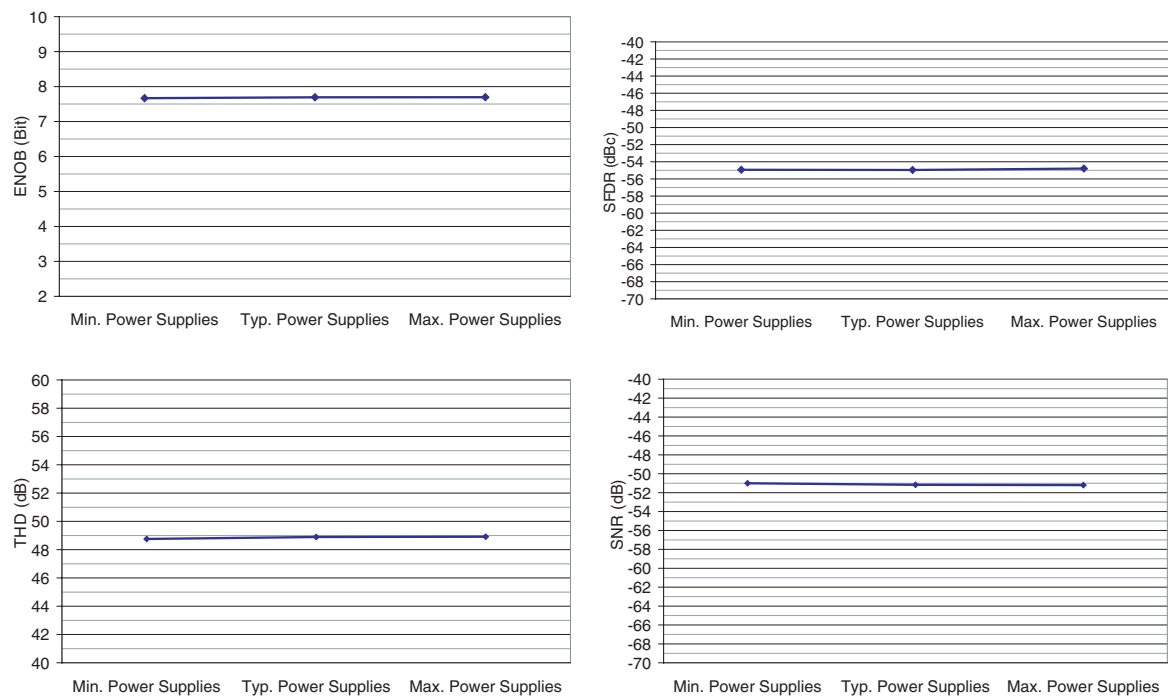


## 5.8 Dynamic Performance Sensitivity versus Temperature and Power Supply

**Figure 5-8.** Dynamic Parameters versus Junction Temperature at  $F_s = 2$  Gsps,  $F_{in} = 998$  MHz,  $-1$  dBFS Analog Input



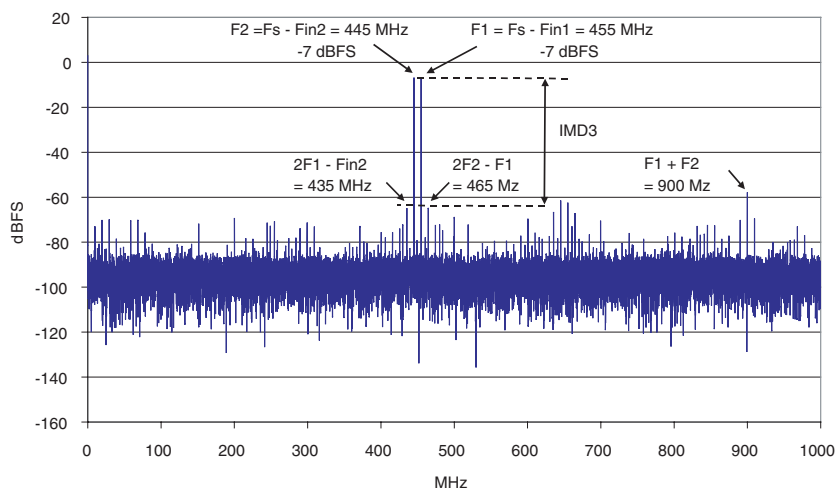
**Figure 5-9.** Dynamic Parameters at Min., Typ. and Max. Power Supplies,  $F_s = 2$  Gsps,  $F_{in} = 998$  MHz,  $-1$  dBFS Analog Input



Note: Minimum power supplies:  $V_{CC} = 3.45V$ ,  $V_{EE} = -4.75V$   
 Typical power supplies:  $V_{CC} = 3.3V$ ,  $V_{EE} = -5V$   
 Maximum power supplies:  $V_{CC} = 3.15V$ ,  $V_{EE} = -5.25V$

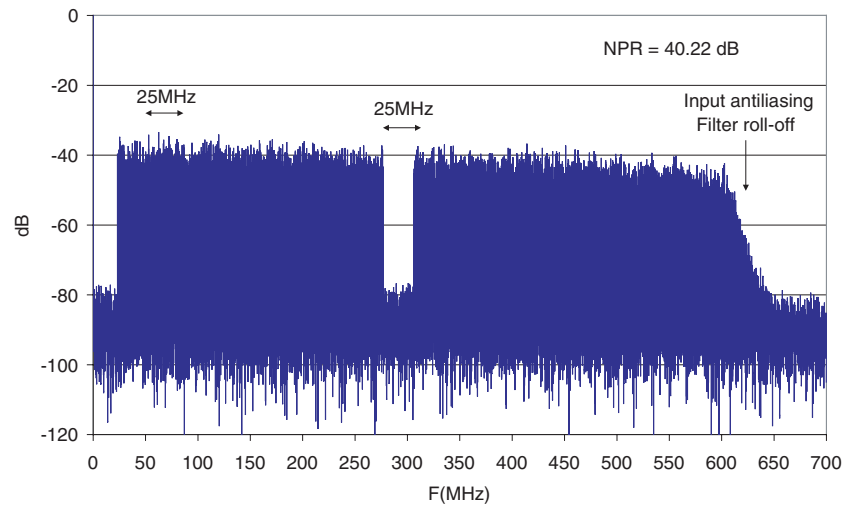
## 5.9 Dual Tone Performance

**Figure 5-10.** Dual Tone Signal Spectrum at  $F_s = 2$  Gsps,  $F_{in1} = 1545$  MHz,  $F_{in2} = 1555$  MHz ( $-7$  dBFS)



## 5.10 NPR Performance

**Figure 5-11.** Digitizing of 575 MHz Broadband Pattern at 1.4 Gsps, 25 MHz Notch Centered Around 290 MHz, -12 dBFS Loading Factor



## 6. Pin Description

Figure 6-1. EBG317 Pinout Table (View from Bottom Package)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
1	NC	B3N	B3N	B4	B5	B6	B7N	B8N	B9N	B9N	B9N	B9N	B9N	B9N	B9N	B9N	B9N	B9N	B9N
2	B3N	B3	B2	VCCD	VCCD	VCCD	VPLUSD	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND
3	B2N	B1	B0	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
4	B1N	B0N	B0N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
5	B0N	B0N	B0N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
6	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
7	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
8	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
9	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
10	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
11	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
12	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
13	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
14	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
15	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
16	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
17	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
18	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
19	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
20	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
21	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
22	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
23	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
24	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
25	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
26	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD
27	ADP1N	ADP1N	ADP1N	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD	VPLUSD

Table 6-1. Pin Description

Symbol	Pin Number	Function
Power Supplies		
DGND	C17, C18, D17, D18, F3, F4, H3, H4, M3, M4, P3, P4, R18, T18, U16, U17	Digital ground
AGND	B21, B23, C21, C23, D21, D23, E21, E23, F21, F23, F26, F27, G25, G26, G27, H25, H26, J25, J26, K27, N25, P25, R22, R23, R24, R25, R26, R27, T22, t23, T24, T25, T26, T27, U22, U23, U24, U25, U26, U27, V21, V23, V24, V26, V27, W22, W25, W26, W27	Analog ground
V <sub>CCA</sub>	A24, A26, A27, B24, B26, B27, C24, C26, C27, D24, D26, D27, E24, E26, F25, L25, L26, M27, R21, T21, U21,	ADC analog positive power supply
V <sub>EE</sub>	A25, B22, B25, C20, C22, C25, D20, D22, D25, E20, E22, E25, F20, F22, F24, K25, K26, L27, M25, M26, N26, N27, R20, T20	ADC analog negative power supply
SUB	D14, D15, R17	Connect to V <sub>EE</sub>
V <sub>PLUSD</sub>	C4, C5, C6, C7, C9, C11, C13, C14, C15, C16, C19, D5, D6, D7, D9, D11, D13, D19, E3, E19, F19, J3, J4, L3, L4, N3, N4, R3, R4, R19, T6, T7, T9, T11, T13, T14, T15, T19, U4, U5, U6, U7, U9, U11, U13, U14, U15	ADC and DMUX output power supply
V <sub>CCD</sub>	C3, C8, C10, C12, D3, D4, D8, D10, D12, D16, E4, E17, G3, G4, K3, K4, R16, T3, T4, T5, T8, T10, T12, T16, T17, U3, U8, U10, U12	DMUX digital power supply
V <sub>MINUSD</sub>	A19, A20, B19, B20, E18, F18, U19, U20	ADC digital negative power supply (–2.2V)
Inputs		
CLK, CLK <sub>N</sub>	H27, J27	ADC clock differential Inputs ECL/PECL/LVDS compatible
VIN	V25, W24	ADC in-phase analog input (double pin: one of the two has to be terminated via 50Ω to ground)
VINN	V22, W23	ADC Inverted-phase analog input (double pin: one of the two must be terminated via 50Ω to ground)
Outputs		
A0...A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-phase digital outputs port A LVDS compatible
A0N...A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted-phase digital outputs port A LVDS compatible

**Table 6-1.** Pin Description (Continued)

Symbol	Pin Number	Function
AOR/DRAN, AORN/DRA	B6, A6	Port A Out Of Range bit or Port A output clock in staggered mode
B0...B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-phase digital outputs port B LVDS compatible
B0N...B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted-phase digital outputs port B LVDS compatible
BOR/DRBN, BORN/DRB	J2, H1	Port B Out Of Range bit or Port B output clock in staggered mode
C0...C9	M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	In-phase digital outputs port C LVDS compatible
C0N...C9N	L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	Inverted-phase digital outputs port C LVDS compatible
COR/DRCN, CORN/DRC	V5, W5	Port C Out Of Range bit or Port C output clock in staggered mode
D0...D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-phase digital outputs port D LVDS compatible
D0N...D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted-phase digital outputs port D LVDS compatible
DOR/DRDN, DORN/DRD	V16, W16	Port D Out Of Range bit or Port D output clock in staggered mode
DR, DRN	J1, K2	Differential output clock LVDS compatible
Control Functions Inputs		
DRRB	P27	ADC data ready reset LVCMOS (3.3V) compatible
ASYNCRST	B17	DMUX asynchronous reset
SDAEN	P26	ADC sampling delay adjust enable - SDA disabled when left floating or connected to ground - SDA enabled when connected to V <sub>EE</sub>
SDA	E27	ADC sampling delay adjust (± 0.5V range)
PGEB	A23	Pattern generator enable - Leave floating or connect to ground for normal mode - Connect to V <sub>EE</sub> for test mode
B/GB	A21	Binary or gray output coding selection - Leave floating or connect to ground for binary coding - Connect to V <sub>EE</sub> for gray coding



Table 6-1. Pin Description (Continued)

Symbol	Pin Number	Function
GA	W21	ADC gain adjust control pin ( $\pm 0.5V$ range)
CLKTYPE	V18	Connect to $V_{CCD}$
SLEEP	A18	DMUX SLEEP mode Enable - Leave floating or connect to $V_{CCD}$ for normal mode - Connect to ground for SLEEP mode
STAGG	A17	DMUX staggered mode enable - Leave floating or connect to $V_{CCD}$ for normal mode - Connect to ground for STAGG mode
DRTYPE	K1	DMUX output clock mode selection - Connect to ground for DR/2 type - Leave floating or connect to $V_{CCD}$ for DR type
RS	L2	DMUX Ratio mode selection - Connect to ground for 1:2 ratio - Leave floating or connect to $V_{CCD}$ for 1:4 ratio
BIST	V17	DMUX BIST mode - Leave floating or connect to $V_{CCD}$ for normal mode - Connect to ground for BIST mode
CLKDACTRL	U18	DMUX clock delay control (from $1/3 \times V_{CCD}$ to $2/3 \times V_{CCD}$ )
DACTRL	W18	Standalone delay cell control (from $1/3 \times V_{CCD}$ to $2/3 \times V_{CCD}$ )
DAEN	W17	Standalone delay cell enable - Delay cell disabled when left floating or connected to $V_{CCD}$ - Delay cell enabled when connected to ground
DAI, DAIN	W19, V19	Standalone delay cell differential inputs LVDS compatible
Control Functions Outputs		
DAO, DAON	W20, V20	Standalone delay cell differential outputs LVDS compatible
DIODE ADC	A22	ADC die junction temperature monitoring
NC	A1, B18, W1	No connect (leave this pin floating)

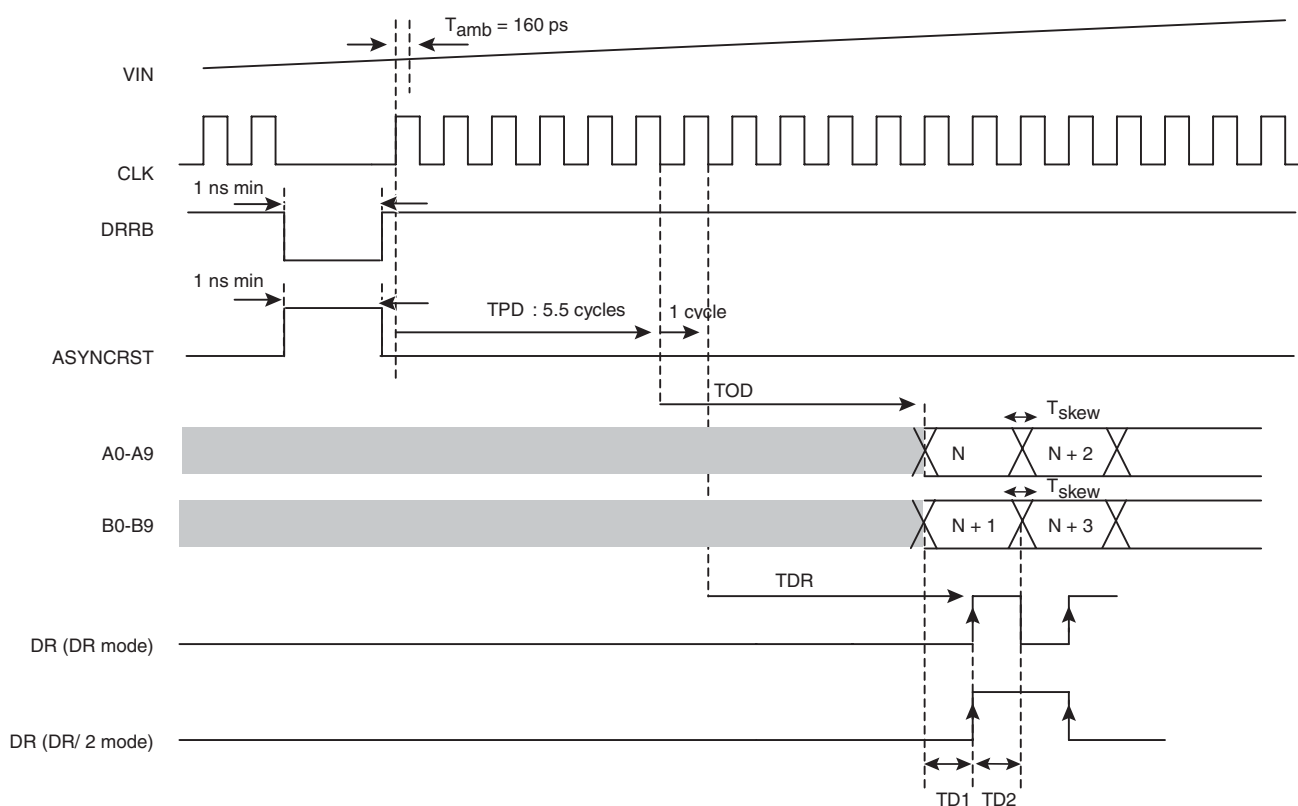
## 7. Main Features

### 7.1 Reset

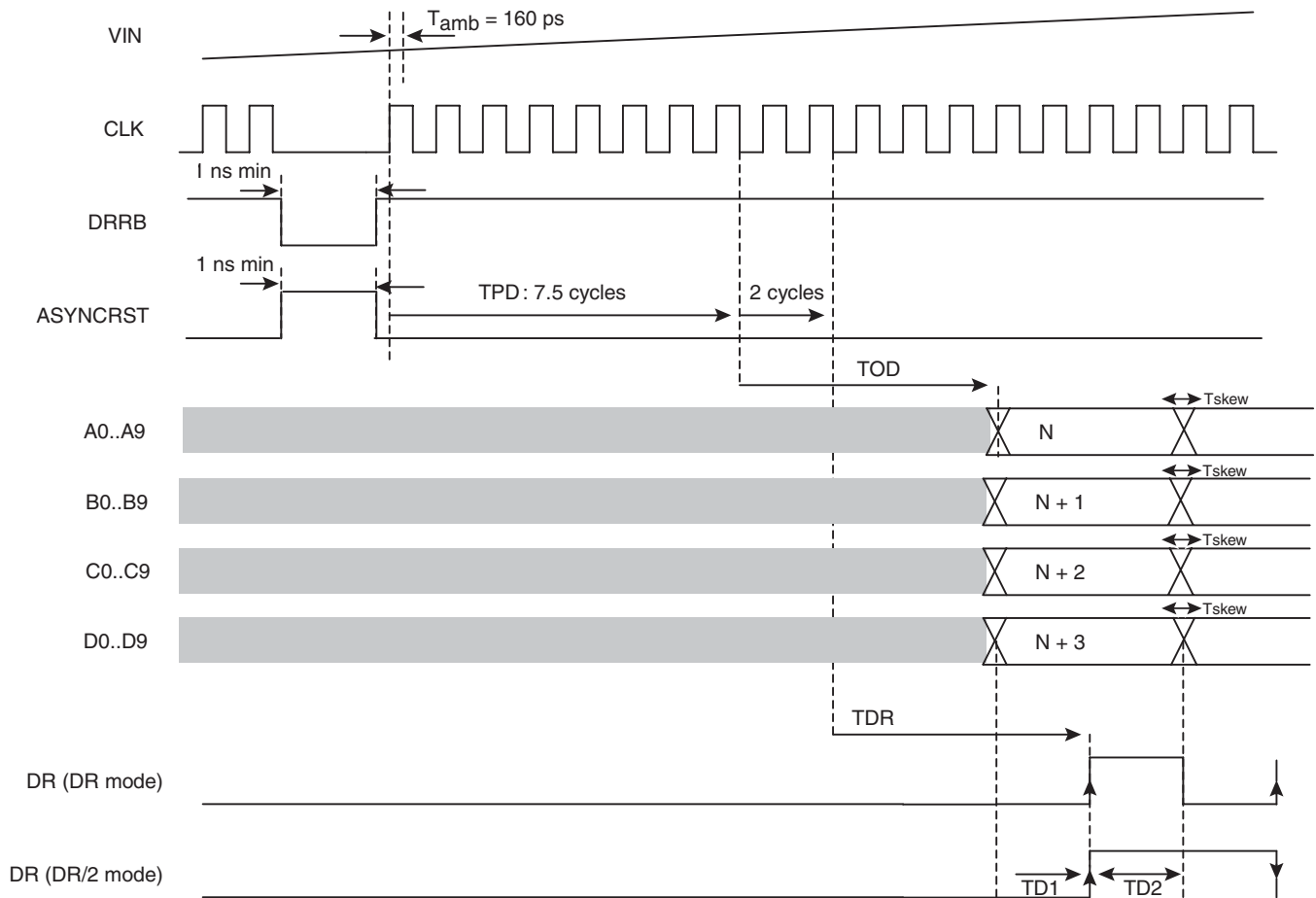
There are two reset signals available: DRRB and ASYNCRST. DRRB is active low while ASYNCRST is active high. These reset signals are required to start the device properly. It is recommended to apply both reset signals simultaneously. Please refer to the Application Section for more information on how to implement the reset functions. In the case of multiple channels, it is recommended to hold the input clock signal low during reset (as described in [Figure 7-1](#)) to ensure synchronization of the channels.

The DRRB/ASYNCRST signal frequency should be 200 MHz maximum. The reset pulse should be 1 ns minimum.

**Figure 7-1.** Asynchronous Reset Timing Diagram, 1:2 Mode, Simultaneous Mode (Principle of Operation)



**Figure 7-2.** Asynchronous Reset Timing Diagram, 1:4 Mode, Simultaneous Mode (Principle of Operation)



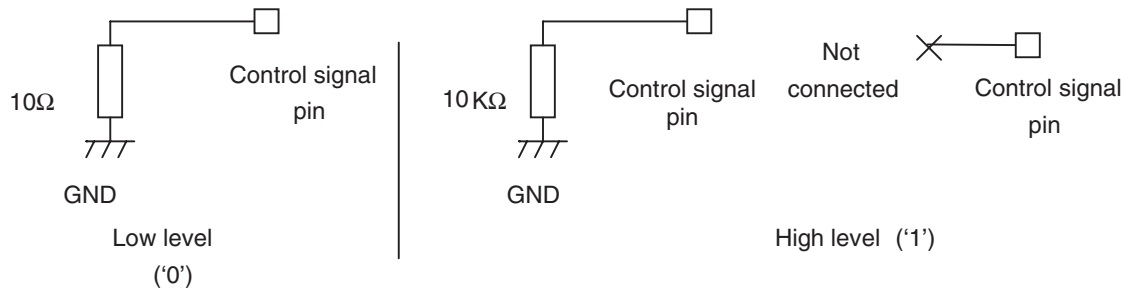
- Notes:
1. TPD time is the delay between the first rising edge after the reset signal and before the TOD or TDR delay. This time is a number of clock cycle.
  2. Definition of TOD: it is the time between the falling edge and the next point of change of data.
  3. Definition of TDR: it is the time between the falling edge and the next point of change of data ready.
  4. TOD - TDR is always lower to 600 ps over temperature and power supply.
  5.  $TD1 = TDR - TOD + 2 \text{ Clock cycles}$ .
  6.  $TD2 = TOD + 2 \text{ clock cycles} - TDR$  With  $TOD = 7.2 \text{ ns}$ . This delay is long due to the several delay lines in the DMUX.

## 7.2 Control Signal Settings

The SLEEP, RS, DAEN, STAGG, BIST and DRTYPE control signals use the same static buffer.

SLEEP, DAEN, STAGG, BIST are activated on logic low (10Ω grounded), and deactivated on logic high (10 kΩ to ground, or tied to  $V_{CCD} = 3.3V$ , or left floating). This is illustrated in [Figure 7-3](#).

**Figure 7-3.** Control Signal Setting



**Table 7-1.** DMUX Mode Settings – Summary

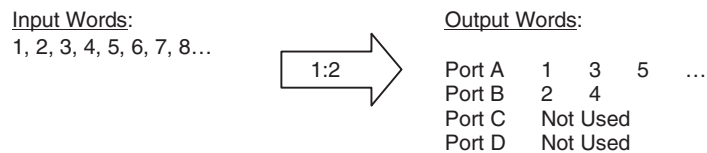
Function	Logic Level	Electrical Level	Description
BIST	0	10Ω to ground	BIST
	1	10 kΩ to ground	Normal conversion
		N/C	
SLEEP	0	10Ω to ground	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10Ω to ground	Normal conversion
		N/C	
STAGG	0	10Ω to ground	Staggered mode
	1	10 kΩ to ground	Simultaneous mode
		N/C	
DAEN	0	10Ω to ground	Standalone delay adjust activated
	1	10 kΩ to ground	Standalone delay adjust disabled
		N/C	
RS	0	10Ω to ground	1:2 ratio
	1	10 kΩ to ground	1:4 ratio
		N/C	
DRTYPE	0	10Ω to ground	DR/2 mode
	1	10 kΩ to ground	DR mode
		N/C	

### 7.3 Programmable DMUX Ratio

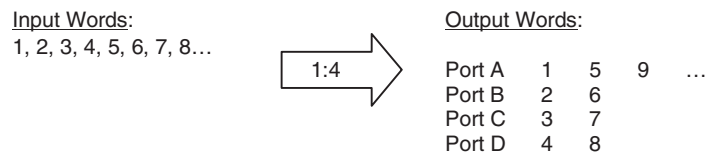
The demultiplexer ratio is programmable thanks to the RS ratio selection signal:

RS	DMUX Ratio
0	1:2
1	1:4

**Figure 7-4.** DMUX in 1:2 Ratio



**Figure 7-5.** DMUX in 1:4 Ratio



### 7.4 Output Mode (STAGG)

Two output mode are provided:

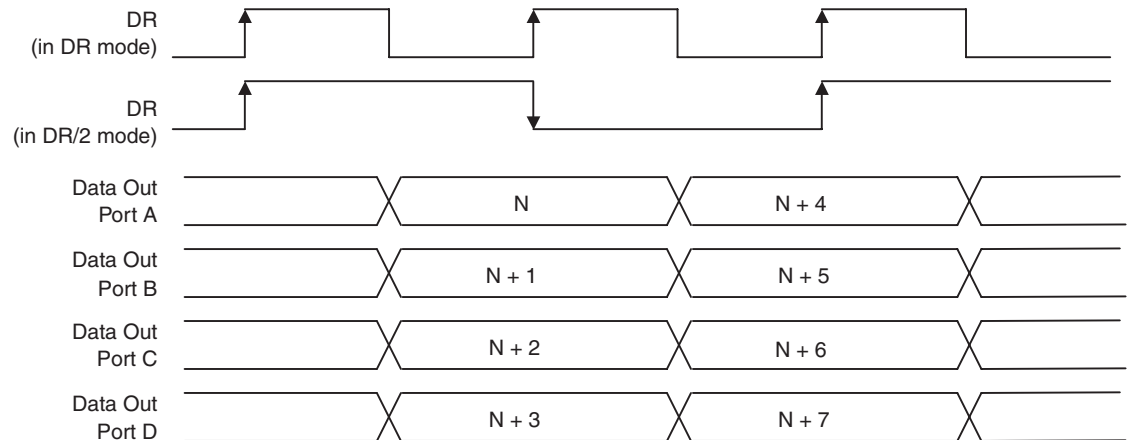
- Staggered: the output data come out of the DMUX the one after the other;
- Simultaneous: the output data come out of the DMUX at the same time.

In staggered mode, the output clock for each port is provided by the DRA, DRAN, DRB, DRBN, DRC, DRCN and DRD, DRDN signals which corresponds respectively to the AORN, AOR, BRON, BOR, CORN, COR, DORN and DOR.

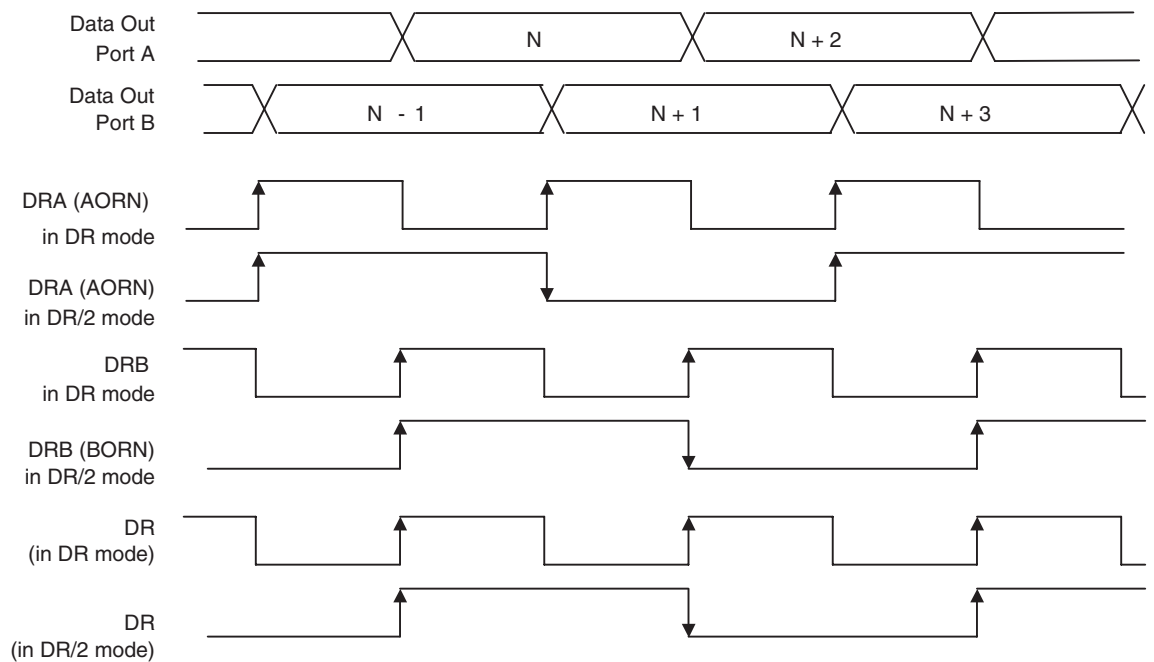
The simultaneous mode is the default mode (STAGG left floating of at logic 1).

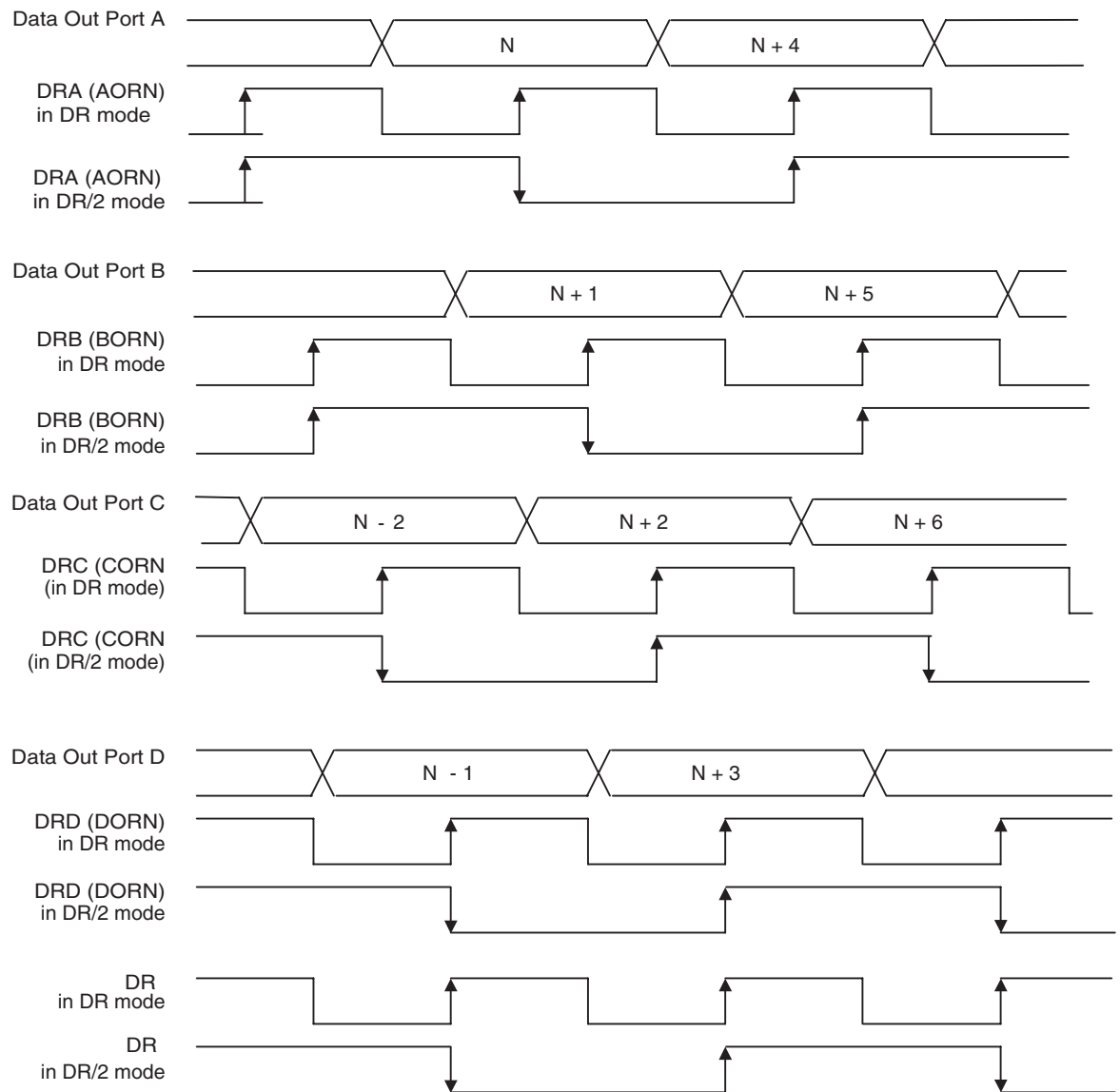
The staggered mode is activated by the means of the STAGG input (active low).

**Figure 7-6.** Simultaneous Mode in 1:4 Ratio (STAGG = 1)



**Figure 7-7.** Staggered Mode in 1:2 Ratio (STAGG = 0)



**Figure 7-8.** Staggered Mode in 1:4 Ratio (STAGG = 0)

7.5 Out Of Range Bit and Data Ready Output Clock

In simultaneous output mode:

The (AOR/DRAN, AORN/DRA), (BOR/DRBN, BORN/DRB), (COR/DRCN, CORN/DRC) and (DOR/DRDN, DORN/DRD) signals are used to process the out-of-range bit from the ADC as the ADC output data.

In 1:2 ratio, (AOR, AORN) and (BOR, BORN) will output this signal at half its initial speed.

In 1:4 ratio, (AOR, AORN), (BOR, BORN), (COR, CORN) and (DOR, DORN) will output this signal at ¼ of its initial speed.

In Staggered output mode: (AOR/DRAN, AORN/DRA), (BOR/DRBN, BORN/DRB), (COR/DRCN, CORN/DRC) and (DOR/DRDN, DORN/DRD) will output a Data Ready signal for each ports, centered on the corresponding data.

The frequency of the (DRA, DRAN), (DRB, DRBN), (DRC, DRCN) and (DRD, DRDN) depends on the DRTYPE mode (same as data in DR mode, half in DR/2 mode).

In 1:2 ratio, DR/DRN and DRB/DRBN are the same.

In 1:4 ratio, DR/DRN and DRD/DRDN are the same.

7.6 Output Clock Type Selection

Two modes for the output clock type can be chosen:

- DR mode: only the output clock rising edge is active, the output clock rate is the same as the output data rate;
- DR/2 mode: both the output clock rising and falling edges are active, the output clock rate is half the output data rate.

This is illustrated in [Figure 7-9](#) and [Figure 7-10](#).

Figure 7-9. DR Mode

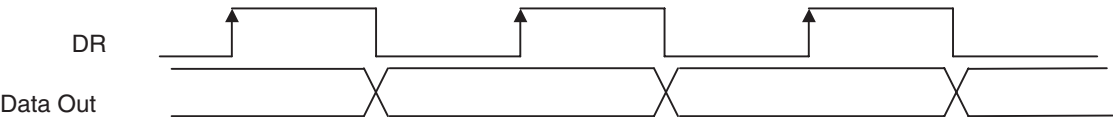


Figure 7-10. DR/2 Mode

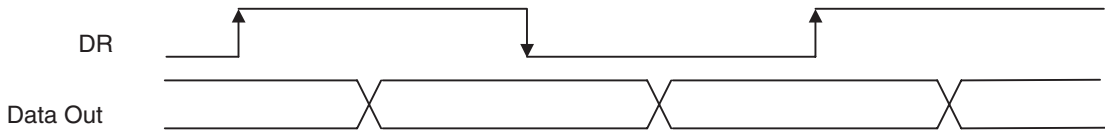


Table 7-2. Table 8. DMUX Output Clock Type Selection Settings

DRTYPE	DMUX Output Clock Type
1	DR
0	DR/2

When DRTYPE is left floating, the default mode is DR.



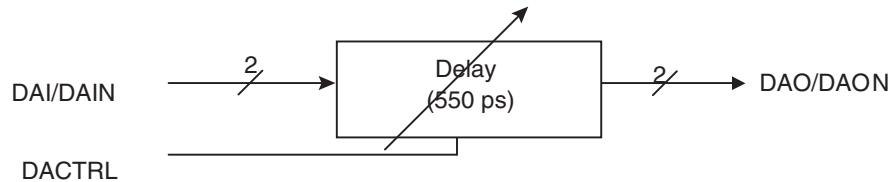
## 7.7 Power Reduction Mode (SLEEP)

The power reduction (SLEEP) mode allows the user to reduce the power consumption of the device (demultiplexing part in Sleep mode). In this mode, the device's consumption is reduced to 5W. The Power reduction mode is active when SLEEP is low. The device is in normal mode when SLEEP is high.

## 7.8 Standalone Delay Cell

A standalone delay cell is provided to allow the user to add a delay on the DAI/DAIN differential input signal. The delay is controlled via the DACTRL. The tuning range is about 550 ps varying from  $V_{CCD} / 3$  to  $(2 \times V_{CCD}) / 3$ . This function results in a delayed output signal: DAO/DAON. The DAI/DAIN and DAO/DAON are LVDS signals.

**Figure 7-11.** Standalone Delay Cell Block Diagram

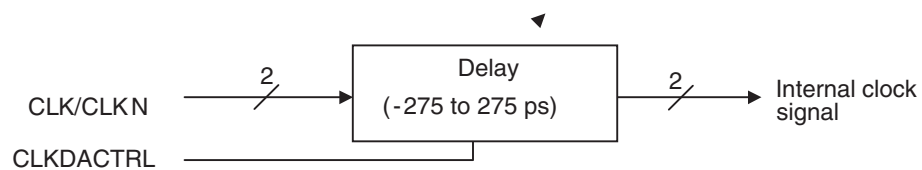


## 7.9 Clock input Delay Cell

A delay cell is provided to allow the user to tune the delay between clock and data at the DEMUX input. The delay is controlled via the CLKDACTRL. It ranges from  $-275$  ps to  $275$  ps for CLKDACTRL varying from  $V_{CCD} / 3$  to  $(2 \times V_{CCD}) / 3$ .

This function results in a delayed internal clock signal.

**Figure 7-12.** Standalone Delay Cell Block Diagram



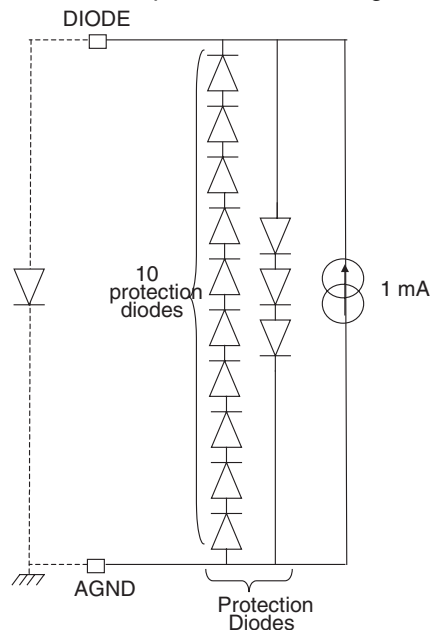
## 7.10 Built-In Self Test

The Built-in Self Test allows to test rapidly the DMUX block of the device. It is activated via the BIST bit (active low). When this signal is left floating, the BIST is inactive.

When in BIST mode, a clock must be applied to the device, which can be set to 1:2 or 1:4 mode. The output clock mode DRTYPE can be either DR or DR/2. In the BIST mode, all the bits are either all at low or high level (even and odd bits are in phase opposition) and transition every new cycle. For proper operation of the Built-In Self Test,  $V_{CCD}$  should be set to 3.3V minimum.

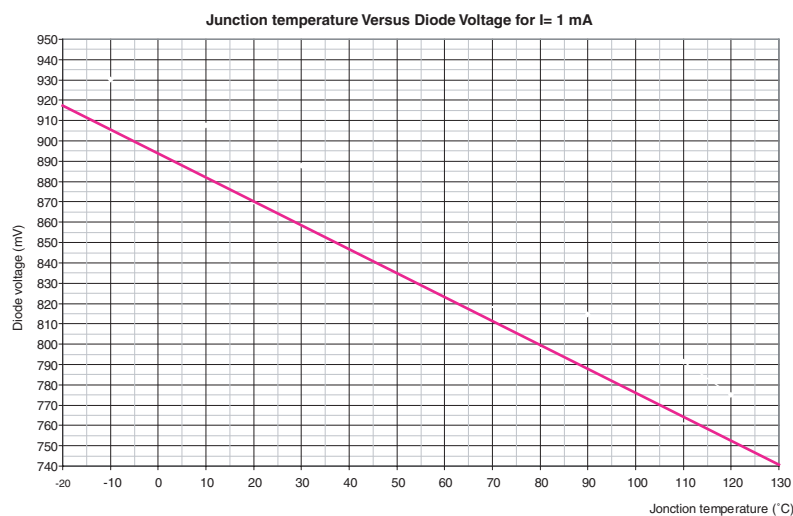
## 7.11 ADC Die Junction Temperature Monitoring

A die junction temperature measurement setting is available, for maximum junction temperature monitoring (hot point measurement). The measurement method consists in forcing a 1 mA current into a diode mounted transistor and sensing the voltage across the DIODE pin and the closest available ground pin. The measurement setup is described in [Figure 7-13 on page 34](#).

**Figure 7-13.** ADC Diode for Die Junction Temperature Monitoring Setup (10 in parallel of 3)**Caution:**

Respect the current source polarity. In all cases, make sure that the maximum voltage compliance of the current source is limited to a maximum of 1V or use a resistor mounted in series with the current source to avoid damages, which may occur to the transistor device (this may occur for instance if the current source is connected in reverse).

The diode VBE forward voltage versus junction temperature (in steady state conditions) characteristic is given in [Figure 7-14](#). The forward voltage drop, ( $V_{DIODE}$ ) across diode component, versus junction temperature, (including chip parasitic resistance), is given below ( $I_{DIODE} = 1 \text{ mA}$ ).

**Figure 7-14.** ADC Diode Characteristic ( $I = 1 \text{ mA}$ )

**Note:** The operating die junction temperature must be kept below 125°C, to ensure long term device reliability.

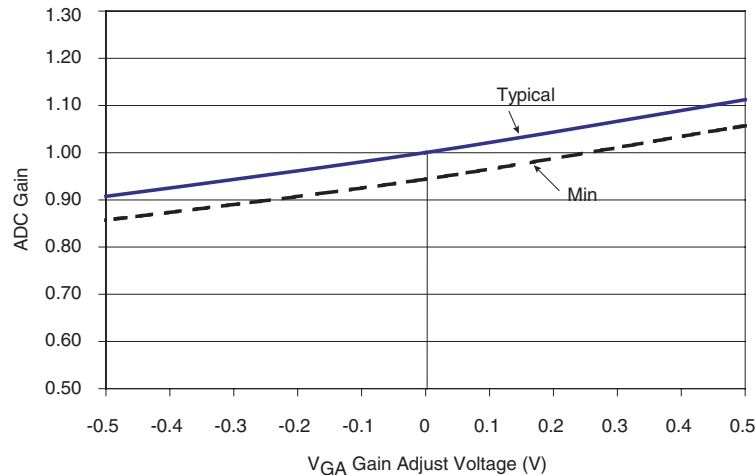
## 7.12 Pattern Generator Function

The Pattern Generator function (enabled by connecting pin PGEB to  $V_{EE} = -5V$ ) allows to check rapidly the ADC operation thanks to a checker board pattern delivered internally to the ADC. Each output bit of the ADC should toggle from 0 to 1 successively. At the AT84AS004 output, all bits of each port are all 1 or all 0. The data on each port is either 0x2AA either 0x155 and does not change over clock cycles.

## 7.13 ADC Gain Control

The ADC gain is adjustable by the means of the pin W21 of the EPGA package.

The gain adjust transfer function is given below:

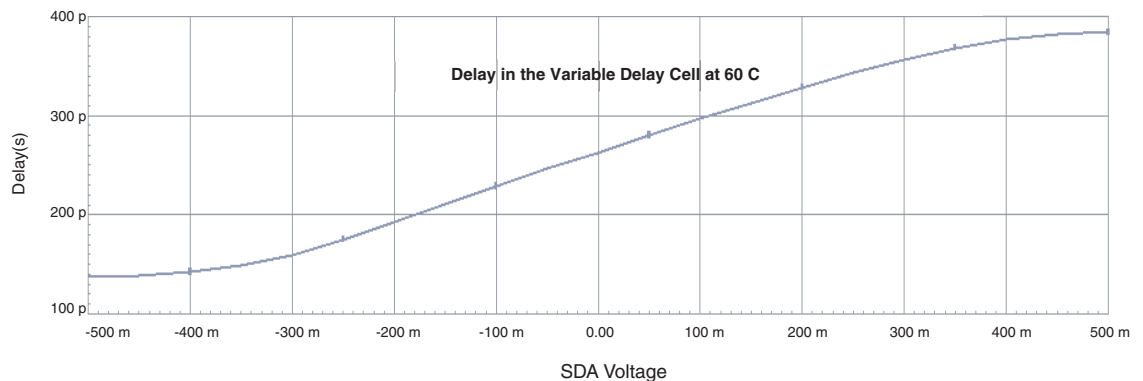


## 7.14 Sampling Delay Adjust

Sampling delay adjust (SDA pin) allows to fine tune the sampling ADC aperture delay TAD around its nominal value (160ps). This functionality is enabled thanks to the SDAEN signal, which is active when tied to  $V_{EE}$  and inactive when tied to GND.

This feature is particularly interesting for interleaving ADCs to increase sampling rate. The variation of the delay around its nominal value as a function of the SDA voltage is shown in the following graph (simulation result).

**Figure 7-15.** Typical Tuning Range is  $\pm 120$  ps for Applied Control Voltage Varying Between  $-0.5V$  to  $0.5V$  on SDA pin.

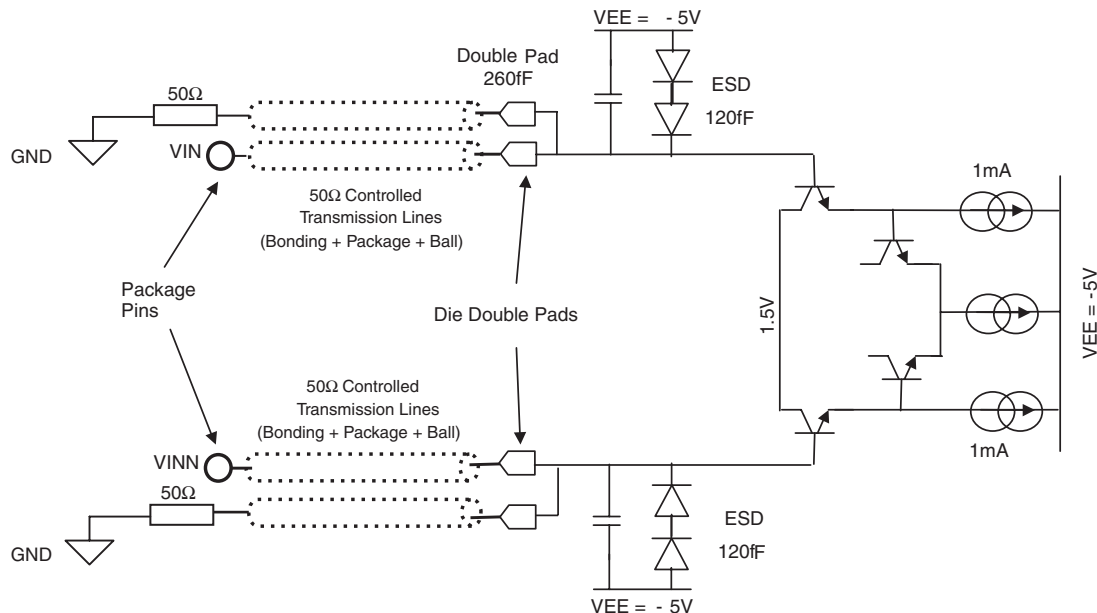


Note: The variation of the delay in function of the temperature is negligible.

## 8. Equivalent Input/Output Schematics

### 8.1 Equivalent Analog Input Circuit and ESD Protection

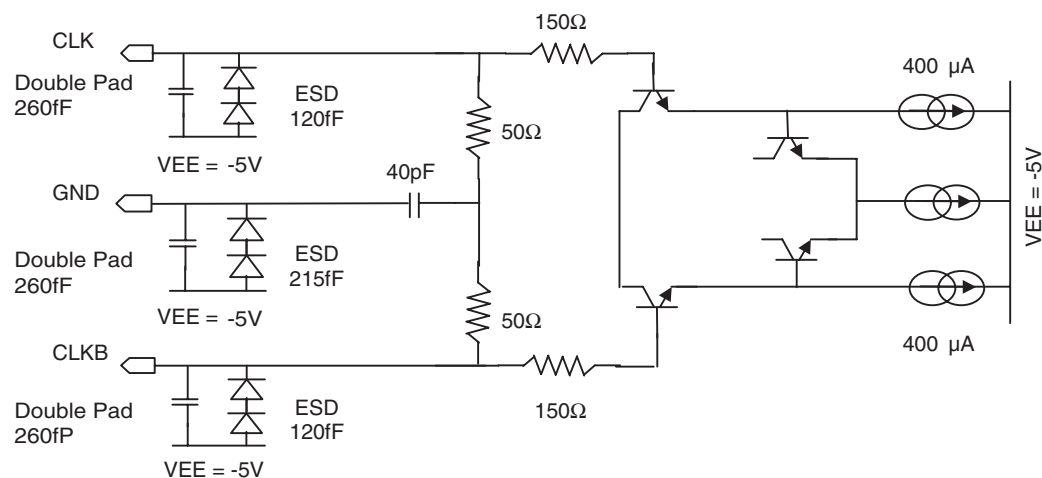
**Figure 8-1.** AT84AS004 Analog Input Buffer Schematic (VIN/VINN)



Note: External 50Ω reverse termination are required.

### 8.2 Equivalent Clock Input Circuit and ESD Protection

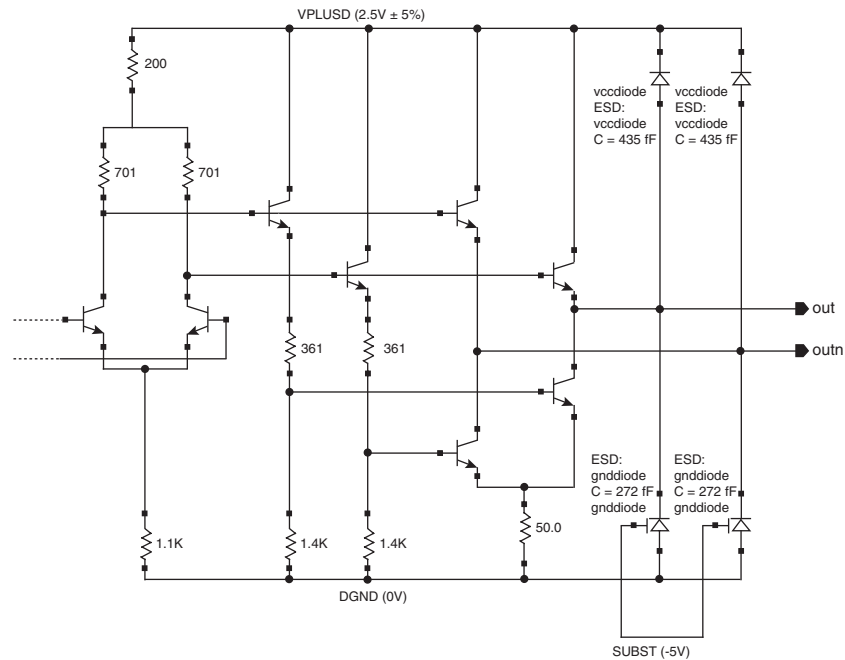
**Figure 8-2.** AT84AS004 Clock Input Buffer Schematic (CLK/CLKN)



Note: The 100Ω termination mid point is on chip and AC coupled to ground through a 40 pF capacitor.

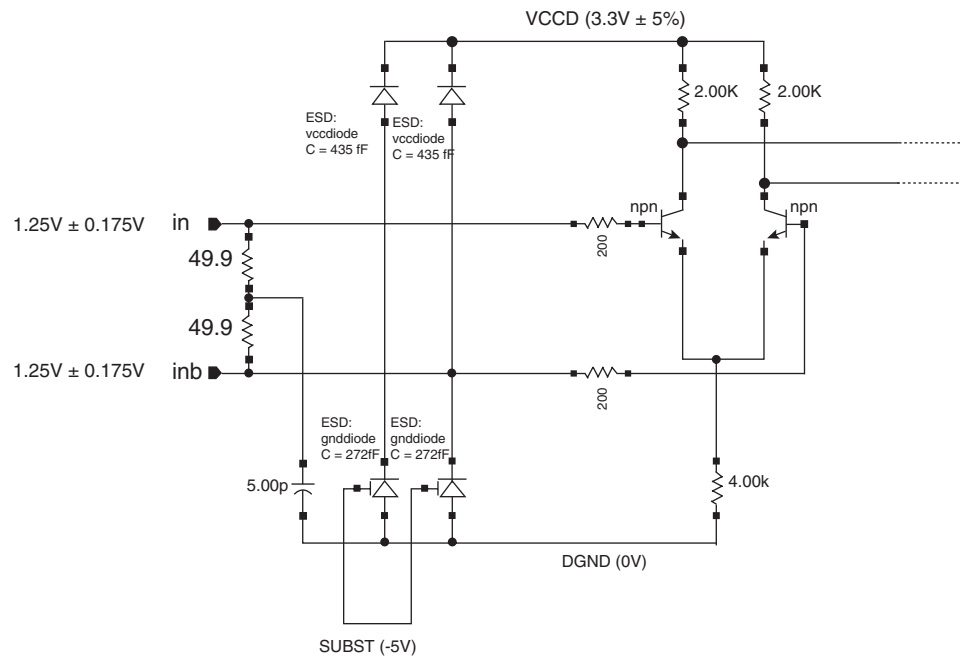
### 8.3 Equivalent Data/Clock Output Buffer Circuit and ESD Protection

**Figure 8-3.** AT84AS004 Data (Ai/AiN...Di/DiN), Clock (DR/DRN) and DAO/DAON Output Buffer Schematic



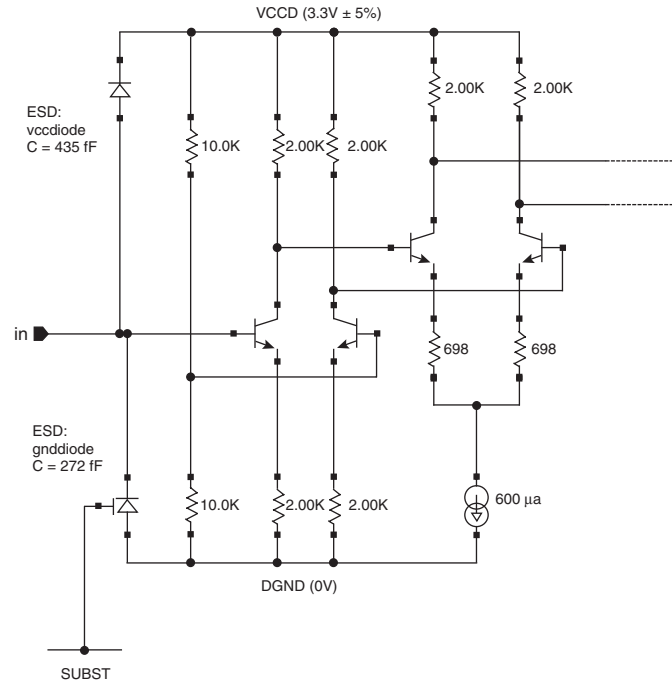
### 8.4 Standalone Delay Cell Data Input (DAI/DAIN) Buffer Circuit and ESD Protection

**Figure 8-4.** AT84AS004 Standalone Delay Cell Input DAI/DAIN Buffer Schematic



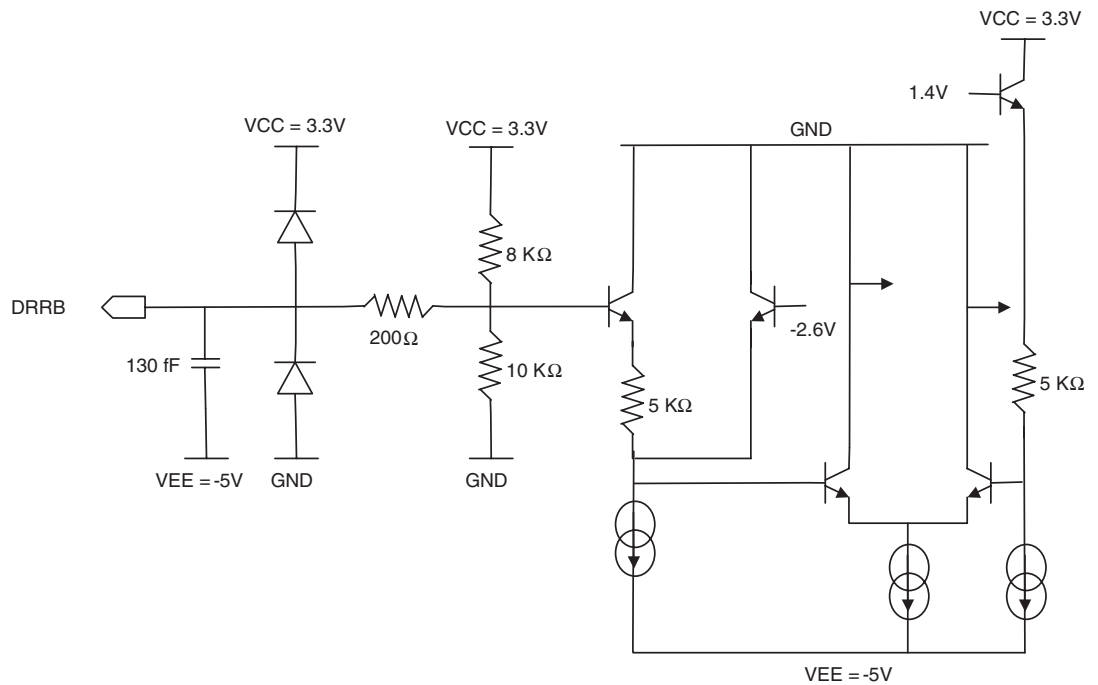
## 8.5 Delay Cell (DACTRL/DACTRLN and CLKCTRL/CLKCTRLN) Control Input Schematic and ESD Protection

**Figure 8-5.** AT84AS004 Delay Cell Control Input DACTRL/DACTRLN and CLKCTRL/CLKCTRLN Buffer Schematic



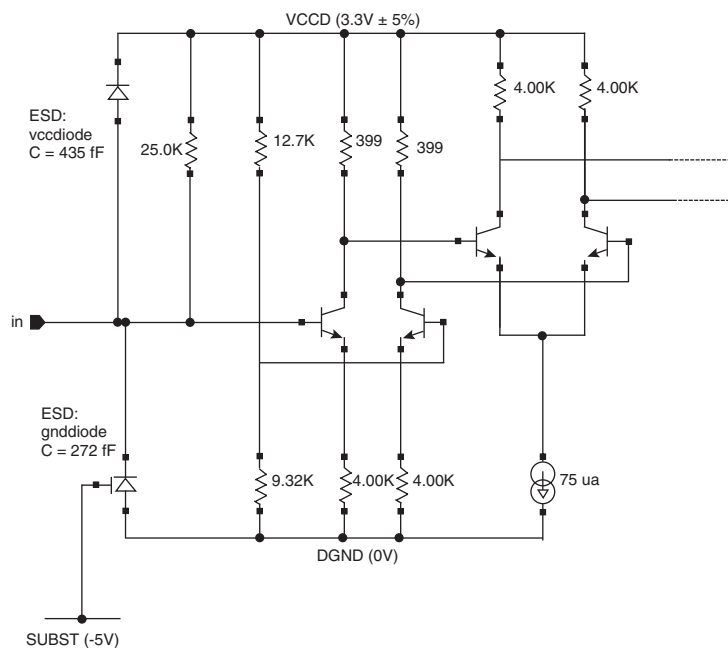
## 8.6 DRRB Equivalent Input Schematic and ESD Protection

**Figure 8-6.** AT84AS004 DRRB Reset Input Buffer Schematic



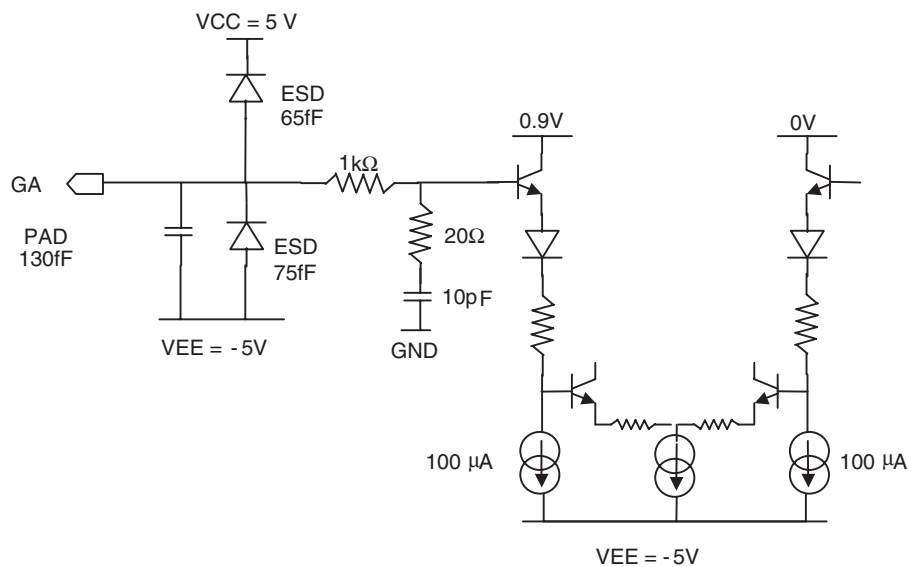
## 8.7 ASYNCRST Equivalent Input Schematic and ESD Protection

Figure 8-7. AT84AS004 Asynchronous Reset ASYNCRST Buffer Schematic



## 8.8 ADC Gain Adjust Equivalent Input Circuits and ESD Protection

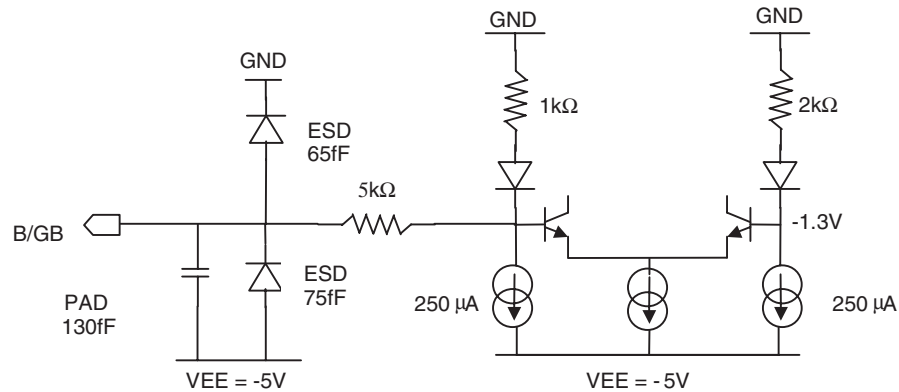
Figure 8-8. AT84AS004 Gain Adjust Control Input Buffer Schematic (GA)





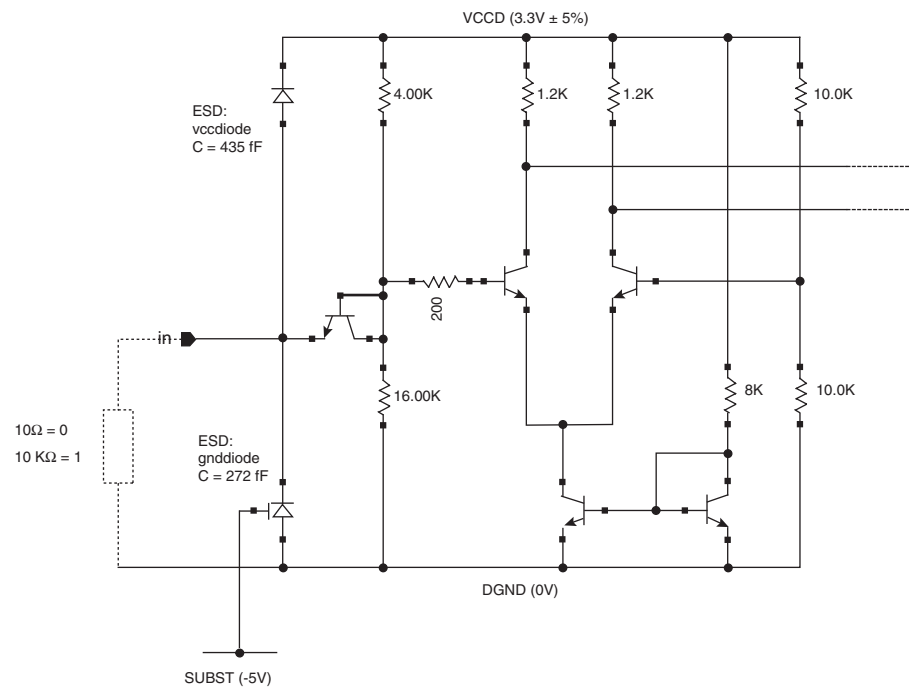
## 8.9 B/GB, SDAEN and PGEB Equivalent Input Schematics and ESD Protection

**Figure 8-9.** AT84AS004 B/GB, SDAEN and PGEB, Control Buffer Schematic



## 8.10 Control Signals Input Buffers and ESD Protection

**Figure 8-10.** AT84AS004 Control Signals Buffer Schematic (RS, DRTYPE, BIST, SLEEP, STAGG, RS, DAEN)



## 9. Definitions of Terms

**Table 9-1.** Definition of Terms

(Fs max)	Maximum sampling frequency	Sampling frequency for which ENOB < 6bit.s
(Fs min)	Minimum sampling frequency	Sampling frequency for which the ADC Gain has fallen by 0.5 dB with respect to the gain reference value. Performances are not guaranteed below this frequency.
(BER)	Bit error rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than $\pm 32$ LSB from the correct code.
(FPBW)	Full power input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale $-1$ dB ( $-$ dBFS).
(SSBW)	Small signal input bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale $-10$ dB ( $-10$ dBFS).
(SINAD)	Signal-to-noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale ( $-1$ dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	Signal-to-noise ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below full-scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.
(THD)	Total harmonic distortion	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full-scale. It may be reported in dB (that is, related to converter $-1$ dB full-scale), or in dBc (i.e, related to input signal level).
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (that is, related to converter $-1$ dB full-scale), or in dBc (i.e, related to input signal level).
(ENOB)	Effective number of bits	$ENOB = \frac{SINAD - 1 \cdot 76 + 20 \log \frac{A}{FS/2}}{6 \cdot 02}$ <p>Where A is the actual input amplitude and V is the full-scale range of the ADC under test.</p>
(DNL)	Differential nonlinearity	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	integral nonlinearity	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all INL (i).
(TA)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (VIN,VINB) is sampled.

**Table 9-1.** Definition of Terms (Continued)

(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	Settling time	Time delay to achieve 0.2 % accuracy at the converter output when a 80% full-scale step function is applied to the differential analog input.
(ORT)	Over voltage recovery time	Time to recover 0.2% accuracy at the output, after a 150 % full-scale step applied on the input is reduced to midscale.
(TOD)	Digital data output delay	Delay from the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TDR)	Data ready output delay	Delay from the falling edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TD1)	Time delay from data transition to data ready	General expression is $TD1 = TDR - TOD + 2 \text{ Clock cycles}$
(TD2)	Time delay from data ready to data	General expression is $TD2 = TOD + 2 \text{ clock cycles} - TDR$
(TC)	Encoding clock period	$TC1 = \text{Minimum clock pulse width (high)}$ $TC = TC1 + TC2$ $TC2 = \text{minimum clock pulse width (low)}.$
(TPD)	Pipeline delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	Power supply rejection ratio	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	Nonreturn to zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the out-of-range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out-of-range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	Intermodulation distortion	The two tones inter modulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermediation products.
(NPR)	Noise power ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	Voltage standing wave ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (i.e.. 99% power transmitted and 1% reflected).

## 10. Thermal and Moisture Characteristics

As there is no JEDEC standard definition for the thermal resistance applied to a multi-die device, only the thermal resistance for each die (ADC block powered on only or DMUX block powered on only) is provided. For easy understanding of the thermal behavior of the device, thermal data with both devices powered on are however provided.

All results were computed with ANSYS thermal simulation tool and with the following assumptions:

- Half geometry simulation
- DC heating zone =  $1.9 \times 1.9 \text{ mm}^2$
- MUX heating  $4.0 \times 4.0 \text{ mm}^2$
- No air, pure conduction, no radiation

### 10.1 Thermal Resistance from Junction To Bottom of Balls

When both blocks are powered on, the thermal simulation results in:

- Temperature at the center of the ADC block =  $32.9^\circ\text{C}$
- Temperature at the center of the DMUX block =  $13.6^\circ\text{C}$

When each block is powered on at a time, the resulting thermal resistance from junction to bottom of balls is:

- Rth Junction-bottom of balls (ADC block on only) =  $7^\circ\text{C/W}$
- Rth Junction-bottom of balls (DMUX block on only) =  $3.9^\circ\text{C/W}$

### 10.2 Thermal Resistance from Junction To Top of Case

When both blocks are powered on, the resulting thermal resistance from junction to top of case is:

- Temperature at the center of the ADC block =  $18.5^\circ\text{C}$
- Temperature at the center of the DMUX block =  $4.1^\circ\text{C}$

When each block is powered on at a time, the resulting thermal resistance from junction to top of case is:

- Rth Junction- top of case (ADC block on only) =  $4.1^\circ\text{C/W}$
- Rth Junction- top of case (DMUX block on only) =  $1.5^\circ\text{C/W}$

### 10.3 Thermal Resistance from Junction To Board

When both blocks are powered on, the resulting thermal resistance from junction to board is:

- Temperature at the center of the ADC block =  $57.6^\circ\text{C}$
- Temperature at the center of the DMUX block =  $37.3^\circ\text{C}$

When each block is powered on at a time, the resulting thermal resistance from junction to board is:

- Rth Junction- board (ADC block on only) =  $8^\circ\text{C/W}$
- Rth Junction- board (DMUX block on only) =  $4.9^\circ\text{C/W}$

Note: Assumed board size =  $53 \times 43 \text{ mm}^2$

## 10.4 Thermal Resistance from Junction To Ambient

When both blocks are powered on, the resulting thermal resistance from junction to ambient is:

- Temperature at the center of the ADC block =  $106^{\circ}\text{C}$
- Temperature at the center of the DMUX block =  $85.3^{\circ}\text{C}$

When each block is powered on at a time, the resulting thermal resistance from junction to ambient is:

- $R_{\text{th}}$  Junction- ambient (ADC block on only) =  $17.1^{\circ}\text{C/W}$
- $R_{\text{th}}$  Junction- ambient (DMUX block on only) =  $13.9^{\circ}\text{C/W}$

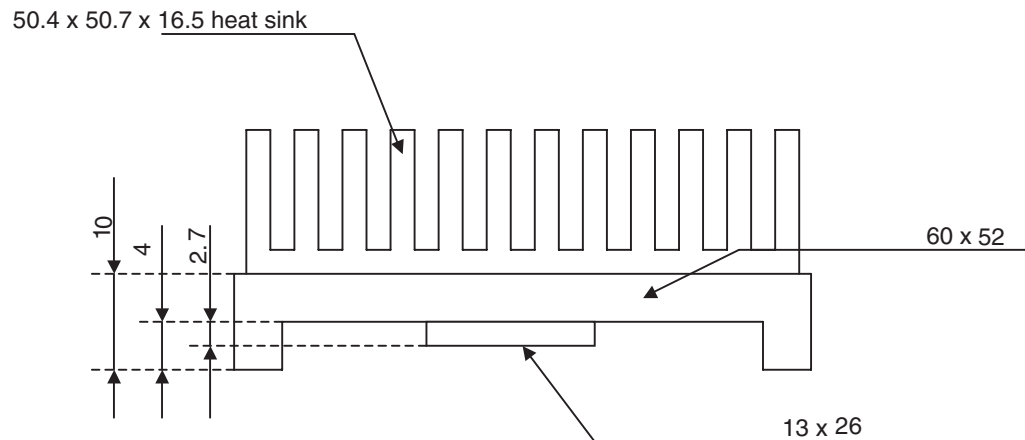
## 10.5 Thermal Management Recommendations

In still air and  $25^{\circ}\text{C}$  ambient temperature conditions, the maximum temperature of  $106^{\circ}\text{C} + 25^{\circ}\text{C} = 131^{\circ}\text{C}$  is reached for the ADC block. It is consequently necessary to manage the heat from the AT84AS004 very carefully to avoid permanent damages of the device due to over temperature operation.

In no air cooling conditions, an external heatsink must be placed on top of package. An electrical isolation may be necessary as the top of the package is at  $V_{EE} = -5\text{V}$  potential.

It is advised to use an external heatsink with intrinsic thermal resistance better than  $4^{\circ}\text{C/Watt}$  when using air at room temperature  $20\sim 25^{\circ}\text{C}$ . At  $60^{\circ}\text{C}$ , the external heatsink should have an intrinsic thermal resistance better than  $3^{\circ}\text{C/Watt}$ . [Figure 10-1](#) provides the outlines of the heat sink used on the AT84AS004-EB evaluation board.

**Figure 10-1.** AT84AS004-EB Evaluation Board Heat Sink Outlines



Note: All units are in mm

## 10.6 Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard).

Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 260°C for ROHS versions and 220°C for non ROHS versions) must be:

- Mounted within 168 hours at factory conditions of  $\pm 30^\circ\text{C}/60\%$  RH, or
- Stored at  $\pm 20\%$  RH

Devices require baking, before mounting, if Humidity Indicator is >20% when read at 23°C  $\pm 5^\circ\text{C}$ .

If baking is required, devices may be baked for:

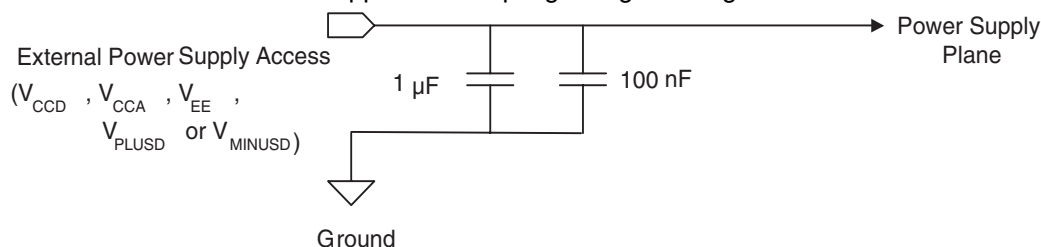
- 192 hours at 40°C + 5°C/–0°C and <5% RH for low temperature device containers, or
- 24 hours at 125°C  $\pm 5^\circ\text{C}$  for high-temperature device containers.

## 11. Applying the AT84AS004

### 11.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1  $\mu\text{F}$  in parallel to 100 nF.

**Figure 11-1.** AT84AS004 Power supplies Decoupling and grounding Scheme



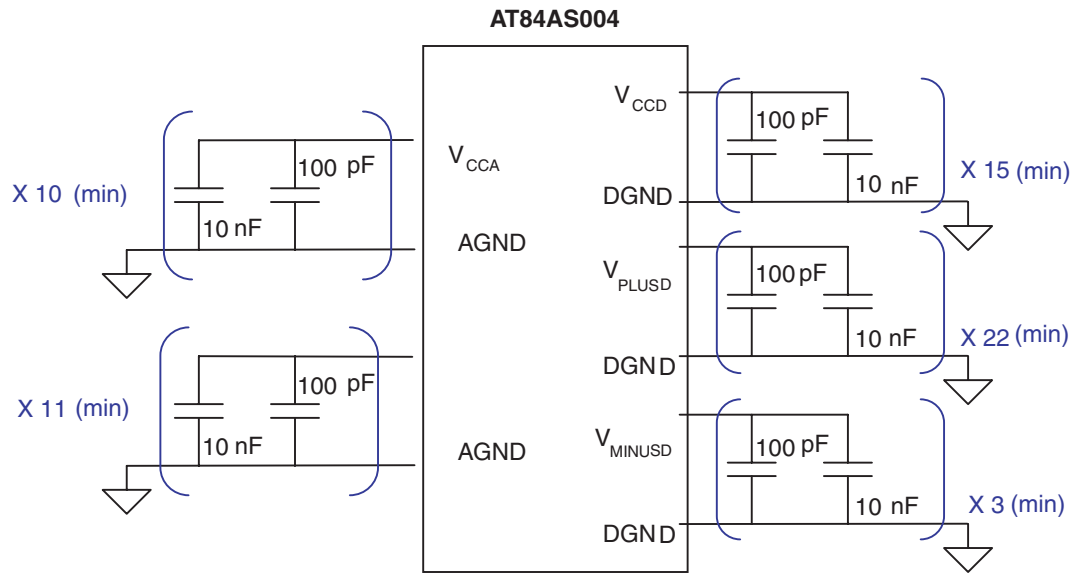
Note:  $V_{\text{CCD}}$  and  $V_{\text{CCA}}$  planes should be separated but the two power supplies can be reunited by a strap on the board.

Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required pairs of capacitors by power supply type is:

- 10 for  $V_{\text{CCA}}$
- 15 for  $V_{\text{CCD}}$
- 11 for  $V_{\text{EE}}$
- 22 for  $V_{\text{PLUSD}}$
- 3 for  $V_{\text{MINUSD}}$

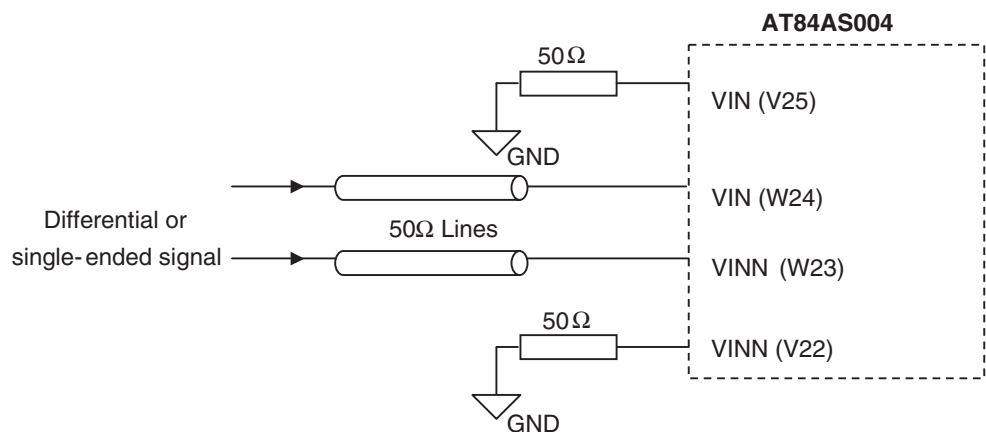
**Figure 11-2.** AT84AS004 Power Supplies Bypassing Scheme



## 11.2 Analog Input Implementation

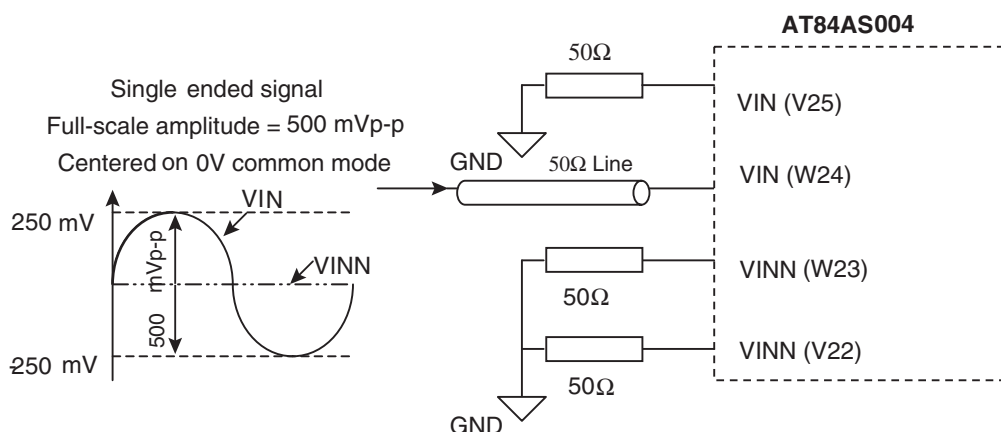
Two pins are available for each positive ( $V_{IN}$ ) and negative ( $V_{INN}$ ) inputs. It is necessary to terminate one of each input pair by  $50\Omega$  to ground as close as possible to the EPGA package pins. This is illustrated in [Figure 11-3](#).

**Figure 11-3.** AT84AS004 Analog Input Reverse Termination Scheme



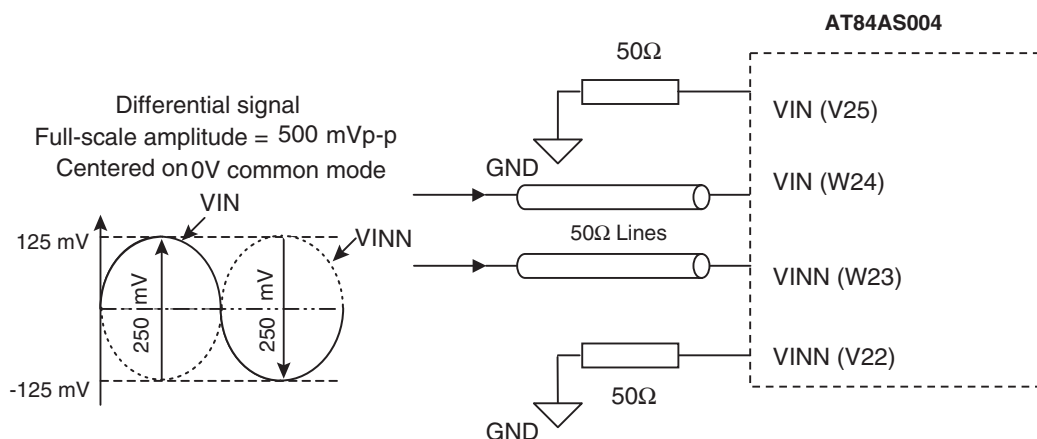
The analog input of the AT84AS004 device can be indifferently entered in single-ended or differential mode.

**Figure 11-4.** AT84AS004 Analog Input Termination Scheme (Single-ended)



**Note:** The two 50Ω terminations connected to the two negative inputs (VINN) can be replaced by one 25Ω resistor to ground.

**Figure 11-5.** AT84AS004 Analog Input Termination Scheme (Differential)



## 11.3 Clock Input Implementation

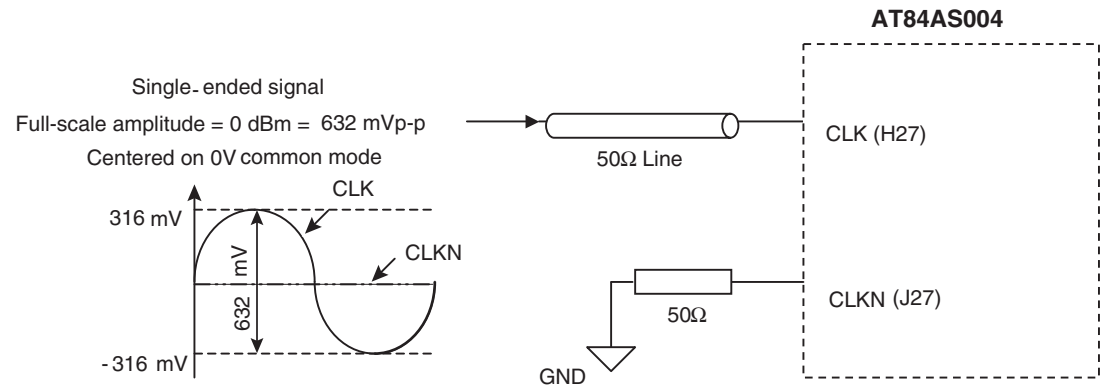
Please refer to the ADC Application Note AT84AS003/4 for a recommended clock input AC coupling scheme. The AT84AS004 clock inputs (CLK/CLKN) are designed for either single-ended or differential operation but it is recommended to drive the clock differentially to optimize the device's performances at high frequencies. No external 50Ω termination are required for the clock inputs (CLK/CLKN) as they are already on-chip terminated by two 50Ω resistors connected to ground via an on-chip 40 pF capacitor.

The AT84AS004 input clock can be used in either DC coupled (0V common mode) or AC coupled (ECL, LVDS for example) mode. It is recommended to use a differential sinewave signal (0 dBm or 894 mVp-p differential) centered on 0V common mode to drive the clock signals. A balun (with  $\sqrt{2}$  ratio) may then be necessary to convert the single-ended clock signal to a differential clock signal.

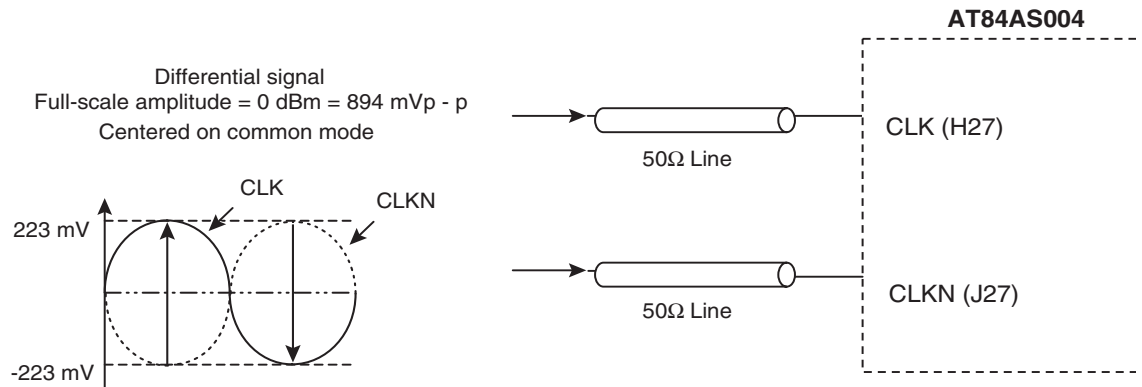


Note: If the clock frequency is fixed, then it is recommended to narrow-band filter the clock signal in order to minimize its jitter and the integrated noise over the band of interest.

**Figure 11-6.** AT84AS004 Clock Input Termination Scheme (Single-ended)



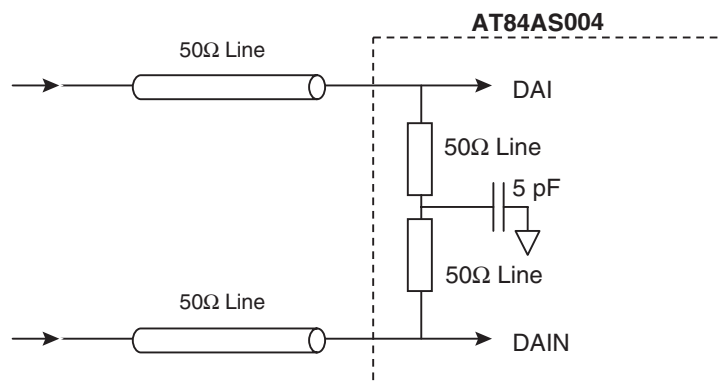
**Figure 11-7.** AT84AS004 Clock Input Recommended Termination Scheme (Differential)



## 11.4 LVDS Input Implementation

The DAI/DAIN input data of the standalone delay cell is LVDS compatible. It is  $2 \times 50\Omega$  differentially on-chip terminated as described in [Figure 11-8](#).

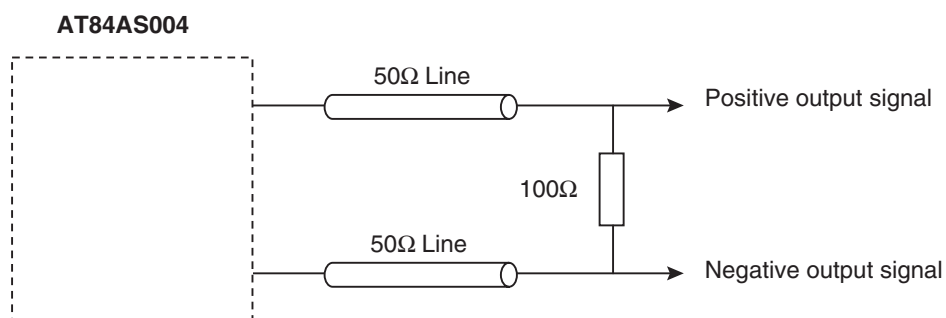
**Figure 11-8.** AT84AS004 LVDS Input (DAI/DAIN) Termination Scheme



## 11.5 LVDS Output Implementation

The data (Ai/AiN...Di/DiN, AOR/AORN...DOR/DORN and DAO/DAON) and clock outputs (DR/DRN) are LVDS compatible. They have to be  $100\Omega$  differentially terminated as described in [Figure 11-9](#).

**Figure 11-9.** AT84AS004 LVDS Output Termination Scheme

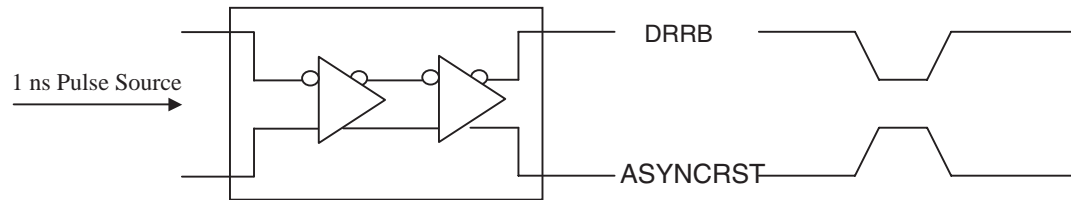


## 11.6 DRRB and ASYNCRST Implementation

The DRRB and ASYNCRST are required to start the device properly. DRRB is active at low level while ASYNCRST is active at high level.

As it is recommended to apply both reset signals simultaneously, one possible solution is to use a differential driver so that DRRB and ASYNCRST are generated as the two signals of a differential pair. This would allow for both the simultaneous application of the signals to the device a simple way to drive both signals. An example is provided below, [Figure 11-10](#).

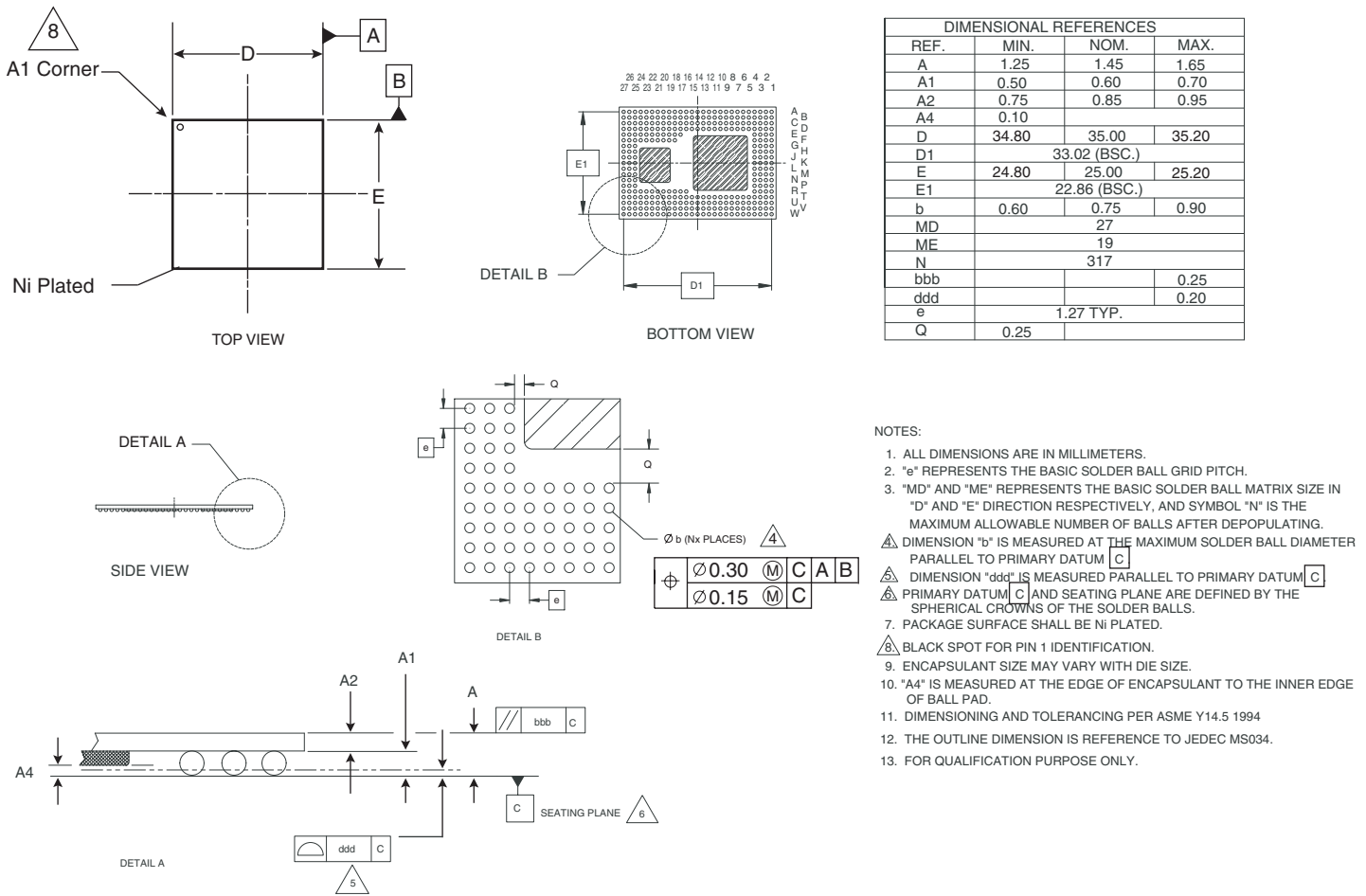
**Figure 11-10.** AT84AS004 DRRB and ASYNCRST Driver Scheme



Please refer to the AT84AS003/4 ADC Application Note for Reset implementation.

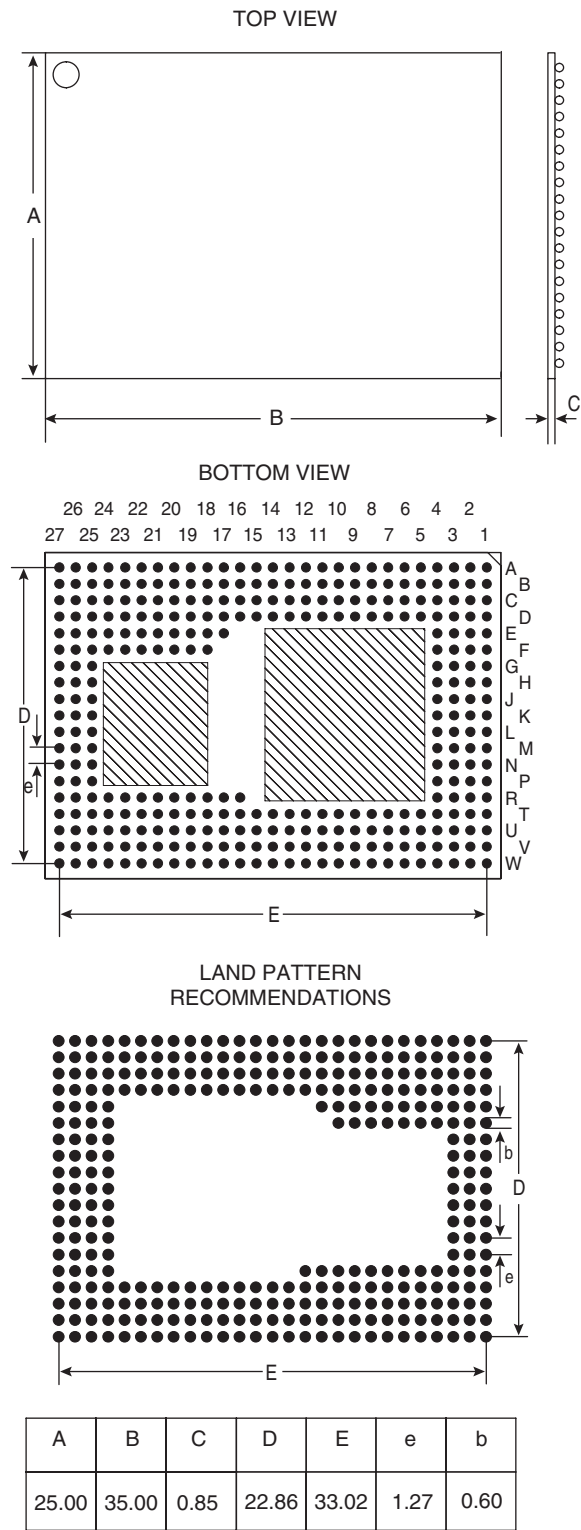
12. Package Information

Figure 12-1. EBGA317 Package Outline



Note: The two pads at the bottom of the EBGA package are the dice moldings and should not be soldered to the board.

Figure 12-2. Land Pattern Recommendation



## 13. Ordering Information

**Table 13-1.** Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84AS004CTP	EBGA 317	Commercial C $0^{\circ}\text{C} < T_{\text{amb}}, T_{\text{J}} < 90^{\circ}\text{C}$	Standard	Contact e2v sales
AT84AS004VTP	EBGA 317	Industrial V $-40^{\circ}\text{C} < T_{\text{amb}}, T_{\text{J}} < 110^{\circ}\text{C}$	Standard	Contact e2v sales
AT84AS004CTPY	EBGA 317 RoHS	Commercial C $0^{\circ}\text{C} < T_{\text{amb}}, T_{\text{J}} < 90^{\circ}\text{C}$	Standard	Contact e2v sales
AT84AS004VTPY	EBGA 317 RoHS	Industrial V $-40^{\circ}\text{C} < T_{\text{amb}}, T_{\text{J}} < 110^{\circ}\text{C}$	Standard	Contact e2v sales
AT84AS004TP-EB	EBGA 317	Ambient	Standard	Evaluation kit

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